

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

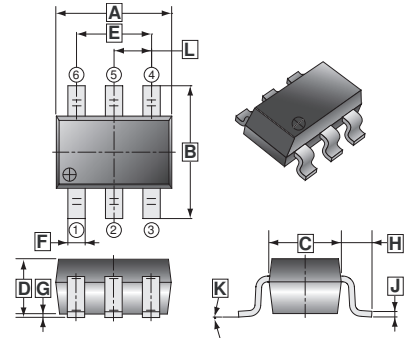
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSOP-6 saves board space
- Fast switching speed
- High performance trench technology

APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

TSOP-6

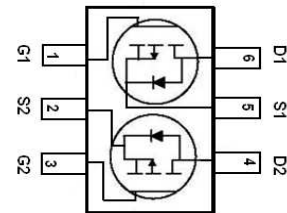


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	MAX.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7 inch

Top View



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current ¹	$T_A=25^\circ\text{C}$	I_D	-2.5	A
	$T_A=70^\circ\text{C}$		-1.9	
Pulsed Drain Current ²		I_{DM}	-10	A
Continuous Source Current (Diode Conduction) ¹		I_S	-1.6	A
Power Dissipation ¹	$T_A=25^\circ\text{C}$	P_D	1.15	W
	$T_A=70^\circ\text{C}$		0.7	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating				
Maximum Junction to Ambient ¹	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	110	$^\circ\text{C} / \text{W}$
	Steady State		150	

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-0.6	-	-	V	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{DS}=0$, $V_{GS}= \pm 12\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS}= -16\text{V}$, $V_{GS}=0$
		-	-	-10		$V_{DS}= -16\text{V}$, $V_{GS}=0$, $T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-3	-	-	A	$V_{DS}= -5\text{V}$, $V_{GS}= -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	130	m Ω	$V_{GS}= -4.5\text{V}$, $I_D= -2.5\text{A}$
		-	-	190		$V_{GS}= -2.5\text{V}$, $I_D= -1.9\text{A}$
Forward Transconductance ¹	g_{fs}	-	3	-	S	$V_{DS}= -5\text{V}$, $I_D= -2.5\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.7	-	V	$I_S= -1.6\text{A}$, $V_{GS}=0$
Dynamic ²						
Total Gate Charge	Q_g	-	12.2	-	nC	$V_{DS}= -5\text{V}$, $V_{GS}= -4.5\text{V}$, $I_D= -2.5\text{A}$
Gate-Source Charge	Q_{gs}	-	1.1	-		
Gate-Drain Charge	Q_{gd}	-	1.5	-		
Turn-on Delay Time	$T_{d(on)}$	-	6.5	-	nS	$V_{DD}= -5\text{V}$, $V_{GEN}= -4.5\text{V}$, $R_L=5\Omega$, $R_G=6\Omega$
Rise Time	T_r	-	20	-		
Turn-off Delay Time	$T_{d(off)}$	-	31	-		
Fall Time	T_f	-	21	-		

Notes:

1. Pulse test: $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.