

## GaAs Broadband High Power SP3T Switch DC - 4.0 GHz

Rev. V1

### Features

- CDMA Handset Switching Applications
- Balanced (symmetrical) RF Ports
- Low Cross Modulation
- Low Insertion Loss: 0.55 dB @ 1 GHz
- High Isolation: 27 dB @ 1 GHz
- High Power: P0.1dB = 36 dBm @ 1 GHz
- 0.5 micron GaAs pHEMT Process
- Lead-Free 2 mm 12-Lead STQFN with 0.4 mm lead pitch package
- Halogen-Free "Green" Mold Compound
- RoHS\* Compliant and 260°C Reflow Compatible

### Description

M/A-COM's MASW-009359 is an industry leading GaAs PHEMT MMIC single pole three throw (SP3T) CDMA-GPS switch in a lead-free 2 mm 12-lead STQFN package with 0.4 mm lead pitch. The MASW-009359 is uniquely configured to enable switching from a common antenna port to CDMA cellular, CDMA PCS, or GPS ports. It is also ideal for other applications where a compact, high performance, symmetrical SP3T switch is required.

The design is symmetric and has been fully optimized for excellent cross modulation performance in all three paths while still maintaining excellent insertion loss and isolation. The symmetrical design allows the user to assign CDMA cellular, CDMA PCS and GPS to ports RF1, RF2 or RF3 to optimize the layout.

The MASW-009359 is fabricated using a 0.5 micron gate length GaAs pHEMT process. The process features full passivation for performance and reliability.

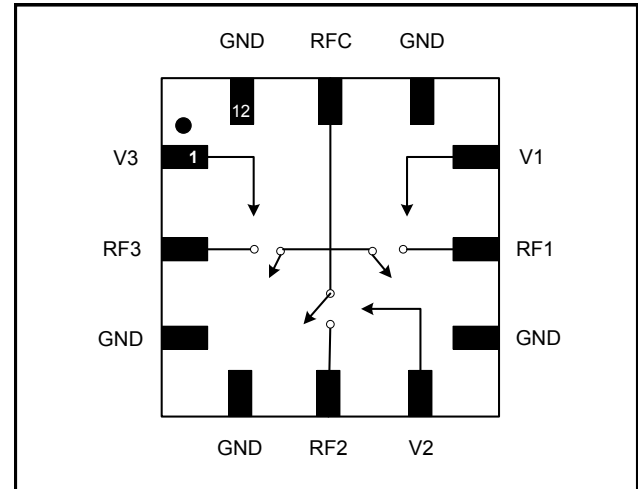
### Ordering Information<sup>1,2</sup>

Part Number	Package
MASW-009359-TR3000	3000 piece reel
MASW-009359-001SMB	Sample Board 0.05 - 4.0 GHz Tuning

1. Reference Application Note M513 for reel size information.
2. All sample boards include 5 loose parts.

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

### Functional Schematic



### Pin Configuration<sup>3</sup>

Pin No.	Function	Description
1	V3	Control 3
2	RF3	RF Port 3
3	GND	Ground
4	GND	Ground
5	RF2	RF Port 2
6	V2	Control 2
7	GND	Ground
8	RF1	RF Port 1
9	V1	Control 1
10	GND	Ground
11	RFC	RF Common
12	GND	Ground
13	GND (paddle)	Ground

3. All package ground pins (P3,4,7,10, 12) and paddle ground are no connection (N/C) electrically to the internal die. M/A-COM recommends connecting all ground path connections to PCB ground to ensure a good thermal path.

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**Electrical Specifications:  $T_A = 25^\circ\text{C}$ ,  $Z_0 = 50 \Omega$ ,  $V_C = 0 \text{ V} / 2.7 \text{ V}$ , 1000 pF Capacitors <sup>4</sup>**

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss (All Paths)	1.0 GHz	dB	—	0.55	0.7
	2.0 GHz	dB	—	0.75	0.9
	2.5 GHz	dB	—	0.75	0.9
Isolation	1.0 GHz	dB	23	27	—
	2.0 GHz	dB	17	21	—
	2.5 GHz	dB	16	20	—
Return Loss (All RF ports)	DC - 2.5 GHz	dB	—	20	—
IP3	Two Tone, +23 dBm/tone, 5 MHz Spacing, 1 GHz	dBm	—	65	—
	Two Tone, +23 dBm/tone, 5 MHz Spacing, 2 GHz	dBm	—	64	—
Cross Modulation	For Cell Band: Two-tone signal input: $T_{X1} = +22 \text{ dBm @ } 820 \text{ MHz}$ , $T_{X2} = +22 \text{ dBm @ } 821 \text{ MHz}$ , $R_X \text{ interferer} = -23 \text{ dBm @ } 865 \text{ MHz}^5$	dBm	—	-108	—
	For PCS Band: Two-tone signal input: $T_{X1} = +18 \text{ dBm @ } 1880 \text{ MHz}$ , $T_{X2} = +18 \text{ dBm @ } 1881 \text{ MHz}$ , $R_X \text{ interferer} = -23 \text{ dBm @ } 1960 \text{ MHz}^5$	dBm	—	-109	—
2 <sup>nd</sup> Harmonic	$F_{in} = 1 \text{ GHz}$ , $P_{in} = +26 \text{ dBm}$	dBc	—	82	—
	$F_{in} = 2 \text{ GHz}$ , $P_{in} = +26 \text{ dBm}$		—	83	—
3 <sup>rd</sup> Harmonic	$F_{in} = 1 \text{ GHz}$ , $P_{in} = +26 \text{ dBm}$	dBc	—	84	—
	$F_{in} = 2 \text{ GHz}$ , $P_{in} = +26 \text{ dBm}$		—	74	—
P0.1dB	$V_C = 0 \text{ V}/2.7 \text{ V}$ , 1 GHz	dBm	—	36	—
Trise, Tfall	10% to 90% RF, 90% to 10% RF, 900 MHz	ns	—	45	—
Ton, Toff	50% control to 90% RF, and 50% control to 10% RF, 900 MHz	ns	—	70	—
Transients	In Band	mV	—	40	—
Control Current	$V_C = 0 \text{ V}/2.7 \text{ V}$	$\mu\text{A}$	—	6	25

4. External DC blocking capacitors are required on all RF ports. Typical performance specifications are with 1000 pF blocking and decoupling capacitors / as shown on the application schematic.

5.  $R_X$  Interferer power set to  $-10 \text{ dBm}$  during test to improve dynamic range of measurement system. Typical performance with  $-23 \text{ dBm}$  interferer is determined by using a linear relationship between interferer power level and cross modulation products.

### Absolute Maximum Ratings <sup>6,7</sup>

Parameter	Absolute Maximum
Input Power (0.5 - 4.0 GHz, 2.6 V Control)	+36 dBm
Control Voltage	$\pm 8.5 \text{ volts}$
Operating Temperature	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Storage Temperature	$-65^\circ\text{C}$ to $+150^\circ\text{C}$

6. Exceeding any one or combination of these limits may cause permanent damage to this device.

7. M/A-COM does not recommend sustained operation near these survivability limits.

### Truth Table <sup>8,9</sup>

V1	V2	V3	ANT-RF1	ANT-RF2	ANT-RF3
1	0	0	On	Off	Off
0	1	0	Off	On	Off
0	0	1	Off	Off	On

8. Differential voltage, V (state 1) -V (state 0) must be 2.6 V minimum and must not exceed 8.5 V.

9. Positive Control: 1 = +2.6 V to +8.0 V, 0 = 0 V +/- 0.2V  
Negative Control: 1 = 0 V +/- 0.2V, 0 = -2.6 V to -8.0 V

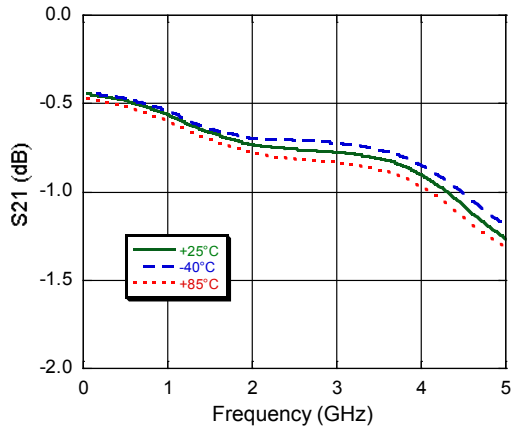
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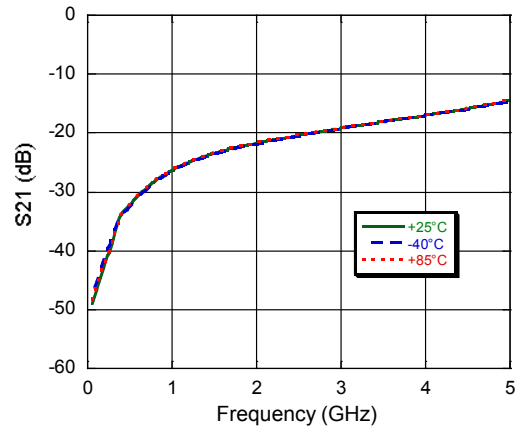
### Typical Performance Curves:

$Z_0 = 50 \Omega$ , 1000 pF Blocking and decoupling caps,  $V_{CTL} = 0/+2.7$  Vdc

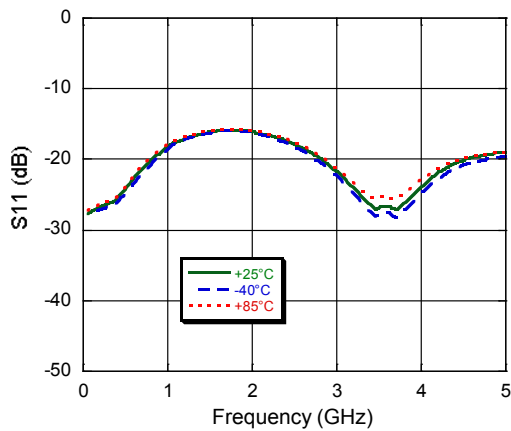
**Insertion Loss**



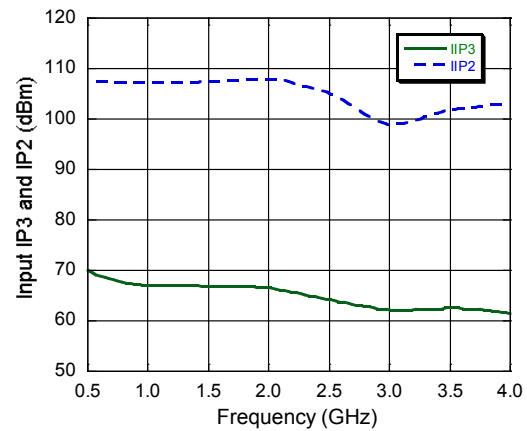
**Isolation**



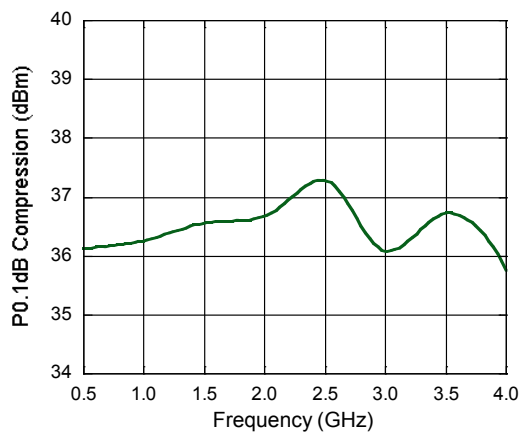
**Input Return Loss**



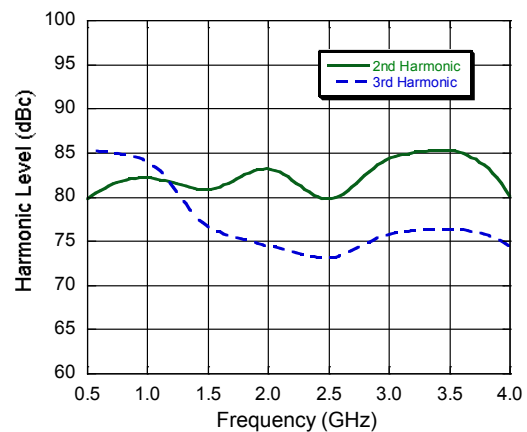
**Input IP2 and IP3**



**Input P0.1dB Compression**



**Harmonics**

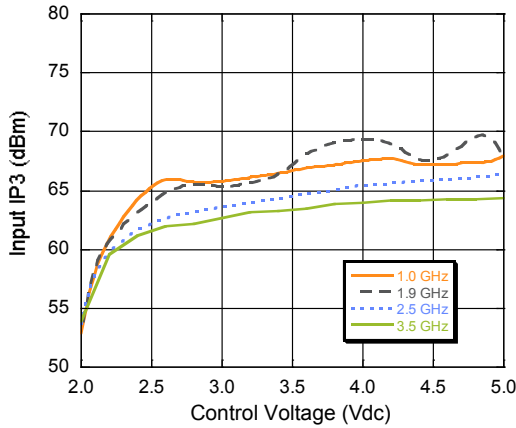


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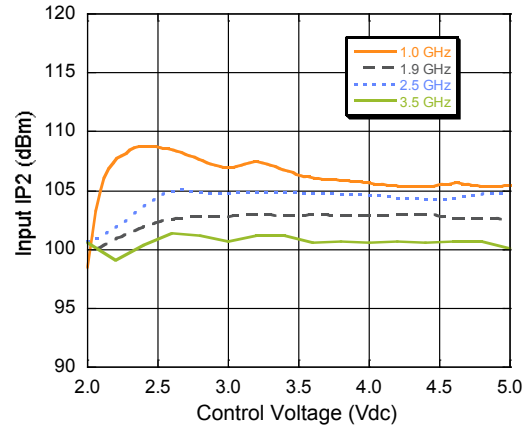
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Typical Performance Curves vs. Control Voltage:  
 $Z_0 = 50 \Omega$ , 1000 pF Blocking and decoupling caps

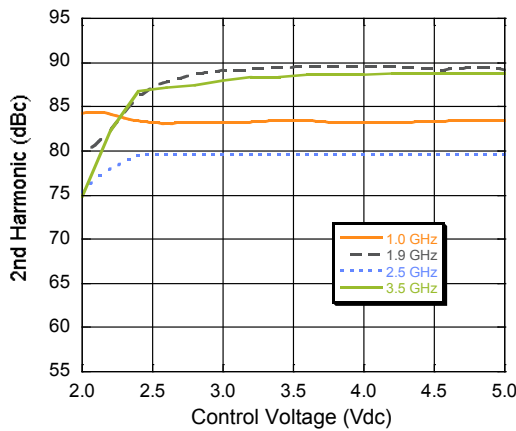
Input IP3 vs. Control Voltage



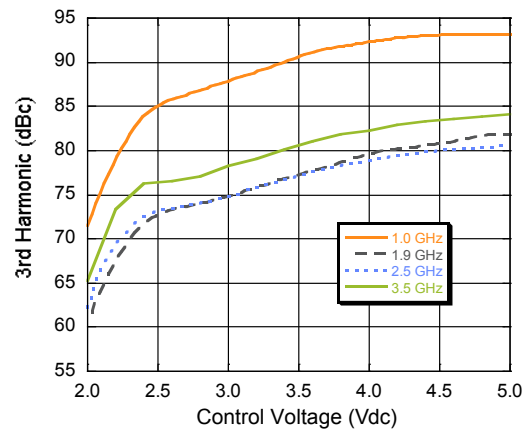
Input IP2 vs. Control Voltage



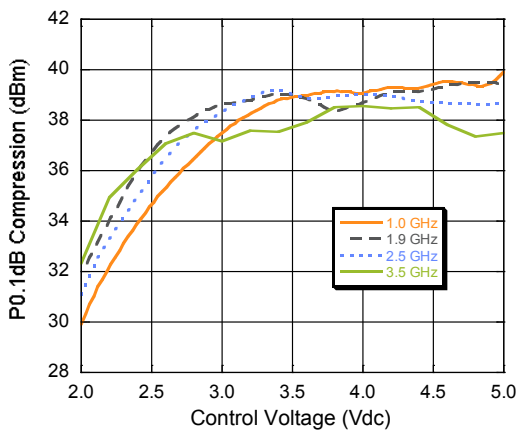
2nd Harmonic vs. Control Voltage



3rd Harmonic vs. Control Voltage



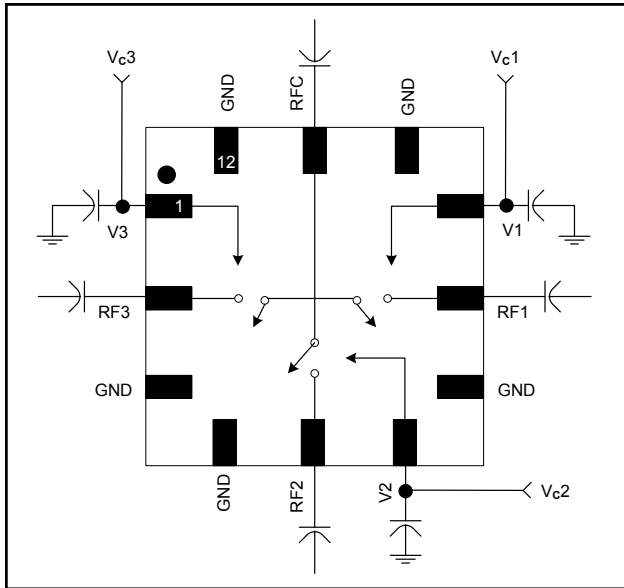
Input P0.1dB vs. Control Voltage



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### Application Schematic <sup>10,11</sup>



- 10. The exposed pad centered on the package bottom must be connected to ground to ensure a good thermal path.
- 11. All blocking and decoupling capacitors = 1000 pF

### Qualification

Qualified to M/A-COM specification REL-201, Process Flow -2.

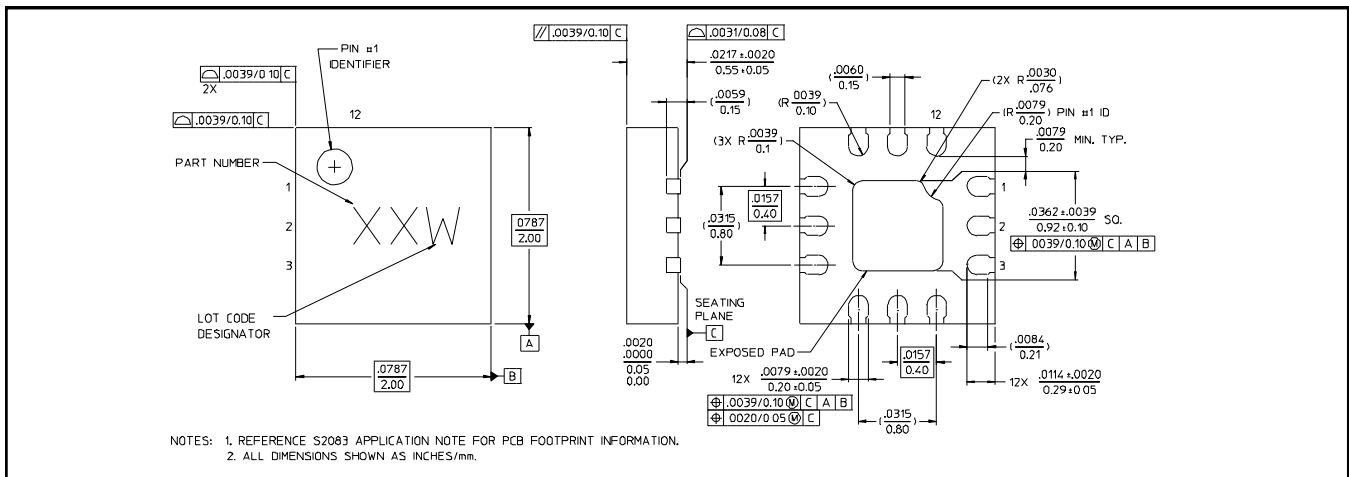
### Handling Procedures

Please observe the following precautions to avoid damage:

### Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

### Lead-Free 2 mm STQFN-12LD-0.4mm Pitch<sup>†</sup>



- <sup>†</sup> Reference Application Note S2083 for lead-free solder reflow recommendations.
- Meets JEDEC moisture sensitivity level 1 requirements.
- Plating is Ni/Pd/Au over Copper.

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