TPS43340-Q1 低 I_Q、30μA、高 V_{IN} 四路输出电源

1 特性

- 适用于汽车电子 应用
- 具有下列结果的 AEC-Q100 测试指南：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 H1
  - 器件组件充电模式 (CDM) ESD 分类等级 C3B
- 输入电压范围最高达 40V（瞬态电压高达 60V)
- 输入电压范围：4V 至 40V
  - 瞬态电压高达 60V
- 双输入同步降压控制器
  - 峰值栅极驱动电流为 0.6A
  - 自动低功率模式运行
  - 低功耗模式 I_Q：30μA（一个降压转换器工作），35μA（两个降压转换器工作）
- 低关断电流，I_{sh} = 5μA（典型值）
- 单一同步降压调节器转换器 BUCK3
  - 最大输出电流 2A
- 线性稳压器 LREG1
- 独立的使能输入（EN1、EN2、EN3、EN4）
- 内部振荡器，可借助外部电阻器进行编程，150kHz 至 600kHz 的开关频率$f_{SW_BUCK1，2，3}$
- 集成锁相环路 (PLL)，外部同步频率：150kHz 至 600kHz
- 以 180° 相移运行的开关模式稳压器
- 用于所有输出电源轨的复位输出
- 电源和过压检测及关断
- 耐热增强型 PowerPAD™封装
  - 48 引脚带散热片方形扁平封装 (HTQFP) (PHP)

2 应用

- 汽车信息娱乐系统、主机、导航、音频和仪表板
- 高级驾驶员辅助系统 (ADAS)
- 汽车和工业多轨直流配电系统

3 说明

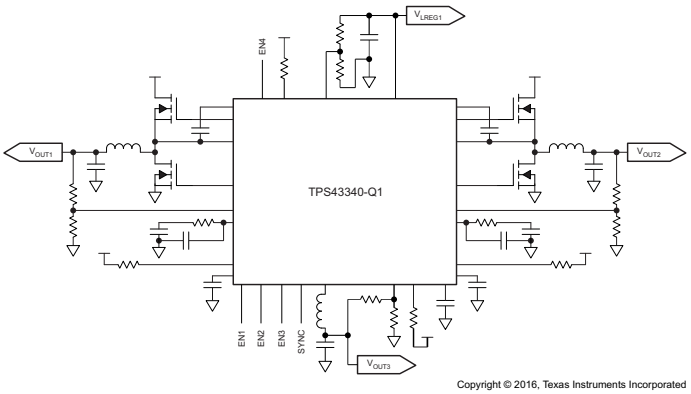
TPS43340-Q1 是一款四路轨电源，特有两个栅极驱动电流为 0.6A 的同步降压控制器、一个同步 2A 降压转换器以及一个具有低静态电流的 300mA LDO。该器件专为包括 MCU 和 DSP（分别直接通过汽车电池供电）在内的整个系统供电，输入电压最高为 40V。该器件 在 降压稳压器控制器的栅极驱动输出上集成了短路和过流保护功能，并且可在稳压器输出接地短路时单独为每个降压稳压器电源施加电流折返控制。每个输出电源包含一个软启动以确保最初加电时这些经稳压的输出不受电流限制的影响。加电时执行的复位延迟使得 Buck1，Buck2，Buck3 和线性稳压器的输出达到稳定调节。一个外部电容器将延迟设定为 300ms 的最大范围。每个电源输出具有可根据外部电阻器网络设置进行调节的输出电压。根据使能和禁用控制或者软启动，此器件可在输出电源轨加电和断电期间进行排序控制。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS43340-Q1	HTQFP (48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



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目录

1 特性 1
2 应用 1
3 说明 1
4 修订历史记录 2
5 Pin Configuration and Functions 4
6 Specifications 7
6.1 Absolute Maximum Ratings 7
6.2 ESD Ratings 8
6.3 Recommended Operating Conditions 8
6.4 Thermal Information 9
6.5 Electrical Characteristics 9
6.6 Typical Characteristics 13
7 Detailed Description 16
7.1 Overview 16
7.2 Functional Block Diagram 16
7.3 Feature Description 16
7.4 Device Functional Modes 20
8 Application and Implementation 26
8.1 Application Information 26
8.2 Typical Application 27
9 Power Supply Recommendations 32
10 Layout 32
10.1 Layout Guidelines 32
10.2 Layout Example 33
10.3 Power Dissipation 33
10.4 Thermal Considerations 35
11 器件和文档支持 37
11.1 器件支持 37
11.2 文档支持 37
11.3 社区资源 37
11.4 商标 37
11.5 静电放电警告 37
11.6 Glossary 37
12 机械、封装和可订购信息 37

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (July 2015) to Revision E — **Page**

- Update the HBM ESD ratings and added the MM ESD rating back in the *ESD Ratings* table 8

Changes from Revision C (January 2013) to Revision D — **Page**

- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1

Changes from Revision B (April 2012) to Revision C — **Page**

- 已添加特性要点至 特性 列表顶部 1
- 已将缺失的“-Q1”添加至部件编号中 1
- 修改了首页电路原理图 1
- Added a sentence to the EXTSUP pin description 5
- Changed "converter" to "controller" for pin SS2 6
- Deleted thermal characteristics from Recommended Operating Characteistics table 8
- Added the Thermal Information table 9
- Multiple changes throughout *Electrical Characteristics* table 9
- Appended missing "-Q1" to part number 16
- Changed the recommended capacitor value 17
- Added a sentence to the second paragraph of the Gate-Driver Supply section 17
- Added new sentence to Gate-Driver Supply section 17
- Replaced the two paragraphs following 图 14 with three new paragraphs 17
- Modified 公式 2 20
- Changed $f_{SW\text{-}Trans\text{-}delay}$ to $t_{SW\text{-}Trans\text{-}delay}$ 20
- Modified 公式 3 20
- Renamed VBUCKx to V_{OUTx} 20

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- Added (Farads) to 公式 4 20
- Changed "resistor" to "V_{OUT3}" 20
- Revised 图 17 23
- Changed "VBAT" to "V_{IN}" 24
- Modified power-dissipation equations 28
- Buck2 Component Selection, modified 公式 22, 公式 25, 公式 26, and 公式 29, 公式 31 29
- Added 公式 27, 公式 28, 公式 30, and 公式 32 29
- Buck3 Component Selection, modified 公式 34, 公式 36, 公式 37, and 公式 38, ... 30
- Added 公式 39, 公式 40, 公式 41, and 公式 43 30
- Modified several equations in Summary of Equations table 34

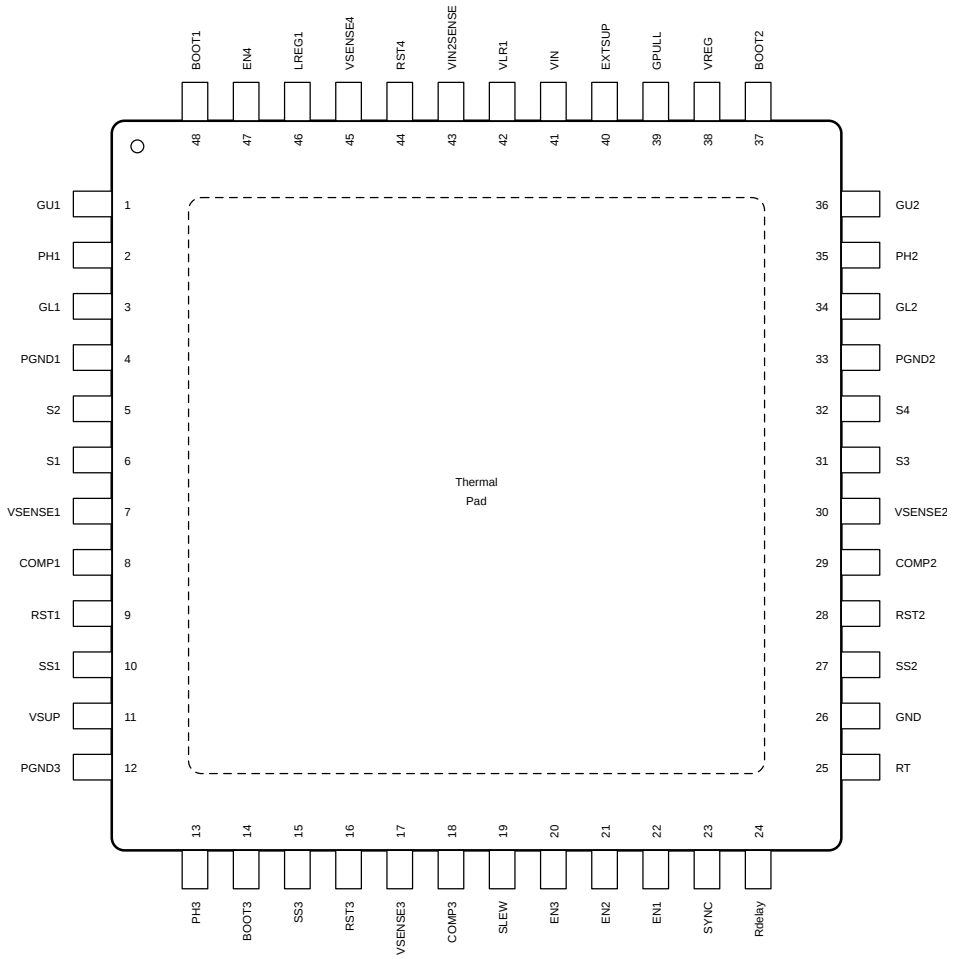
Changes from Revision A (January 2012) to Revision B **Page**

- Changed Feedback input to Supply sense input in Abs Max Ratings table 7
- Inserted Input voltage for Buck 2 information in the Recommended Operating Conditions table 8
- Added VIN2SENSE = 4 V to 40 V in *Electrical Characteristics* table header. 9
- Changed I_{q_LPM} to I_q, changed LPM quiescent current to Quiescent current, and changed the conditions for EN in the Electrical Characteristics table. 9

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5 Pin Configuration and Functions

PHP Package
48-Pin HTQFP With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT1	48	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck converter Buck1. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
BOOT2	37	I	A capacitor on this pin acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck converter Buck2. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
BOOT3	14	I	A capacitor between BOOT3 and PH3 acts as the voltage supply for the high-side N-channel MOSFET gate-drive circuitry in buck converter Buck3. When the buck is in a dropout condition, the device automatically reduces the duty cycle of the high-side MOSFET to approximately 95% on every fourth cycle to allow the capacitor to recharge.
COMP1	8	O	Error amplifier output of Buck1 and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the respective inductor. Clamping this voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.
COMP2	29	O	Error amplifier output of Buck2 and compensation node for voltage-loop stability. The voltage at this node sets the target for the peak current through the respective inductor. Clamping this voltage on the upper and lower ends provides current-limit protection for the external MOSFETs.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP3	18	O	Error amplifier output of Buck3 and compensation node for voltage loop stability. The voltage at this node sets the target for the peak current through the respective inductor.
EN1	22	I	Enable input for Buck1. This input has an internal pullup with approximately 0.5 µA of current.
EN2	21	I	Enable input for Buck2. This input has an internal pullup with approximately 0.5 µA of current.
EN3	20	I	Enable input for Buck3. This input has an internal pullup with approximately 0.5 µA of current.
EN4	47	I	Enable input for LREG1 (active-high with an internal pullup current source). An input voltage higher than V_{IH} enables the regulator, whereas an input voltage lower than V_{IL} disables the regulator. This input has an internal pullup with approximately 0.5 µA of current.
EXTSUP	40	I	One can use EXTSUP to supply the VREG regulator from one of the TPS43340-Q1 buck regulator rails to reduce power dissipation in cases where there is an expectation of high VIN. When EXTSUP is open or lower than 4.6 V, VIN powers the regulator. If EXTSUP is unused, leave the pin open without a capacitor installed.
GL1	3	O	External low-side N-channel MOSFET gate drive for buck regulator Buck1. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GL2	34	O	External low-side N-channel MOSFET for buck regulator This output can drive Buck2. The output provides high peak currents to drive capacitive loads. VREG provides the voltage swing on this pin.
GND	26	O	Analog ground reference
GPULL	39	O	Gate-driver output to implement the reverse-battery protection by an external PMOS. See the *Application Information* section for more details.
GU1	1	O	External high-side N-channel MOSFET gate drive for buck regulator Buck1. The output provides high peak currents to drive capacitive loads. The gate-drive reference is a floating-ground reference provided by PH1 and has a voltage swing provided by BOOT1.
GU2	36	O	This output can drive an external high-side N-channel MOSFET for buck regulator Buck2. The output provides high peak currents to drive capacitive loads. The gate-drive reference is a floating-ground reference provided by PH2 and has a voltage swing provided by BOOT2.
LREG1	46	O	Linear regulator output. Decouple with a low-ESR ceramic output capacitor in the range of 1 µF to 47 µF connected from this terminal to ground.
PGND1	4	O	Power ground connection for the GL1 driver. Connect to the source of the low-side N-channel MOSFET of Buck1.
PGND2	33	O	Power ground connection to the source of the low-side N-channel MOSFETs of Buck2
PGND3	12	O	Buck3 power ground
PH1	2	O	Switching terminal of buck regulator Buck1, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desirable.
PH2	35	O	Switching terminal of buck regulator Buck2, providing a floating ground reference for the high-side MOSFET gate-driver circuitry and used to sense current reversal in the inductor when discontinuous-mode operation is desirable.
PH3	13	O	Switching terminal of buck converter Buck3. Also provides a floating ground reference for the high-side MOSFET gate-driver circuitry
Rdelay	24	O	The capacitor at the Rdelay pin sets the power-good delay interval used to de-glitch the outputs of the power-good comparators. Leaving this pin open sets the power-good delay to an internal default value of 20 µs, typical.
RST1	9	O	Open-drain power-good output for Buck1, with a 50-kΩ pullup resistor to S2. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ of the set value.
RST2	28	O	Open-drain power-good output for Buck2 with a 50 kΩ pullup resistor to S4. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ of the set value.
RST3	16	O	Open-drain power-good output for Buck3. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ of the set value.
RST4	44	O	Open-drain power-good indicator pin for LREG1, with a 50-kΩ pullup resistor to LREG1. An internal power-good comparator monitors the voltage at the feedback pin and pulls this output low when the output voltage falls by $RSTx_{th1}$ of the set value.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
RT	25	O	Connecting a resistor to analog ground on this pin sets the operating switching frequency of the buck controllers and converter. Shorting this pin to ground or leaving it open defaults operation to 400 kHz for the buck controllers and the converter.
S1	6	I	High-impedance differential-voltage inputs from the current-sense element (sense resistor or inductor DCR) for the buck controller. For details, see the *Functional Description* section.
S2	5	I	
S3	31	I	
S4	32	I	
SLEW	19	I	Slew rate (dV/dt) selector of the internal high-side switching MOSFET for Buck3. For details, see the *Application Information* section.
SS1	10	O	Soft-start or tracking input for buck controller Buck1. The buck controller regulates the VSENSE1 voltage to the lower of 0.8 V or the SS1 pin voltage. An internal pullup current source of 1 μA is present at the pin, and use of an appropriate capacitor connected here can set the soft-start ramp duration. Alternatively, use of a resistor divider from another supply can provide a tracking input to this pin.
SS2	27	O	Soft-start or tracking input for buck controller Buck2. The buck controller regulates the VSENSE2 voltage to the lower of 0.8 V or the SS2 pin voltage. An internal pullup current source of 1 μA is present at the pin, and use of an appropriate capacitor connected here can set the soft-start ramp interval. Alternatively, use of a resistor divider from another supply can provide a tracking input to this pin.
SS3	15	O	Soft-start or tracking input for buck converter Buck3. The buck converter regulates the VSENSE3 voltage to the lower of 0.8 V or the SS3 pin voltage. An internal pullup current source of 1 μA is present at the pin, and an appropriate capacitor connected here can set the soft-start ramp duration. Alternatively, use of a resistor divider from another supply can provide a tracking input to this pin.
SYNC	23	I	PLL synchronization, low-power mode-control pin. If an external clock is present on this pin, the device detects it and the internal PLL locks on to the external clock. This overrides the internal oscillator frequency. The device can synchronize to frequencies from 150 kHz to 600 kHz. For details, see the *Application Information* section.
VIN	41	I	Main Input pin. This is the buck controller and buck converter input pin. Additionally, it powers the internal control circuits of the device. Connect a bypass capacitor to filter noise between this pin and signal ground.
VIN2SENSE	43	I	Supply-voltage sense input for the current mode of Buck2. Connect to the drain of the high-side-FET of Buck2. Cascading Buck1 as the supply for the Buck2 configuration does not support LPM on Buck2.
VLR1	42	I	The VLR1 terminal is the input voltage source for the linear regulator supply. This pin requires an input capacitor to ground to filter any noise present on the line.
VREG	38	O	This pin requires an external capacitor to provide a regulated supply for the gate drivers of the buck controllers and converter. The regulator can obtain power either from VIN or EXTSUP. This pin has current limit-protection; do not use it to drive any other loads.
VSENSE1	7	I	Feedback voltage pin for Buck1. For details, see the *Application Information* section.
VSENSE2	30	I	Feedback voltage pin for Buck2. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
VSENSE3	17	I	Feedback voltage pin for Buck3. The buck controller regulates the feedback voltage to the internal reference of 0.8 V. A suitable resistor divider network between the buck output and the feedback pin sets the desired output voltage.
VSENSE4	45	I	Feedback voltage pin for linear regulator LREG1. LREG1 regulates the feedback voltage to the internal reference. A suitable resistor divider network between the LDO output and the feedback pin sets the desired output voltage. See the LREG1 parameters and the *Application Information* section.
VSUP	11	I	Power supply for the Buck3 regulator. Provide good decoupling to PGND3 with a ceramic capacitor close to the pins.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply inputs	Input voltage	VIN	–0.3	60	V
Buck controller Buck1 and Buck2	Enable inputs	EN1, EN2	–0.3	60	V
	Bootstrap supplies	BOOT1, BOOT2	–0.3	68	V
	Bootstrap supplies	BOOT1-PH1, BOOT2-PH2, BOOT3-PH3	–0.3	8.8	V
	Phase inputs	PH1, PH2	–1	60	V
		PH1, PH2 (for 100 ns)	–2		V
	Feedback inputs	VSENSE1, VSENSE2	–0.3	13	V
	Error-amplifier outputs	COMP1, COMP2	–0.3	13	V
	Peak output currents from external MOSFET driver	GU1,GU2, GL1,GL2		1	A
	External MOSFET driver	GL1-PGND1,GL2-PGND2	–0.3	8.8	V
		GU1-PH1,GU2-PH2	–0.3	8.8	
	Current-sense voltage	S1, S2, S3, S4	–0.3	13	V
	Absolute differential voltage	|S1 – S2|, |S3 – S4|		2	V
	Soft start	SS1, SS2	–0.3	13	V
	Power-good outputs	RST1, RST2	–0.3	13	V
	Switching-frequency oscillator	RT	–0.3	13	V
	External input clock	SYNC	–0.3	13	V
	External input supply for gate drive	EXTSUP	–0.3	13	V
Buck converter Buck3	Input supply	VSUP	–0.3	13	V
	Slew-rate setting	SLEW	–0.3	13	
	Enable input	EN3	–0.3	13	
	Bootstrap supply	BOOT3	–1	20	
	Phase inputs	PH3	–1	13	
		PH3 (for 100 ns)	–2		
	Feedback input	VSENSE3	–0.3	13	
	Soft start	SS3	–0.3	13	
	Power-good output	RST3	–0.3	13	
	Error-amplifier output	COMP3	–0.3	13	
Linear regulator LREG1	Input voltage	VLR1	–0.3	60	V
	Output voltage	LREG1	–0.3	7	
	Enable input	EN4	–0.3	60	
	Power-good output	RST4	–0.3	8.8	
	Feedback inputs	VSENSE4	–0.3	13	
GPULL, Rdelay, VREG, VIN2SENSE	PMOS driver	GPULL	–0.3	60	V
	Zener clamp current	GPULL		0.2	mA
	Internal regulator	VREG	–0.3	8.8	V
	Reset delay	Rdelay	–0.3	8.8	V
	Supply sense input	VIN2SENSE	–0.3	60	V
Temperature	Junction temperature: T_J		–40	150	°C
	Operating temperature: T_A		–40	125	
	Storage temperature: T_{STG}		–55	165	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	All pins except VLR1	±2000	V
			VLR1	±1000	
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)	±750	
			Other pins	±500	
		Machine model (MM)	All pins except RSTx	±200	
			RSTx	±100	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply inputs	Input voltage	VIN	4		40	V
	Input voltage for Buck 2	VIN2SENSE	4		40	V
Buck controller Buck1 and Buck2	Enable inputs	EN1, EN2	0		40	V
	Bootstrap inputs	BOOT1, BOOT2	4		48	V
	Phase inputs	PH1, PH2	–0.6		40	V
		PH1, PH2 (for 50 ns)	–2			V
	Feedback inputs	VSENSE1, VSENSE2	0		6	V
	Error-amplifier outputs	COMP1, COMP2	0		6	V
	Peak output currents from external MOSFET driver	GU1,GU2, GL1,GL2			0.75	A
	Current-sense voltage	S1, S2, S3, S4	0		11	V
	Soft start	SS1, SS2	0		6	V
	Power-good outputs	RST1, RST2	0		11	V
	Switching-frequency setting	RT	0		1.2	V
	External input clock	SYNC	0		9	V
	External input supply for gate drive	EXTSUP	0		9	V
Buck converter Buck3	Input supply	VSUP	4		10	V
	Slew-rate setting	SLEW	0		V_{REG}	
	Enable input	EN3	0		6	
	Boot inputs	BOOT3	0		18	
	Phase inputs	PH3	–1		11	
		PH3 (for 50 ns)	–2			
	Feedback input	VSENSE3	0		6	
	Soft start	SS3	0		6	
	Power-good output	RST3	0		11	
	Error-amplifier output	COMP3	0		6	
Linear regulator LREG1	Input voltage	VLR1	4		40	V
	Output voltage	LREG1	0.8		5.25	
	Enable input	EN4	0		40	
	Power-good output	RST4	0		5.25	
	Feedback inputs	VSENSE4	0		6	
PMOS driver	PMOS driver	GPULL	4		40	V
	Internal regulator	VREG	0		6	
Temperature ratings	Operating temperature, T_A		–40		125	°C

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6.4 Thermal Information

THERMAL METRIC(1)		TPS43340-Q1 PHP (HTQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

$V_{IN} = V_{LR1}$ = 8 V to 18 V, V_{SUP} = 4 V to 10 V, $V_{IN2SENSE}$ = 4 V to 40 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT SUPPLY							
V_{IN}	Input voltage required for device on initial start-up			6.5		40	V
	Operating range after initial start-up			4			V
$V_{IN\ UV}$	Undervoltage lockout	V_{IN} falling. After a reset, initial start-up conditions may apply.(1)		3.5	3.6	3.8	V
		V_{IN} rising. After a reset, initial start-up conditions may apply.(1)			3.8	4	V
V_{LR1}	Device operating range for linear regulator			4		40	V
I_Q	Quiescent current	T_A = 25°C	EN1 = 1, LPM; EN2,3,4 = 0		30	40	µA
			EN2 = 1, LPM; EN1,3,4 = 0		30	40	
			EN4 = 1, LPM; EN1,2,3 = 0		48	60	
			EN1,2 = 1, LPM; EN3,4 = 0		35	45	
			EN3,4 = 1, EN1,2 = 0		4	4.5	mA
		T_A = 125°C	EN1 = 1, LPM; EN2,3,4 = 0		40	50	µA
			EN2 = 1, LPM; EN1,3,4 = 0		40	50	
			EN4 = 1, LPM; EN1,2,3 = 0		52	60	
			EN1,2 = 1, LPM; EN3,4 = 0		40	45	
			EN3,4 = 1, EN1,2 = 0		5		mA
I_{VIN}	Quiescent current	T_A = 25°C	V_{IN} = 13 V, Buck1: CCM, Buck2: off, or V_{IN} = 13 V, Buck2: CCM, Buck1: off, or V_{IN} = 13 V, Buck1 and Buck2: CCM		5		mA
		T_A = 125°C	Normal operation, SYNC = 5 V		5		mA
			V_{IN} = 13 V, Buck1: CCM, Buck2: off		5		
			V_{IN} = 13 V, Buck2: CCM, Buck1: off		5		
			V_{IN} = 13 V, Buck1, 2: CCM		7		
I_{VIN-SD}	Shutdown current at T_A = 25°C	EN1,2,3,4 = 0: off, $V_{IN} = V_{LR1}$ = 13 V			5	10	µA
I_{VIN-SD}	Shutdown current at T_A = 125°C	EN1,2,3,4 = 0: off, $V_{IN} = V_{LR1}$ = 13 V				20	µA
$I_{VLRI-SD}$	Shutdown current at T_A = 125°C	EN1,2,3,4 = 0: off, $V_{IN} = V_{LR1}$ = 13 V				5	µA
INTERNAL SUPPLY VREG							
V_{REG}	Internal regulated supply	V_{IN} = 8 V to 18 V, EXTSUP = 0 V, SYNC = High		5.5.	5.8	6.1	V
	Load regulation	EXTSUP = 0 V, SYNC = High I_{VREG} = 0 mA to 100 mA			0.2%	1%	
$V_{REG-EXTSUP}$	Internal regulated supply	EXTSUP = 8.5 V		7.2.	7.5	7.8	V
	Load regulation	EXTSUP = 8.5 V to 13 V, I_{VREG} = 0 mA to 125 mA, SYNC = High			0.2%	1%	
$V_{EXTSUP-VREG}$	EXTSUP switch-over voltage	I_{VREG} = 0 mA to 100 mA, EXTSUP ramping positive		4.4	4.6	4.8	V

(1) If V_{BAT} and V_{REG} remain adequate, the buck can continue to operate if V_{IN} is > 3.8 V

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Electrical Characteristics (接下页)

V_{IN} = V_{LR1} = 8 V to 18 V, V_{SUP} = 4 V to 10 V, $V_{IN2SENSE}$ = 4 V to 40 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{EXTSUP-HYS}$	EXTSUP switch-over hysteresis		150		250	mV
$I_{REG-LIM}$	Current limit on VREG	EXTSUP = 0 V normal mode as well as LPM	100		400	mA
$I_{REG-EXTSUP-LIM}$	Current limit on VREG when using EXTSUP	I_{VREG} = 0 mA to 100 mA, EXTSUP = 8.5 V, SYNC = High	125		400	mA
INPUT VOLTAGE VIN - OVERVOLTAGE LOCK OUT AND REVERSE POLARITY PROTECTION						
V_{OVLO}	Overvoltage shutdown	VIN rising	45	46	47	V
		VIN falling	43	44	45	V
$OVLO_{Hys}$	Hysteresis		1	2	3	V
$OVLO_{filter}$	Filter time			5		µs
V_{GD}	Clamping voltage of ext. FET	VIN - GPULL		17		V
R_{GPULL}	Internal resistance to GND			500		kΩ
BUCK CONTROLLERS						
V_{OUT1}, V_{OUT2}	Adjustable output voltage range		0.9		11	V
V_{REF}	Internal reference voltage and tolerance in normal mode	Measure VSENSEx pin	0.792	0.8	0.808	V
			–1%		1%	
$V_{REF, LPM}$	Internal reference voltage and tolerance in low-power mode	Measure VSENSEx pin	0.784	0.8	0.816	V
			–2%		2%	
V_{SENSE}	V_{SENSE} for forward-current limit in CCM	VSENSEx = 0.75 V, duty cycles < 10%	60	75	90	mV
	V_{SENSE} for reverse-current limit in CCM	VSENSEx = 1 V	–65	–37.5	–23	mV
$V_{I-Foldback}$	V_{SENSE} for output short	VSENSEx = 0 V (foldback)	17	43.8	48	mV
t_{dead}	Shoot through delay, blanking time			20		ns
DC_{NRM}	High-side minimum on-time			100		ns
	Maximum duty cycle (digitally controlled)			98.75%		
DC_{LPM}	Duty cycle LPM				80%	
I_{LPM_Entry}	LPM entry threshold load current as fraction of maximum set load current			1%		
V_{LPM_Exit}	LPM exit threshold load current as fraction of maximum set load current			10%		
HIGH-SIDE EXTERNAL NMOS GATE DRIVERS FOR BUCK CONTROLLERS						
I_{GUx_peak}	Gate driver peak current			0.6		A
$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8 V, I_{GUx} current = 200 mA		5		Ω
LOW-SIDE NMOS GATE DRIVERS FOR BUCK CONTROLLERS						
I_{GLx_peak}	Gate driver peak current			0.6		A
$r_{DS(on)}$	Source and sink driver	V_{REG} = 5.8V, I_{GLx} current = 200 mA		5		Ω
INTERNAL OSCILLATOR (RT)						
f_{SW}	Buck switching frequency	RT pin: GND	360	400	440	kHz
f_{SW}	Buck switching frequency	RT pin: 60 kΩ external resistor	360	400	440	kHz
f_{SW-adj}	Buck adjustable range with external resistor	RT pin: external resistor	150		600	kHz
f_{sync}	Buck synch. range	External clock input on SYNC	150		600	kHz
V_{RT}	Oscillator reference voltage			1.2		V
$t_{SW-Prop\ dly}$	SYNC rising edge to PH rising edge delay		0	20	40	ns
$t_{SW-Trans-delay}$	Last SYNC rising edge to return to resistor mode if CLK is not present on SYNC pin			20		µs

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Electrical Characteristics (接下页)

V_{IN} = V_{LR1} = 8 V to 18 V, V_{SUP} = 4 V to 10 V, $V_{IN2SENSE}$ = 4 V to 40 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ERROR AMPLIFIER (OTA) FOR BUCK CONTROLLERS AND BUCK CONVERTER							
$I_{PULLUP_VSENSEx}$	Pullup current at VSENSEx pins	VSENSEx = 0 V		50	100	200	nA
gm	Forward transconductance	COMP1, COMP2 = 0.8 V; source/sink = 5 µA, Test in feedback loop		0.7	0.9	1.35	mS
EXTERNAL CLOCK AND ENABLE INPUTS: SYNC. EN1, EN2, EN3, EN4							
V_{IH}	Higher threshold	V_{IN} = 13 V		1.7			V
V_{IL}	Lower threshold	V_{IN} = 13 V				0.7	V
R_{IH}	Pulldown resistance	V_{SYNC} = 5 V			500		kΩ
I_{IL_ENx}	Pullup current	V_{ENx} = 0V			0.5	2	µA
$t_{deglitch}$	Deglitch time, ENx			2		16	µs
LINEAR REGULATOR LREG1							
V_{LREG1}	Regulated output range	I_L = 10 µA to 300 mA		0.8		5.25	V
V_{REF}	Internal reference voltage tolerance	Referred to 0.8-V V_{REF}, measured at VSENSE4		–2.5%		2.5%	
$V_{line-reg}$	Line regulation	V_{IN} = V_{LR1}: 6 V to 28 V, I_{OUT} 4 = 10 mA,	ΔV_{OUT}, V_{OUT} = 5 V			15	mV
			ΔV_{OUT}, V_{OUT} = 3.3 V			15	
			ΔV_{OUT}, V_{OUT} = 1.5 V			15	
$V_{load-reg}$	Load regulation	I_{OUT4} = 10 mA to 300 mA, V_{IN} = 14 V	ΔV_{OUT}, V_{OUT} = 5 V			10	mV
			ΔV_{OUT}, V_{OUT} = 3.3 V			10	
			ΔV_{OUT}, V_{OUT} = 1.5 V			10	
$V_{Dropout}$	Drop out voltage	V_{IN} = V_{LR1} = 4 V: I_{OUT} = 250 mA				500	mV
		V_{IN} = 9 V, V_{LR1} = 4 V: I_{OUT} = 150 mA				300	
I_{OUT4}	Output current	V_{OUT} in regulation		0.01		300	mA
$I_{LREG1-CL}$	Output current limit	V_{OUT} = 0 V		400		1000	mA
dV_{LREG1} / dt	Output soft start slew rate				5		V/ms
PSRR	Power supply ripple rejection	V_{ripple} = 0.5 V_{PP}, I_{OUT} = 300 mA	Freq = 100 Hz		60		dB
			Freq = 150 kHz		25		
$V_{TH-CP\ ONp}$	Charge-pump turnoff voltage, V_{IN} rising				9.4		V
	Hysteresis				0.18		V
$I_{TH-CP-OFF}$	Low-load current-detection threshold	I_{OUT}4 falling			2		mA
	Low-load current-detection hysteresis				4		mA
SOFT START SSX							
I_{SSx}	Soft-start source current	SSx = 0 V		0.75	1	1.25	µA
RESET RSTx							
RST_{pullup}	RST1 to S2, RST2 to S4, RST4 to LREG1 internal pullups				50		kΩ
$RSTx_{th1}$	Reset threshold	VSENSEx falling		–5	–7	–9.5	%VREF
$RSTx_{hys}$	Hysteresis				2		%VREF
$RSTx_{drop}$	Voltage drop	I_{RSTx} = 5 mA				450	mV
		I_{RSTx} = 1 mA				100	mV
$RSTx_{leak}$	Leakage	V_{S2} = V_{S4} = V_{RSTx} = 13 V, RST4 = 8 V				1	µA
$t_{deglitch}$	Power-good deglitch time			2		16	µs
t_{delay}	Reset release delay	External capacitor = 1 nF			1		ms
t_{delay_fix}	Fixed reset delay	No external capacitor, Rdelay pin open			20	50	µs
I_{OH}	Activate current source (current to charge external capacitor)	Current to charge external capacitor		30	40	50	µA
I_{IL}	Activate current sink (current to discharge external capacitor)	Current to discharge external capacitor		30	40	50	µA

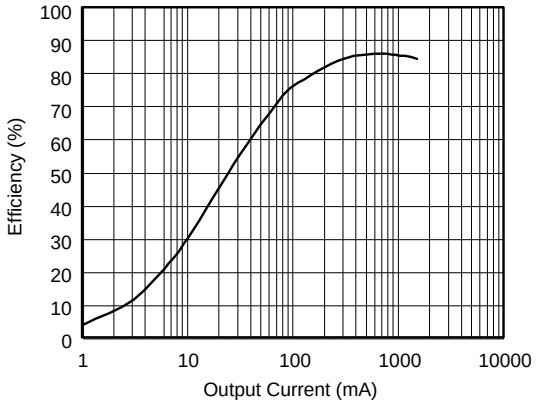
Electrical Characteristics (接下页)

V_{IN} = V_{LR1} = 8 V to 18 V, V_{SUP} = 4 V to 10 V, $V_{IN2SENSE}$ = 4 V to 40 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONOUS BUCK CONVERTER BUCK3						
V_{SUP}	Buck3 supply voltage		4		10	V
V_{SUP_UV}	Buck3 undervoltage lockout	V_{SUP} falling	3.6	3.7	3.8	V
		V_{SUP} rising	3.7	3.8	3.9	V
$r_{DS(on)}$	High-side switch	V_{SUP} = 9 V, $V_{Boot3\ –PH3}$ = 5.8 V		0.14	0.28	Ω
	Low-side switch	V_{SUP} = 9 V, $V_{VREG-PGND3}$ = 5.8 V		0.15	0.28	Ω
$I_{HS-Limit}$	High-side switch		2.5			A
$I_{LS-Limit}$	Low-side switch, current into PH3		2.38			A
V_{SUPLkg}	VSUP leakage current	V_{SUP} = 10 V for high side, EN3 = Low. T_J = 100°C		1		µA
I_{FB3}	Current foldback	VSENSE3 = 0 V		1.9		A
f_{SW-adj}	Buck3 switching frequency range with external resistor	Using external resistor on RT/CLK	150		600	kHz
V_{Sense}	Feedback voltage	Internal ref = 0.8 V	–1.5%		1.5%	
$f_{SW-f-back}$	2-times - frequency foldback exit threshold, VSENSE3 rising			0.65		V
	2-times - frequency foldback entry threshold, VSENSE3 falling			0.6		V
Gm3	Current loop transconductance	$\Delta I_{peakPH3}$ / ΔV_{COMP3}		5.4		S
DC_3	Minimum duty cycle	f_{SW} = 400 kHz, SLEW = LOW or OPEN		10%		
	Maximum duty cycle	In dropout operation		98.75%		
$T_{OT-BUCK3}$	Overtemperature sensor threshold, leads to Buck3 FET deactivation			170		°C
$T_{OT-BUCK3-HYS}$	Overtemperature sensor hysteresis			15		°C
THERMAL SHUTDOWN						
$T_{shutdown}$	Junction temperature shutdown threshold		150	170		°C
T_{hys}	Junction temperature hysteresis			15		°C

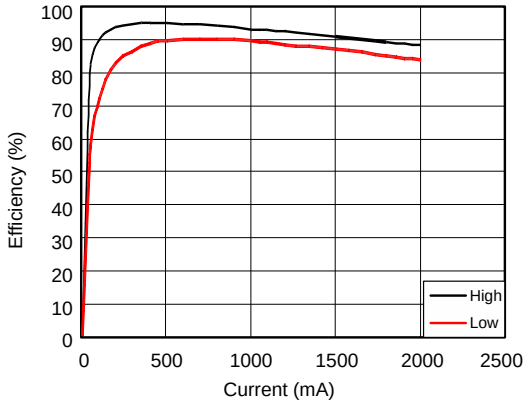
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6.6 Typical Characteristics



V_{OUT} = 3.3 V V_{IN} = 5 V

图 1. Buck2 Efficiency versus Output Current Continuous Mode



V_{IN} = 14 V V_{OUT} = 3.3 V V_{SUP} = 4 V

图 2. Buck3 Efficiency vs Output Current, 400 kHz 25°C

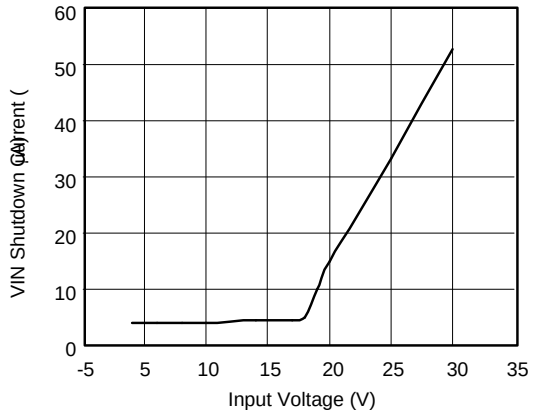


图 3. VIN Shutdown Current vs VIN

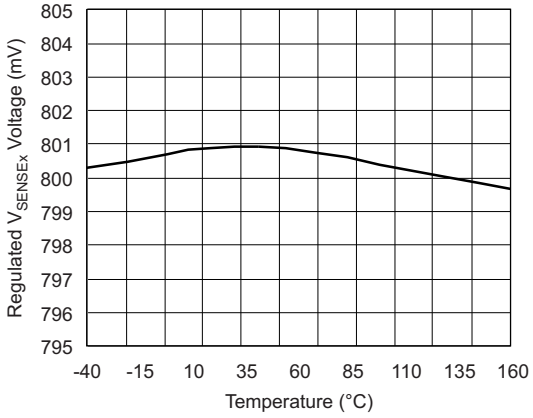
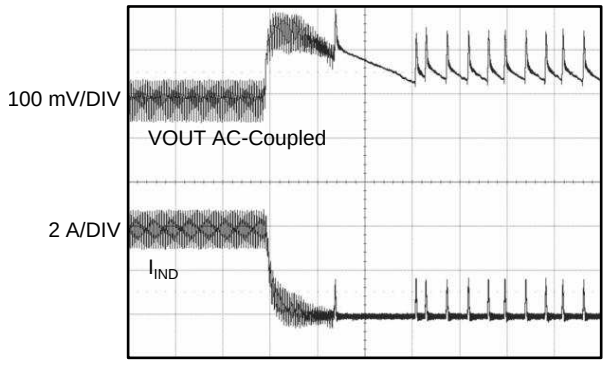


图 4. Regulated VSENSEx Voltage vs Temperature (Buck1 and Buck2)

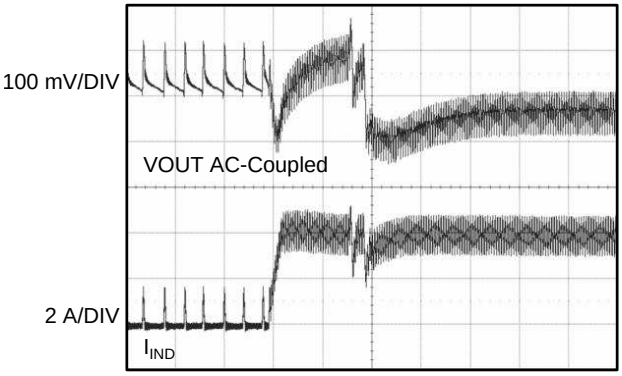


Time = 50 µs/DIV

V_{IN} = 12 V V_{OUTx} = 5 V R_{SENSE} = 10 mΩ

Inductor = 4.7 µH Switching Frequency = 400 kHz

图 5. Buck1 and Buck2 Load Step: Low-Power-Mode Entry (0.09 mA to 4 A at 2.5 A/µs)



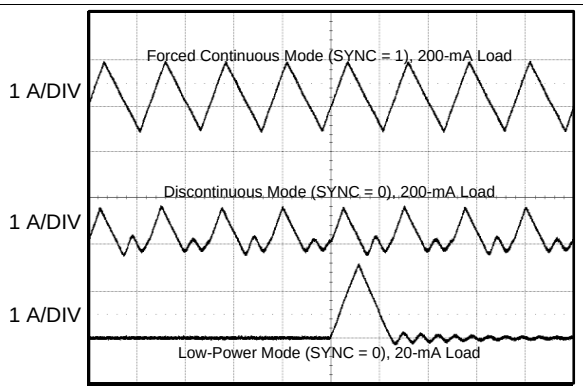
Time = 50 µs/DIV

V_{IN} = 12 V V_{OUTx} = 5 V R_{SENSE} = 10 mΩ

Inductor = 4.7 µH Switching Frequency = 400 kHz

图 6. Buck1 AND Buck2 Load Step: Low-Power-Mode Exit (0.09 mA to 4 A AT 2.5 A/µs)

Typical Characteristics (接下页)



V_{IN} = 12 V V_{OUTx} = 5 V R_{SENSE} = 10 mΩ
Inductor = 4.7 µH Switching Frequency = 400 kHz

图 7. Inductor Currents (Buck1 and Buck2)

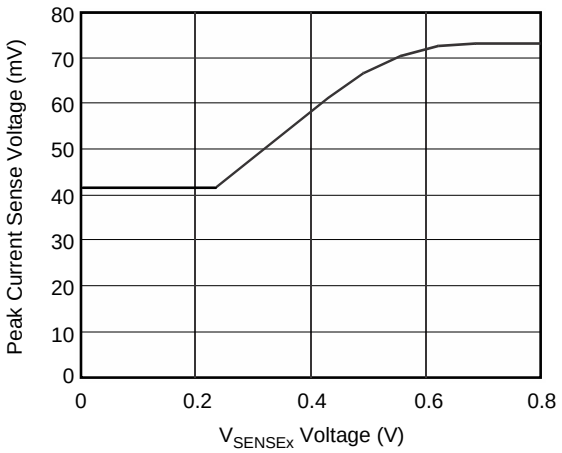


图 8. Foldback Current Limit (Buck1 and Buck2)

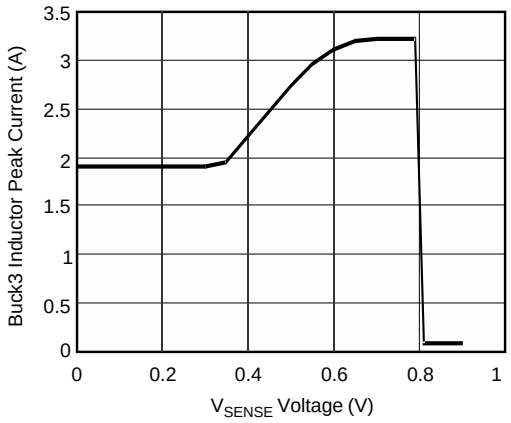


图 9. Foldback Current Limit (Buck3)

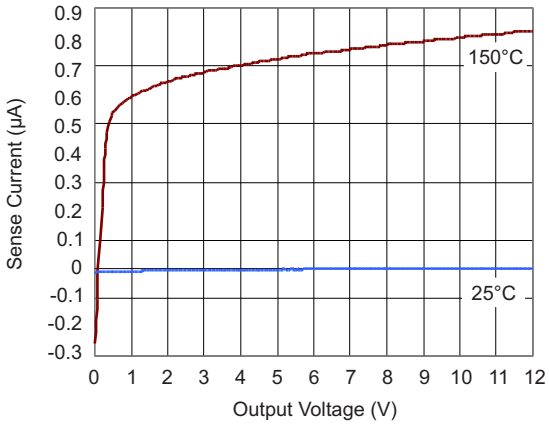


图 10. Current Sense Pins Input Current (Buck1 and Buck2)

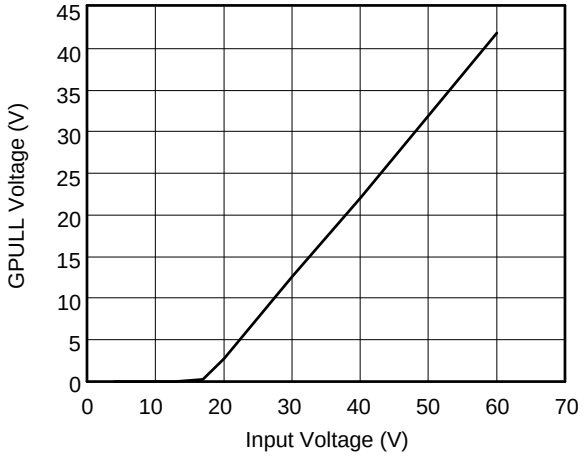


图 11. GPULL Voltage vs VIN

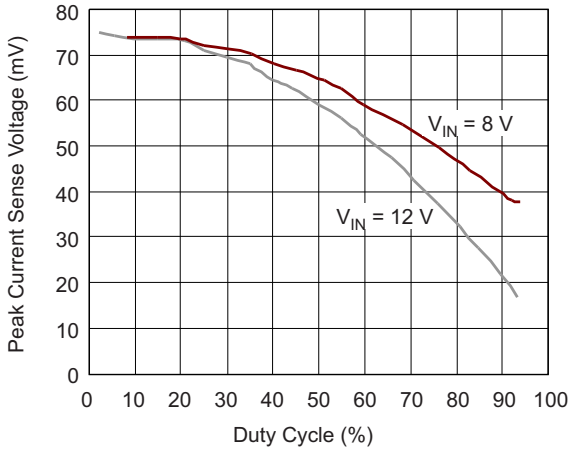
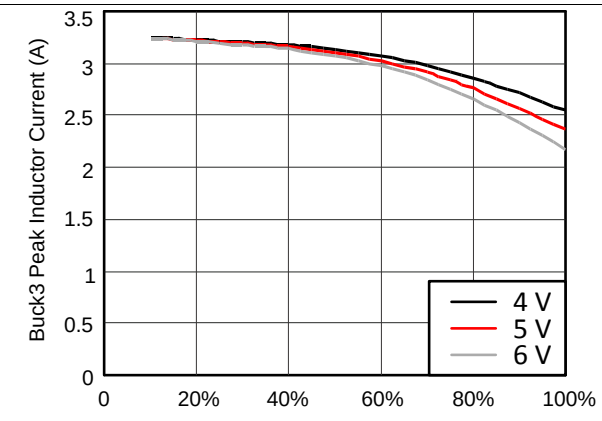


图 12. Current Limit vs Duty Cycle (Buck1 and Buck2)

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Typical Characteristics (接下页)



V_{SUP} = 4, 5, OR 6 V Inductor = 10 µH V_{SENSE3} = 0.75 V
Switching Frequency = 400 kHz

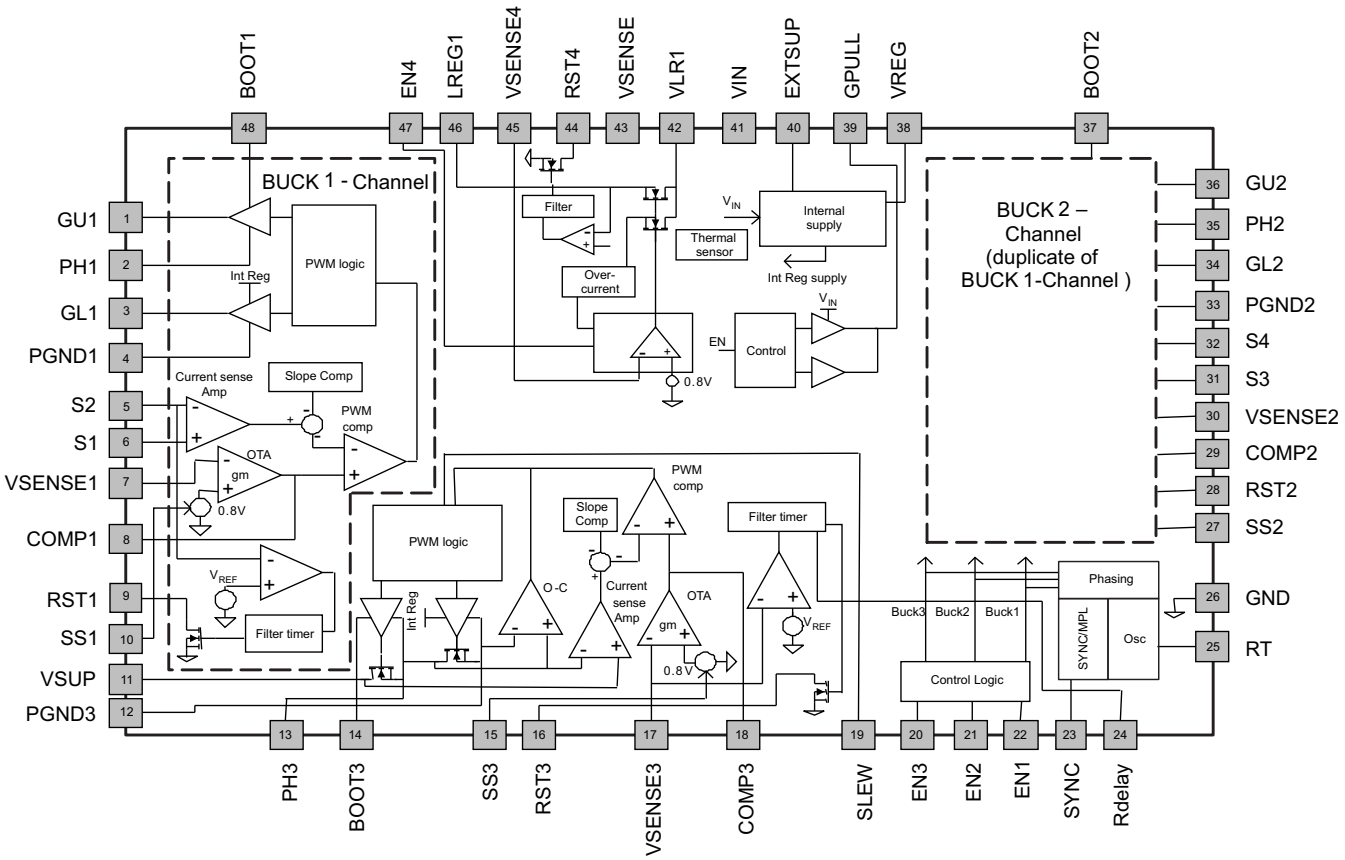
图 13. Buck3 Maximum Peak Inductor Current vs Duty Cycle

7 Detailed Description

7.1 Overview

The TPS43340-Q1 is a dual-buck regulator controller (Buck1, Buck2), single-buck regulator converter (Buck3) and linear regulator (LREG1) designed for powering the Texas Instruments family of DSPs and microcontrollers or general-market MCU products. The device features integrated short-circuit and overcurrent protection on the gate-drive outputs for the buck regulator controllers and independent current-foldback control for each buck regulator supply during regulator output short to ground. Each output supply incorporates a soft start to ensure that on initial power up these regulated outputs are not in current limit. Implementation of reset delay on power up allows the outputs of Buck1, Buck2, Buck3 and the linear regulator to get to stable regulation. An external capacitor sets the delay to a maximum range of 300 ms. Each power-supply output has adjustable output voltage based on the external resistor-network settings. The device has sequencing control during power up and power down of the output rails, based on the enable-and-disable control or soft start.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Enable Inputs

The use of independent enable inputs at the EN1 through EN4 pins enables all the regulators. These pins have internal pullup currents of 0.5 µA (typical). As a result, an open circuit on any of these pins enables its respective regulator. EN1, EN2, and EN4 are high-voltage pins, which permits their connection directly to the battery for self-bias. When all regulators are disabled, the device shuts down and consumes a current of 5 µA typical.

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Feature Description (接下页)

7.3.2 Linear Regulator (LREG1)

The linear regulator is an NMOS output low-dropout regulator with output load current up to 300 mA. It can operate directly from the battery. With EN4 tied high or open, LREG1 turns on its output following an internally generated soft-start ramp. The regulation loop uses internal frequency compensation. If the output shorts to ground, the device protects itself by limiting the current. For V_{IN} lower than 9 V, LREG1 controls the internal charge pump depending on V_{IN} and the load current in accordance with 表 4. An internal voltage selector selects the higher available supply, V_{IN} or the charge pump voltage, for the error amplifier. The device monitors the output voltage of the low-dropout regulator for undervoltage and signals its state on pin RST4.

7.3.3 Gate-Driver Supply (VREG, EXTSUP)

An internal linear regulator supplies the gate drivers of the buck controllers and the buck converter. The regulator output (5.8 V typical) is available at the VREG pin and requires decoupling using a ceramic capacitor in the range of 3.3 µF to 10 µF. This pin has an internal current-limit protection; do not use it to power any other circuits.

Power for the VREG linear regulator comes from VIN by default when the EXTSUP voltage is lower than 4.6 V (typical). Should there be an expectation of VIN going to high levels, there can be excessive power dissipation in this regulator, especially at high switching frequencies and when using large external MOSFETs. In this case, it is advantageous to power this regulator from the EXTSUP pin, connection to which can be to a supply lower than VIN but high enough to provide the gate drive. The voltage on EXTSUP should not exceed 9 V. With EXTSUP connected to a voltage greater than 4.6 V, the linear regulator automatically switches to EXTSUP. Efficiency improvements are thus possible when using one of the switching regulator rails from the TPS43340-Q1 device or any other voltage available in the system to power the EXTSUP. If the EXTSUP supply is above 4.6 V but below 7.5 V, the EXTSUP-LDO acts as a pass element, providing EXTSUP voltage less a small dropout to VREG.

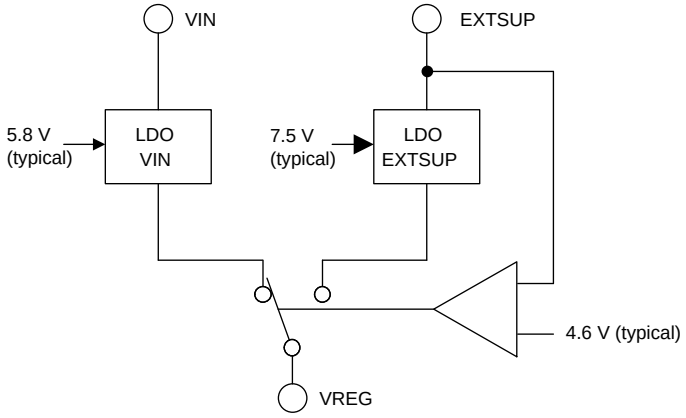


图 14. Internal Gate-Driver Supply

Using a voltage above 5.8 V (sourced by VIN) for EXTSUP is advantageous, as it provides a large gate drive and hence better on-resistance of the external MOSFETs.

When using EXTSUP, always keep the buck rail supplying EXTSUP enabled. Alternatively, if it is necessary to switch off the buck rail supplying EXTSUP, place a diode between the buck rail and EXTSUP.

During low-power mode, the EXTSUP functionality is not available. The internal regulator operates as a shunt regulator powered from VIN and has a typical value of 7.5 V. Current-limit protection for VREG is available in low-power mode as well. If EXTSUP is unused, leave the pin open without a capacitor installed.

7.3.4 External P-Channel Drive (GPULL) and Reverse Battery Protection

The TPS43340-Q1 device includes a gate driver for an external P-channel MOSFET which can be used for reverse battery protection. This is useful to reduce the voltage drop across the protection element compared to using a series diode to V_{IN}. The gate – source voltage of the external PMOS is clamped by an internal Zener diode to 17 V typical.

Feature Description (接下页)

$V_{BAT} \leq V_F \rightarrow | V_{GS} | = 0\ V \rightarrow$ FET and diode not conducting
$V_F \leq V_{BAT} \leq V_T$ (FET) $\rightarrow | V_{GS} | = V_{BAT} \rightarrow$ FET NOT conducting and diode conducting
V_T (FET) $\leq V_{BAT} \leq 17\ V \rightarrow | V_{GS} | = V_{BAT} \rightarrow$ FET conducting
$V_{BAT} \geq 17\ V \rightarrow | V_{GS} | = 17\ V \rightarrow$ FET conducting

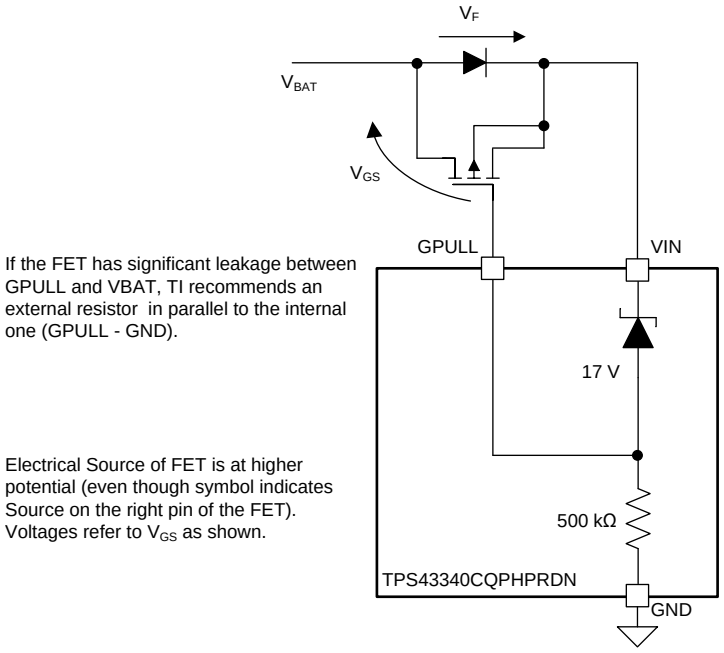


图 15. Internal Circuit of GPULL Output

注

An implementation without the PMOS blocks the current coming from Buck-outputs (improper OR-ing, and others), which may result in exceeding the absolute maximum ratings.

7.3.5 Undervoltage Lockout and Overvoltage Protection

The TPS43340-Q1 device starts up at a VIN voltage of 6.5 V (maximum). Once it has started up, the device operates down to a V_{IN} undervoltage lockout level of 3.6 V or until reaching a VREG undervoltage of 3.6 V. A voltage above 46 V at VIN shuts down the device. In order to prevent transient spikes from shutting down the device, the under- and overvoltage protection have filter times of 5 µs (typical). There is no support for overvoltage protection in LPM.

When the voltages return to the normal operating region, the enabled regulators start up with a soft-start ramp.

7.3.6 Synchronous Buck Converter Buck3

This regulator operates with the switching frequency set on the RT terminal or an external clock input on the SYNC terminal. The internal power FETs switch out of phase to regulate the output voltage, operating in a pulse width modulation. The converter uses a peak-current mode-control loop with external frequency compensation. The synchronous operation mode improves the overall efficiency.

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Feature Description (接下页)

7.3.6.1 Soft Start and Foldback Functions

A capacitor on the SS3 terminal sets the converter soft start. Pulling the enable pin on EN3 high activates soft start. During soft start or whenever the voltage on VSENSE3 falls below limits given by $f_{SW\text{-}f\text{-}back}$, the converter switches to a frequency foldback of f_{sw} / 2 to help control the coil current. In addition to the frequency foldback, implementation of current foldback reduces power dissipation to protect the converter against an output short to ground. Like in the buck controllers, the current foldback reduces the maximum peak current limit depending on the voltage on the VSENSE3 pin. 图 9 shows the characteristic of current foldback.

7.3.6.2 Current-Mode Control and Current-Limit Protection

Measurement of the coil peak current is by use of the high-side integrated FET; peak-current regulation occurs in each switching cycle in accordance with the voltage on the COMP3 pin. COMP3 is the output of a transconductance error amplifier of the voltage feedback loop for Buck3, as COMP1 and COMP2 are for controllers Buck1 and Buck2. COMP3 sets the target for the peak current comparator (inner current loop) and serves as frequency compensation of the voltage loop using a type II compensation network.

Clamping the voltage on the COMP3 node realizes the positive current limit. The positive clamping level depends on the voltage on the VSENSE3 pin, as described previously. The device also implements clamping for low voltage on the COMP3 pin, thereby speeding up the transient response after output overshoot. For stability of the current loop, during the switching cycle the internal slope compensation adjusts the current limit set by COMP3.

For correct operation of the slope compensation, the coil used for Buck3 must satisfy the following:

$$L_{Buck3} = 3.7 / f_{sw} \quad (1)$$

where

- L_{Buck3} is the inductance in henries
- f_{sw} is the switching frequency in hertz

Reaching the positive current limit during the high PWM phase resets the PWM. The high-side FET turns off and the low part of the cycle is initiated. On detecting an overcurrent condition such as an output short to a supply during the PWM low phase, the low-side FET turns off until the end of the given cycle, to allow the coil current to flow through the body diode of the high-side FET.

7.3.6.3 Operation in Dropout and Undervoltage Protection

This converter is capable of operating with a low input-to-output voltage difference. In dropout operation, the integrated high-side MOSFET stays on continuously. In every fourth clock cycle, the device limits the duty cycle to 95% in order to charge the bootstrap capacitor at BOOT3. This allows a maximum duty cycle of 98.75% for the buck converter. In this mode, the output tracks the input until initiation of the internal undervoltage lockout due to low supply voltage on the VSUP pin.

Thermal shutdown monitors the virtual junction temperature of the integrated FETs. When T_J exceeds 170°C, both the high- and low-side switches turn off. The converter returns to normal operation when the temperature decreases to the acceptable level (typically T_J = 150°C)

7.3.6.4 Slew Rate Control (SLEW)

The setting on the SLEW terminal controlss the slew for Buck3. Setting the slew rate to logic high (slowest slew rate) extends the minimum on-time of the buck converter by 5% of the clock period.

SLEW TERMINAL SETTING	t_r (TYP) ns	t_f (TYP) ns
SLEW > V_{REG} – 0.2 V (low slew rate, logic high)	24	7
SLEW pin open – medium slew rate	11	3
SLEW < 0.2 V (fast slew rate, logic low)	8	2

7.4 Device Functional Modes

7.4.1 Buck Controllers: Normal Mode PWM Operation

7.4.1.1 Setting the Operating Frequency

The buck controllers operate using constant-frequency peak-current-mode control for optimal transient behavior and ease of component choices. The switching frequency is programmable between 150 kHz and 600 kHz, depending on the resistor value at the RT pin. Tying this pin to ground sets the default switching frequency to 400 kHz. A resistor connected to RT can also set the frequency according to the formula:

f_{sw} = 24 x 10^9 / RT [Hz]

where

- 600 kHz requires 40 kΩ
- 150 kHz requires 160 kΩ (2)

It is also possible to synchronize to an external clock at the SYNC pin in the same frequency range of 150 kHz to 600 kHz. The device detects clock pulses at this pin, and an internal PLL locks onto the external clock within the specified range. The device can also detect a loss of clock at this pin, and detection of clock loss for $t_{SW\text{-}Trans\text{-}delay}$ sets the switching frequency to the internal oscillator. The two buck controllers operate at the same switching frequency, 180 degrees out of phase.

7.4.1.2 Feedback Inputs

Choose the resistor feedback divider networks connected to the VSENSEx (feedback) pins to set the output voltages. Make the choice such that the regulated voltages at the VSENSEx pins equal 0.8 V. The VSENSEx pins have 100-nA pullup current sources as a protection feature in case the pins open up as a result of physical damage.

$$V_{OUTx} = 0.8\left(1+\frac{R_{TOP}}{R_{BOTTOM}}\right) \quad V$$

where

- R_{TOP} is the resistor from V_{OUTx} to VSENSEx
- R_{BOTTOM} is the resistor from VSENSEx to ground. (3)

7.4.1.3 Soft-Start Inputs

In order to avoid large inrush currents, both buck controllers have independent programmable soft-start timing. The voltage at the SSx pins acts as the soft-start reference voltage. A 1-µA pullup current is available at the SSx pins, and by choosing a suitable capacitor one can obtain a desired soft-start ramp speed. After start-up, the pullup current ensures that pins SSx are higher than the internal reference of 0.8 V, which then becomes the reference for the buck controllers. The required capacitor for Δt, the desired soft-start time, is given by:

$$C_{SS} = \frac{I_{SS} \times \Delta t}{\Delta V} \text{ (Farads)}$$

where

- I_{SS} = 1 µA (typical)
- ΔV = 0.8 V (4)

Alternatively, one can use the soft-start pins as tracking inputs. In this case, connect the pins to the supply to be tracked via a suitable divider network.

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Device Functional Modes (接下页)

7.4.1.4 Current-Mode Operation

Peak current-mode control regulates the peak current through the inductor such that the output voltage maintains its set value. The error between the feedback voltage at VSENSEx and the internal reference produces a signal at the output of the error amplifier (COMPx) which serves as the target for the peak inductor current. This target provides a comparison for the current through the inductor, sensed as a differential voltage at S1-S2 for Buck1 and S3-S4 for Buck2, and compared with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at VSENSEx, causing COMPx to fall or rise, respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. In this way, the device maintains the output voltage in regulation.

The high-side N-channel MOSFET turns on at the beginning of each clock cycle and remains on until the inductor current reaches its peak value. Once this MOSFET turns off, and after a small delay (shoot-through delay), the lower N-channel MOSFET turns on until the start of the next clock cycle. In dropout operation, the high-side MOSFET stays on continuously. In every fourth clock cycle, the duty cycle is limited to 95% in order to charge the bootstrap capacitor at BOOTx. This allows a maximum duty cycle of 98.75% for the buck regulators. Thus, during dropout the buck regulators switch at one-fourth of the normal frequency.

7.4.1.5 Current Sensing and Current Limit With Foldback

Clamping the maximum value of COMPx is such as to limit the maximum current through the inductor to a specified value. When the output of the buck regulator (and hence the feedback value at VSENSEx) falls to a low value due to a short circuit or overcurrent condition, the clamping voltage at the COMPx successively decreases, thus providing current foldback protection. This protects the high-side external MOSFET from excess current (forward-direction current limit).

Similarly, if due to a fault condition the output shorts to a high voltage and turns the low-side MOSFET fully on, the COMPx node drops low. The device holds COMPx at a low level as well in order to limit the maximum current in the low-side MOSFET (reverse direction current limit).

An external resistor senses the current through the inductor. Choose the sense resistor such that the maximum forward peak current in the inductor generates a voltage of 75 mV across the sense pins. This value specification is at low duty cycles only. At typical duty cycle conditions around 40% (assuming 5-V output and 12-V input), 50 mV is a more reasonable value, considering the slope compensation and tolerances. The typical characteristics in 图 17 and 图 12 provide a guide for using the correct current-limit sense voltage.

The current-sense pins Sx are high-impedance pins with low leakage across the entire output range. These pin characteristics allow DCR current sensing using the dc resistance of the inductor for higher efficiency. 图 16 shows DCR sensing. Here the series resistance (DCR) of the inductor serves as the sense element. Place the filter components close to the device for noise immunity. Remember that while DCR sensing gives high efficiency, it is less accurate due to the temperature sensitivity and a wide variation of the parasitic series resistance of the inductor. Hence, it may often be advantageous to use the more-accurate sense resistor for current sensing.

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Device Functional Modes (接下页)

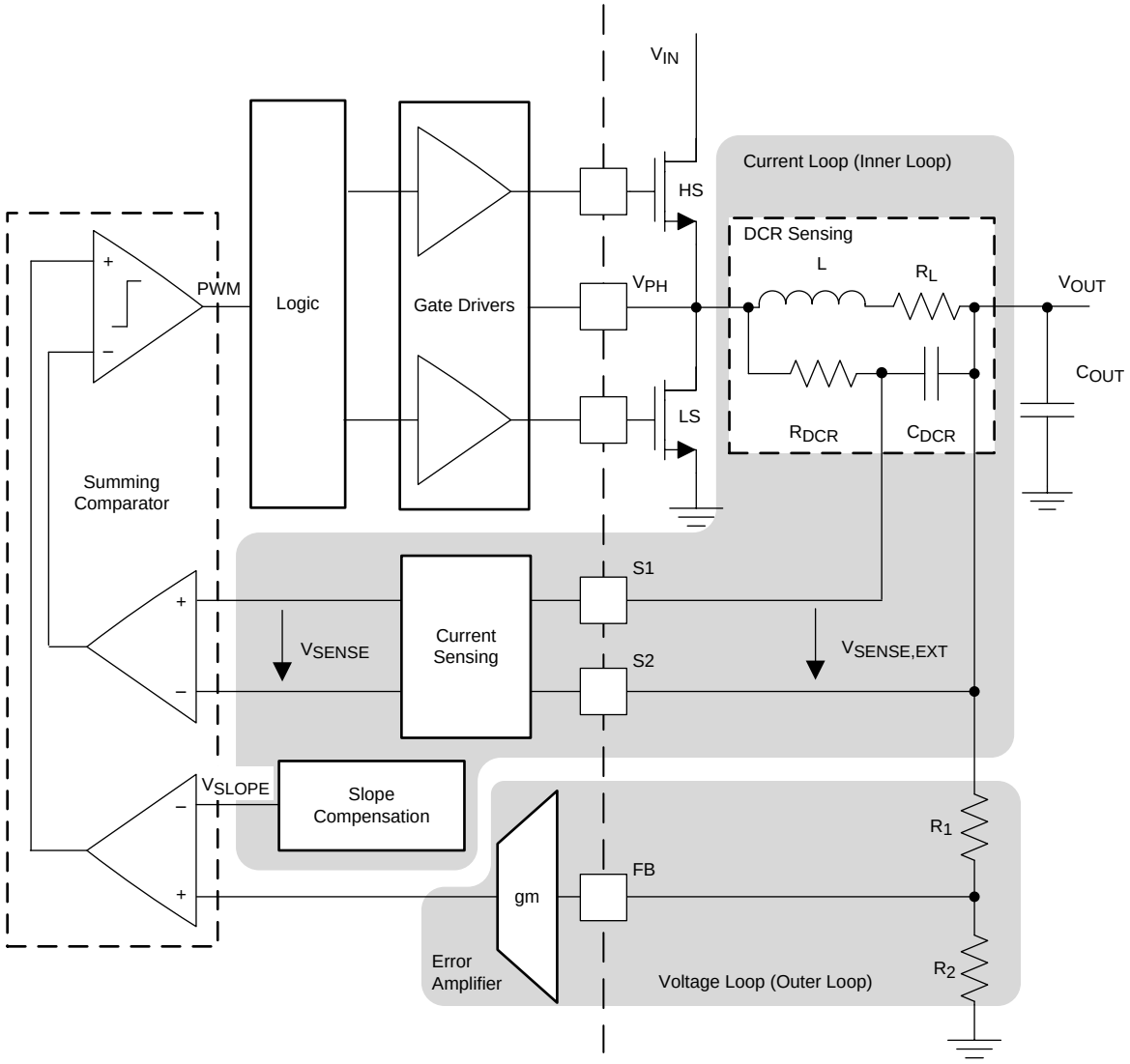


图 16. Overcurrent Sensing and Control

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Device Functional Modes (接下页)

7.4.1.6 Slope Compensation

Optimal slope compensation which is adaptive to changes in input voltage and duty cycle allows stable current-mode operation in all conditions. For optimal performance of this circuit, satisfy the following condition in the choice of inductor and sense resistor:

$$L = \frac{200}{f_{SW}} \times R_S$$

where

- L is the buck regulator inductor in henries
- R_S is the sense resistor in ohms
- f_{sw} is the buck regulator switching frequency in Hz (5)

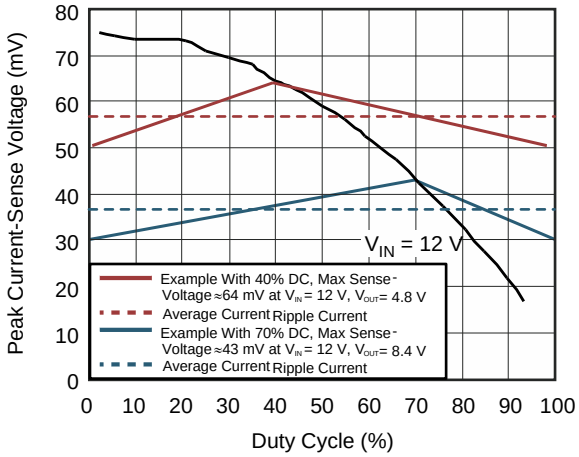


图 17. Peak Current-Sense Voltage versus Duty Cycle

7.4.1.7 Reset Outputs and Filter Delays

Each buck controller has an independent reset comparator monitoring the feedback voltage at the VSENSEx pins and indicating whether the output voltage has fallen below the specified reset threshold. The reset indicator is available as an open-drain output at the RSTx pins. An internal 50-kΩ pullup resistor to S2 or S4 is available, or one can use an external resistor. When a buck controller shuts down, the device pulls down the power-good outputs internally. Connecting the pullup resistor to a rail other than the output of that particular buck channel causes a constant current flow through the resistor when the buck controller powers down.

In order to avoid triggering the power-good indicators due to noise or fast transients on the output voltage, the device implements an internal delay of $t_{deglitch}$ for de-glitching. The output voltage reaching its set value after a start-up ramp or negative transient asserts the power-good indicator high (releases the open-drain pin) after a delay of t_{delay}, at least t_{delay_fix}. A use of this is to delay the reset to the circuits being powered from the buck regulator rail. Program the delay of this circuit by using a suitable capacitor at the Rdelay pin according to 公式 6:

Power-Good Output Delay

$$t_{Rdelay} = 10^6 \times C_{Rdelay} \text{ (seconds)}$$

where

- C_{Rdelay} is the capacitor value in farads on the Rdelay pin. (6)

An open on the Rdelay pin sets the delay to a default value of 20 µs typical. The power-good delay timing is common to all supply rails, but the power good comparators and outputs function independently.

Device Functional Modes (接下页)

7.4.1.8 Light-Load PFM Mode

An external clock or a high level on the SYNC pin or enabling Buck3 results in forced continuous-mode operation of the bucks. Having the SYNC pin low or open allows the buck controllers to operate in discontinuous mode at light loads by turning off the low-side MOSFET on detection of a zero-crossing in the inductor current.

In discontinuous mode, as the load decreases, the duration of the clock period when both the high-side and the low-side MOSFETs are turned off increases (deep discontinuous mode). In case the duration exceeds 60% of the clock period and V_{IN} > 8 V, the buck controller switches to a low-power operation mode. The design ensures that this typically occurs at 1% of the set full-load current if the choice of the inductor and the sense resistor is appropriate as recommended in the slope compensation section.

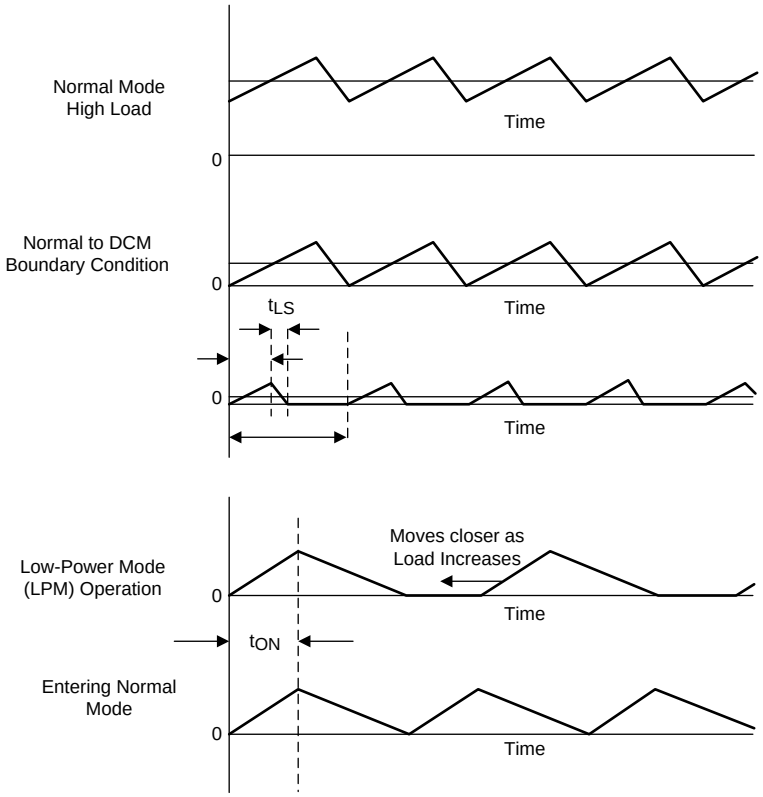


图 18. Modes of Operation

In low-power PFM mode, the buck controllers monitor the V_{SENSEx} voltage and compare it with the 0.8 V internal reference. Whenever the V_{SENSEx} value falls below the reference, the high-side MOSFET turns on for a pulse-duration inversely proportional to the difference across VIN-S2 for Buck 1 and VIN-S4 for Buck2. At the end of this on-time, the high-side MOSFET turns off and the current in the inductor decays until it becomes zero. The low-side MOSFET does not turn on. The next pulse occurs the next time V_{SENSEx} falls below the reference value. This results in a constant volt-second T_{ON} hysteretic operation with a total device quiescent current consumption of 30 µA when a single buck channel is active and 35 µA when both channels are active.

As the load increases, the pulse become more and more frequent until the current in the inductor becomes continuous. At this point, the buck controller returns to normal fixed-frequency current-mode control. Another criterion for exit from the low-power mode is when VIN falls low enough to require a higher-than-80% duty cycle of the high-side MOSFET.

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Device Functional Modes (接下页)

The TPS43340-Q1 device can support the full-current load during low-power mode until the transition to normal mode takes place. The design ensures the low-power-mode exit occurs at 10% (typical) of full-load current if the inductor and sense resistor choices are as recommended. Moreover, there is always a hysteresis between the entry and exit thresholds to avoid oscillating between the two modes.

In the event that both buck controllers are active, low-power mode is only possible when both buck controllers have light loads that are low enough for entry to low-power mode.

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8 Application and Implementation

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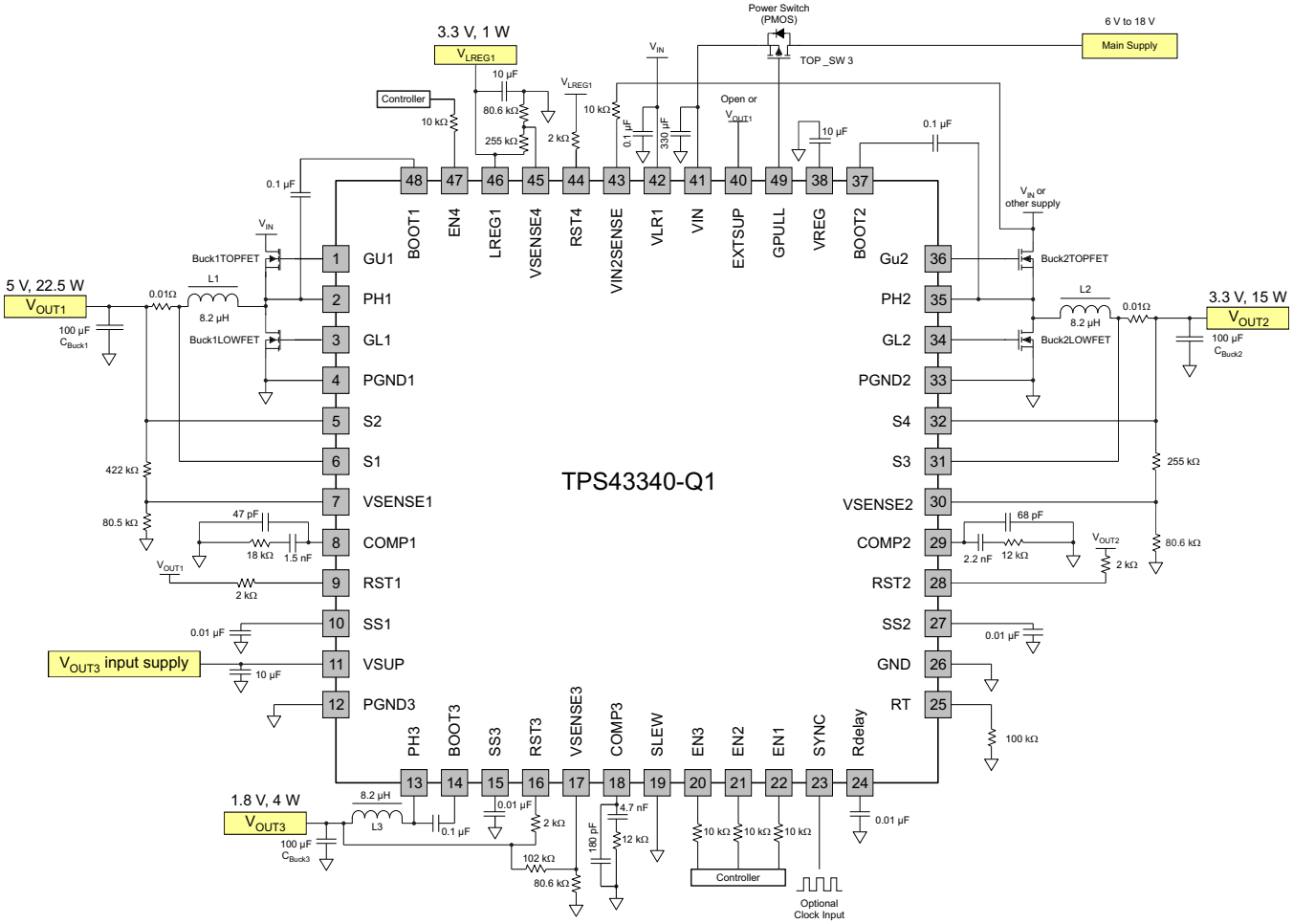
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS43340-Q1 multirail power supply operates with a supply voltage VIN of 4 V to 40 V for the Buck controllers and the LDO. The TPS43340-Q1 Buck converter (Buck3) operates with a supply voltage VSUP of 4 V to 10 V. For reducing power dissipation, TI strongly recommends using the output voltage of one of the buck regulators as the input supply for the LDO regulator. To use the output voltage of the buck regulator this way, the selected buck-regulator output voltage must be higher than the selected LDO-regulator output voltage. For further efficiency improvements, the part offers a pin to control an external FET that can bypass the reverse-polarity-protection diode (GPULL).

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8.2 Typical Application



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L1, L2, L3: DR127-8R2-R (Coiltronics)

TOP_SW3: IRF7663TRPBF (International Rectifier)

TOP_SW1, BOT_SW2: Si4946BEY-T1-E3 (Vishay)

TOP_SW2, BOT_SW2: Si4946BEY-T1-E3 (Vishay)

CBUCK1, CBUCK2, CBUCK3:AVX- TPSD107K016R0060 (AVX)

图 19. Application Schematic

Typical Application (接下页)

8.2.1 Design Requirements

A few parameters must be known to begin the design process. Determination of these parameters is typically at the system level.

The following example illustrates the design process and component selection for the TPS43340-Q1 device. 表 1 lists the design goal parameters.

表 1. Application Example

PARAMETER	Buck1	Buck2	Buck3
Input voltage, V_{IN}	6 V to 18 V 14 V, typical	6 V to 18 V 14 V, typical	4 V to 10 V 5 V, typical
Output ripple voltage	±0.2 V	±0.2 V	±0.1 V
Output voltage, V_{OUT}	5 V ±2%	3.3 V ±2%	1.8 V ±2%
Maximum output current, I_{OUT}	4.5 A	4.5 A	2.2 A
Minimum output current, I_{OUT}	0.1 A	0.1 A	0.1 A
Load-step output tolerance, $\Delta V_{OUT} + \Delta V_{OUT(Ripple)}$	±0.3 V	±0.3 V	±0.15 V
Current-output load step, ΔI_{OUT}	0.1 A to 4.5 A	0.1 A to 4.5 A	0.1 A to 2.2 A
Converter switching frequency, f_{SW}	400 kHz	400 kHz	400 kHz
Junction temperature, T_J	125°C	125°C	125°C

8.2.2 Detailed Design Procedure

8.2.2.1 High- and Low-Side Power NMOS Selection for the Buck Converters

An internal supply, which is 5.8 V typical under normal operating conditions, provides the gate-drive supply for these MOSFETs. The output is a totem pole, allowing full voltage drive of VREG to the gate with a peak output current of 0.6 A. The high-side MOSFET reference is the phase terminal (PHx), and the low-side MOSFET referenced is the power ground (PGNDx) terminal. For a particular application, select these MOSFETs with consideration for the following parameters $r_{DS(on)}$, gate charge Qg, drain-to-source breakdown voltage BVDSS, maximum dc current I_{DC}(maximum), and thermal resistance for the package.

Power dissipation on the high-side FET (P_{D_HS}):

$$P_{D_HS} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \quad (7)$$

First term is conduction losses.

Second term is switching losses.

Power dissipation on the low-side FET (P_{D_LS}):

$$P_{D_LS} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times (1 - D) + V_f \times I_{OUT}\ (t_{dead}) \times f_{SW} \quad (8)$$

The first term in the foregoing equation refers to conduction losses, and the second term covers the switching losses in the FET body diode during the dead-time.

注

$r_{DS(on)}$ has a positive temperature coefficient TC, which is typically 0.4%/°C.

Gate losses for high-side and low-side FETs:

$$P_{BuckX\ GATE} = 2 \times f_{sw} \times Qg \times V_{REG} \quad (9)$$

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8.2.2.2 Buck1 Component Selection

Duty Cycle

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{5\ V}{14\ V} = 0.357 \quad (10)$$

Selection of Current Sensing Resistor

$$R_{SENSE} = \frac{0.075\ V}{4.5\ A} = 0.017\ \Omega \quad (11)$$

Use 10 mΩ to allow for ripple-current.

Inductor Selection L

$$L = 200 \times \frac{0.01\ \Omega}{400\ kHz} = 5\ \mu H \quad (12)$$

Use 8.2 µH.

Inductor Ripple Current

$$\Delta I_{L(RIPPLE)} = \frac{5\ V}{400\ kHz \times 8.2\ \mu H} \times \left(1 - \frac{5\ V}{14\ V}\right) = 0.98\ A \quad (13)$$

Output Capacitor C_{OUT}

$$C_{OUT} = \frac{2 \times 4.5\ A}{400\ kHz \times 0.2\ V} = 112\ \mu F \quad (14)$$

Use 100 µF.

$$\Delta V_{OUT1} = \frac{\Delta I_{OUT2}}{4 \times f_C \times C_{OUT1}} + \Delta I_{OUT1} \times ESR = \frac{4.4\ A}{4 \times 50\ kHz \times 100\ \mu F} + 4.4\ A \times 10\ m\Omega = 264\ mV \quad (15)$$

$$V_{OUT1(Ripple)} = \frac{I_{OUT1(Ripple)}}{8 \times f_{SW} \times C_{OUT1}} + I_{OUT1(Ripple)} \times ESR = \frac{0.98\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.98\ A \times 10\ m\Omega = 12.8\ mV \quad (16)$$

Input Capacitor C_{IN}

$$C_{IN} = \frac{0.25 \times 4.5\ A}{400\ kHz \times 0.5\ V} = 5.6\ \mu F \quad (17)$$

Use 10 µF, shared between Buck1 and Buck2.

High-Side MOSFET (Buck1TOPFET)

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \quad (18)$$

$$C_{IN} = \frac{0.25 \times 4.5\ A}{400\ kHz \times 0.5\ V} = 5.6\ \mu F \quad (19)$$

Low-Side MOSFET (Buck1LOWFET)

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times (1 - D) + V_F \times I_{OUT} \times (2 \times t_d) \times f_{SW} \quad (20)$$

$$(4.5\ A)^2 \times 0.009 \times (1 + 0.4) \times (1 - 0.357) + 0.6\ V \times 4.5\ A \times (2 \times 20\ ns) \times 400\ kHz = 0.21\ W \quad (21)$$

8.2.2.3 Buck2 Component Selection

Duty Cycle

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{3.3\ V}{14\ V} = 0.236 \quad (22)$$

Selection of Current-Sensing Resistor

$$R_{SENSE} = \frac{0.075\ V}{4.5\ A} = 0.017\ \Omega \quad (23)$$

Use 10 mΩ to allow for ripple current.

Inductor Selection L

$$L = 200 \times \frac{0.01\ \Omega}{400\ kHz} = 5\ \mu H \quad (24)$$

Use 8.2 uH.

Inductor Ripple Current

$$\Delta I_{L(RIPPLE)} = \frac{3.3\ V}{400\ kHz \times 8.2\ \mu H} \times \left(1 - \frac{3.3\ V}{14\ V}\right) = 0.77\ A \quad (25)$$

Output Capacitor C_{OUT}

$$C_{OUT} = \frac{2 \times 4.5\ A}{400\ kHz \times 0.2\ V} = 112\ \mu F \quad (26)$$

Use 100 µF.

$$\Delta V_{OUT2} = \frac{\Delta I_{OUT2}}{4 \times f_C \times C_{OUT2}} + \Delta I_{OUT2} \times ESR = \frac{4.4\ A}{4 \times 50\ kHz \times 100\ \mu F} + 4.4\ A \times 10\ m\Omega = 264\ mV \quad (27)$$

$$V_{OUT2(Ripple)} = \frac{I_{OUT2(Ripple)}}{8 \times f_{SW} \times C_{OUT2}} + I_{OUT2(Ripple)} \times ESR = \frac{0.77\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.77\ A \times 10\ m\Omega = 10.1\ mV \quad (28)$$

Input Capacitor C_{IN}

$$C_{IN} = \frac{0.25 \times 4.5\ A}{400\ kHz \times 0.5\ V} = 5.6\ \mu F \quad (29)$$

Use 10 µF, shared between Buck1 and Buck2. For better line-transient immunity, use a larger value.

High-Side MOSFET (Buck2TOPFET)

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \quad (30)$$

$$(4.5\ A)^2 \times 0.009\ \Omega \times (1 + 0.4) \times 0.236 + \left(\frac{14\ V \times 4.5\ A}{2}\right) \times (20\ ns + 20\ ns) \times 400\ kHz = 0.56\ W \quad (31)$$

Low-Side MOSFET (Buck2LOWFET)

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times (1 - D) + V_F \times I_{OUT} \times (2 \times t_d) \times f_{SW} \quad (32)$$

$$(4.5\ A)^2 \times 0.009\ \Omega \times (1 + 0.4) \times (1 - 0.236) + 0.6\ V \times 4.5\ A \times (2 \times 20\ ns) \times 400\ kHz = 0.24\ W \quad (33)$$

8.2.2.4 Buck3 Component Selection

Duty Cycle

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{1.8\ V}{5\ V} = 0.36 \quad (34)$$

Inductor Selection L_{Buck3}

$$L_{BUCK3} = \frac{3.7\ \Omega}{400\ kHz} = 9.25\ \mu H \quad (35)$$

Use 8.2 µH.

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Inductor Ripple Current

$$\Delta I_{L(RIPPLE)} = \frac{1.8\ V}{400\ kHz \times 8.2\ \mu H} \times \left(1 - \frac{1.8\ V}{5\ V}\right) = 0.46\ A \quad (36)$$

Output Capacitor C_{OUT}

$$C_{OUT3} \approx \frac{2 \times \Delta I_{OUT3}}{f_{SW} \times \Delta V_{OUT3}} = \frac{2 \times 2.1\ A}{400\ kHz \times 0.15\ V} = 70\ \mu F \quad (37)$$

Use 100 µF.

Input Capacitor C_{IN}

$$C_{IN} = \frac{0.25 \times 2.2\ A}{400\ kHz \times 0.05\ V} = 5.76\ \mu F \quad (38)$$

Use 10 µF.

$$\Delta V_{OUT3} = \frac{\Delta I_{OUT3}}{4 \times f_C \times C_{OUT3}} + \Delta I_{OUT3} \times ESR = \frac{2.1\ A}{4 \times 50\ kHz \times 100\ \mu F} + 2.1\ A \times 10\ m\Omega = 126\ mV \quad (39)$$

$$V_{OUT3(Ripple)} = \frac{I_{OUT3(Ripple)}}{8 \times f_{SW} \times C_{OUT3}} + I_{OUT3(Ripple)} \times ESR = \frac{0.46\ A}{8 \times 400\ kHz \times 100\ \mu F} + 0.46\ A \times 10\ m\Omega = 6.03\ mV \quad (40)$$

Internal High-Side MOSFET (Buck3TOPFET)

$$P_{BuckTOPFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times D + \left(\frac{V_{IN} \times I_{OUT}}{2}\right) \times (t_r + t_f) \times f_{SW} \quad (41)$$

$$(2.2\ A)^2 \times 0.28\Omega \times 0.36 + \left(\frac{5\ V \times 2.2\ A}{2}\right) \times (20\ ns + 20\ ns) \times 400\ kHz = 0.58\ W \quad (42)$$

Internal Low-Side MOSFET (Buck3LOWFET)

$$P_{BuckLOWERFET} = (I_{OUT})^2 \times r_{DS(on)}(1 + TC) \times (1 - D) + V_F \times I_{OUT} \times (2 \times t_d) \times f_{SW} \quad (43)$$

$$(2.2\ A)^2 \times 0.28\ \Omega \times (1 - 0.36)\ 0.6 \times 2.2\ A \times (2\ x\ 20\ ns) \times 400\ kHz = 0.89\ W \quad (44)$$

8.2.3 Application Curves

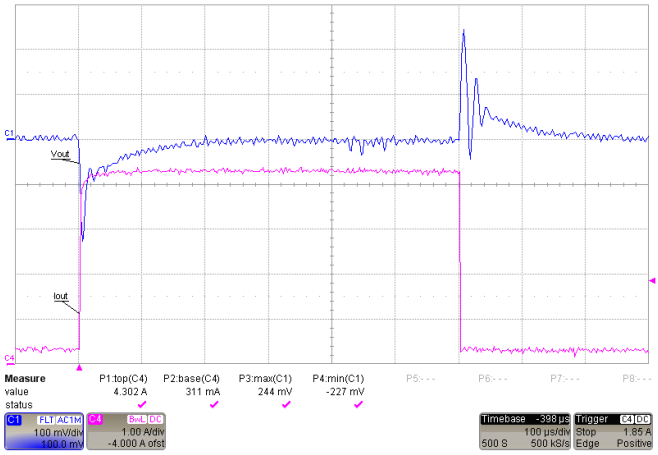


图 20. Load Step Buck 1

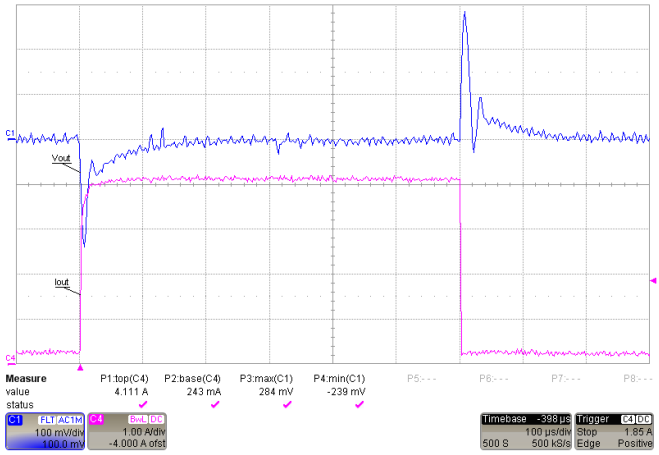


图 21. Load Step Buck 2

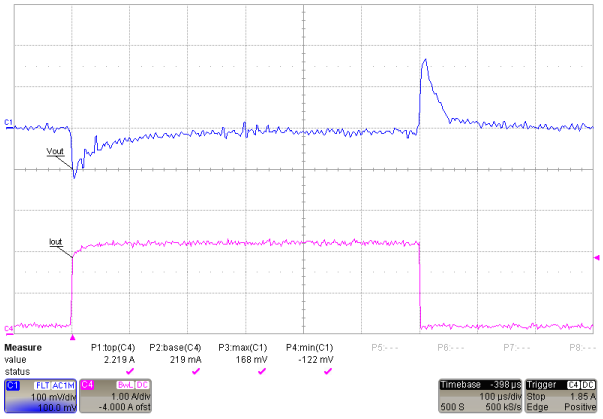


图 22. Load Step Buck 3

9 Power Supply Recommendations

The TPS43340-Q1 device is designed to operate from an input voltage up to 40 V for the buck controllers (Buck1, Buck2). The buck converter (Buck3) accepts input voltages up to 10 V; so in many applications, the output of Buck1 or Buck2 is used to supply it. The linear regulator accepts up to 40 V; however, for power dissipation reasons, TI advises using lower supply voltages. Ensure that the supply for all inputs is well regulated. Furthermore, if the supply voltage in the application is likely to reach negative voltage (for example, reverse battery), a forward diode must be placed at the input of the supply, where GPULL-pin can be used to bypass the diode with an external FET to reduce the voltage drop and power dissipation. For the VIN pin, place a ceramic capacitor or a set of ceramic capacitors close to the pin and add more capacitance as required. Consider capacitance derating for aging, temperature, and DC bias. The PowerPAD package, which offers an exposed thermal pad to enhance thermal performance, must be soldered to the copper landing on the PCB for optimal performance.

- Connect a local decoupling capacitor close to the VSUP pin (supply for Buck3) for proper filtering.
- Connect a local decoupling capacitor close to the VLR1 pin (supply for LDO) for proper filtering.
- Connect a local decoupling capacitor close to the VREG-pin for proper filtering.

10 Layout

10.1 Layout Guidelines

10.1.1 Grounding and PCB Circuit Layout Considerations

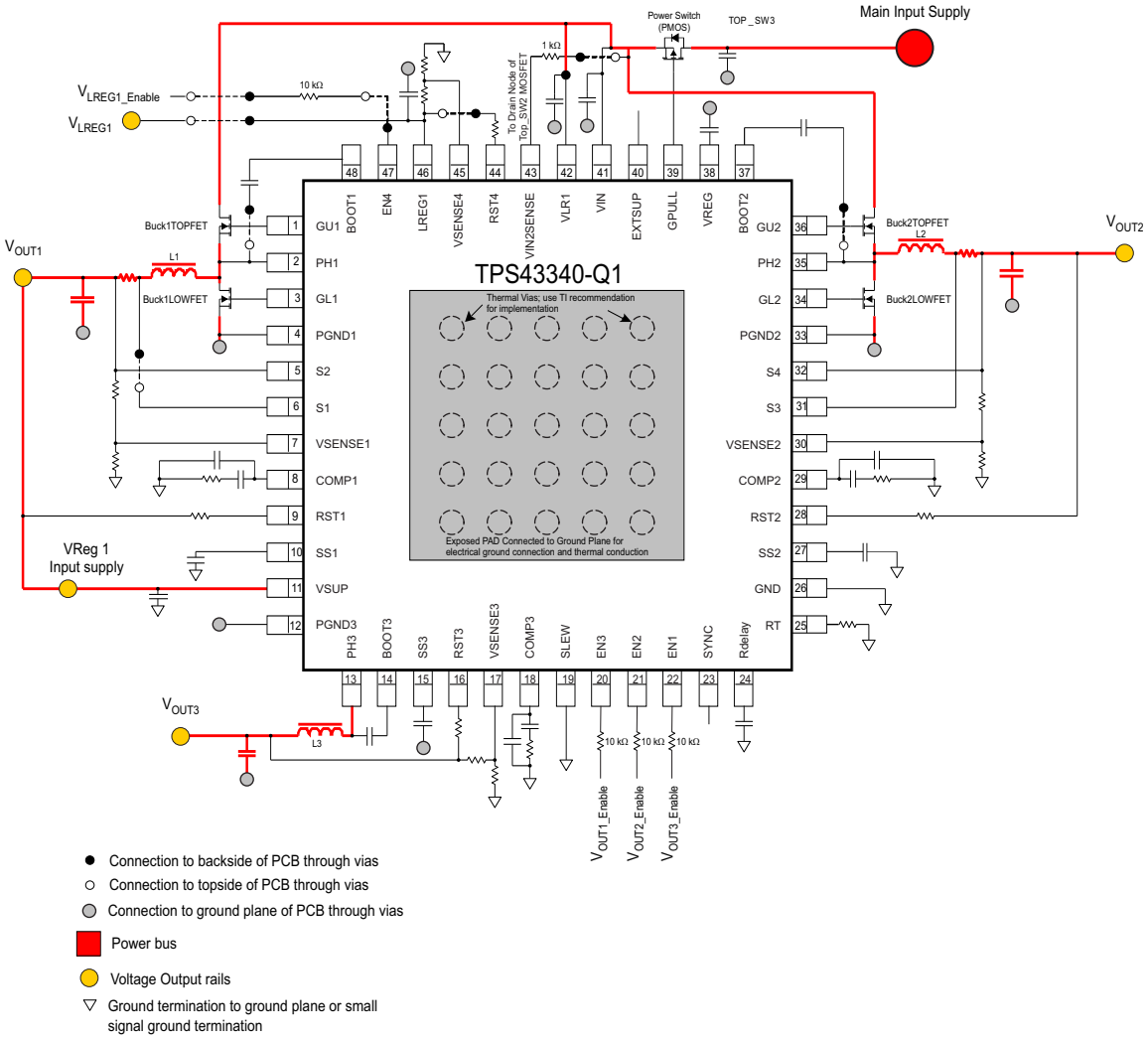
1. Connect the drains of TOP_SW1 and TOP_SW2 together with the +ve terminal of the input capacitor C_{OUT1}. The trace length between these terminals should be short.
2. The Kelvin-current sensing for the shunt resistor should have traces with minimum spacing, routed in parallel with each other. Place any filtering capacitors for noise near the IC pins.
3. Connect the resistor divider for sensing output voltage between the +ve terminal of its respective output capacitor C_{Buck1} or C_{Buck2} or C_{Buck3} and the IC signal ground. Do not route these components or their traces near any switching nodes or high-current traces.

10.1.2 Other Considerations

1. Separate the IC signal ground and power ground terminals (GND and PGNDx) pins. Use a star-ground configuration if connecting to a non-ground plane system. Use tie-ins for the EXTSUP capacitor, compensation network ground, and voltage-sense feedback ground networks to this star ground.
2. Connect a compensation network between the compensation pins and IC signal ground. Connect the oscillator resistor (frequency setting) between the RT pin and IC signal ground. Do not locate these sensitive circuits near the dV/dt nodes; these include the gate drive outputs, phase pins, and boost circuits (bootstrap).
3. Reduce the surface area of the high-current-carrying loops to a minimum by ensuring optimal component placement. Locate the bypass capacitors as close as possible to their respective power and ground pins.

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10.2 Layout Example



(1) The thermal pad is connected to the ground plane for electrical ground connection and thermal conduction.

10.3 Power Dissipation

The power dissipation depends on the MOSFET drive current and input voltage. The drive current is proportional to the total gate charge of the external MOSFET.

10.3.1 Power Dissipation of Buck1 and Buck2 (V_{OUT1} and V_{OUT2})

$$P_{Gate\ drive} = Qg \times V_{REG} \times f_{sw}\ (Watts) \quad (45)$$

Assuming both high and low side MOSFETs are identical in a synchronous configuration, the total power dissipation per buck is

$$P_{Buck1} = 2 \times Qg \times f_{sw} \times V_{REG}\ (Watts) \quad (46)$$

10.3.2 Power Dissipation of Buck Converter Buck3 (V_{OUT3})

10.3.2.1 High-Side Switch

The power dissipation losses are applicable for positive output currents:

$$P_{HS\text{-}CON} = I_{OUT}^{\ 2} \times r_{DS(on)} \times (V_{OUT} / V_{IN})\ (Conduction\ losses) \quad (47)$$

$$P_{HS_SW} = ½ \times V_{SUP} \times I_{OUT} \times (t_r + t_f) \times f_{SW}\ (Switching\ losses) \quad (48)$$

$$P_{HS_Gate} = 1\ nC \times f_{sw}\ (Gate\ drive\ losses,\ valid\ at\ V_{REG} = 5.8\ V,\ V_{SUP} = 4\ V)$$

Power Dissipation (接下页)

$$P_{HS_Total} = P_{HS\text{-}CON} + P_{H_SW} + P_{HS_Gate} \quad (49)$$

10.3.2.2 Low-Side Switch

The power dissipation losses are applicable for positive output currents.

$$P_{LS\text{-}CON} = I_{OUT}^{2} \times r_{DS(on)} \times (1 - V_{OUT} / V_{IN}) \text{ (Conduction losses)} \quad (50)$$

$$P_{LS_SW} = ½ \times V_{SUP} \times I_{OUT} \times (t_r + t_f) \times f_{SW} \text{ (Switching losses)} \quad (51)$$

$$P_{LS_Gate} = 1 \text{ nC} \times f_{sw} \text{ (Gate drive losses, valid at } V_{VREG} = 5.8 \text{ V, } V_{SUP} = 4 \text{ V)} \quad (52)$$

$$P_{LS_DIODE} = 2 \times V_f \times I_{OUT} \times f_{sw} \times t_{dead} \text{ (Low-side body diode losses during dead time)} \quad (53)$$

$$P_{LS_Total} = P_{LS\text{-}CON} + P_{L_SW} + P_{LS_Gate} + P_{LS_DIODE} \quad (54)$$

10.3.2.3 Linear Regulator (LREG1)

$$P_{LREG1} = (V_{VLR1} - V_{LREG1}) \times I_{OUT}$$

where

- V_{OUT} = Output voltage, V_{IN} = Input voltage
- I_{OUT} = Output current, f_{SW} = Switching frequency
- t_r = Rise time of switching node PH3
- t_f = Fall time of switching node PH3
- V_{REG} = FET gate drive voltage
- Vf_diode = Low-side FET diode drop (conduction during dead time) (55)

10.3.2.4 IC Power Consumption

$$P_{IC} = Iq \times V_{IN} \text{ (Watts)} \quad (56)$$

$$P_{Total} = P_{Buck1 \text{ and } Buck2} + P_{HS_Total} + P_{LS_Total} + P_{LREG1} + P_{IC} \text{ (Watts)} \quad (57)$$

表 2. Summary of Equations for Component Selection(1)(2)

PARAMETER OR COMPONENT	Buck1 AND Buck2	Buck3	COMMENTS
Duty cycle D	$D = \frac{V_{OUT}}{V_{IN}}$	$D = \frac{V_{OUT}}{V_{IN}}$	Buck3 is powered from Buck1 or Buck2.
Current-limit sense resistor R_S	$R_S = \frac{0.075}{1.25 \times I_{OUT}\,max}$	Not Applicable	Choose a current limit of 25% more than maximum load.
Inductor selection L	$L = \frac{200}{f_{SW}} \times R_S$	$L = \frac{3.7}{f_{SW}}$	Choose R_S based on the current limit set for the application.
Inductor ripple current	$\Delta I_{L(RIPPLE)} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$	$\Delta I_{L(RIPPLE)} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$	Typically the ± inductor ripple current is 25% of maximum load current.
Output capacitor C_{OUT}	$C_{OUT} = \frac{\Delta I_{OUT}}{4 \times GBW \times \Delta V_{OUT}}$	$C_{OUT} = \frac{\Delta I_{OUT}}{4 \times GBW \times \Delta V_{OUT}}$	Also consider that the ESR of the output capacitor influences the output-voltage ripple due to load steps.
Input capacitor C_{IN}	$C_{IN} = \frac{0.25 \times \Delta I_{OUT\ MAX}}{f_{SW} \times \Delta V_{IN}}$	$C_{IN} = \frac{0.25 \times \Delta I_{OUT\ MAX}}{f_{SW} \times \Delta V_{IN}}$	Base the input-capacitor value on the input-voltage ripple desired.
Soft-start C_{SS}	$C_{SS} = \frac{1\,\mu A \times \Delta t}{0.8}$	$C_{SS} = \frac{1\,\mu A \times \Delta t}{0.8}$	Choose the soft-start time required, Δt, and then calculate C_{SS}.
Bootstrap capacitor CBoot	$C_{BOOT} = \frac{Q_g}{\Delta V}$	$C_{BOOT} = \frac{Q_g}{\Delta V}$	Choose based on the desired amount of ripple based on FET gate charge and operating V_{IN}.

(1) $K_{CFB} = 0.125 / R_{SENSE}$
(2) ß = V_{REF} / V_{OUT}

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Power Dissipation (接下页)

表 2. Summary of Equations for Component Selection[00] (接下页)

PARAMETER OR COMPONENT	Buck1 AND Buck2	Buck3	COMMENTS
Compensation resistor for GBW	$R3 = \frac{GBW \times 2\pi \times C_{OUT}}{gm \times K_{CFB} \times \beta}$	$R3 = \frac{GBW \times 2\pi \times C_{OUT}}{gm \times Gm3 \times \beta}$	To determine resistor R3, assume GBW ≈ f_{sw} / 5 to f_{sw} / 20.
Compensation capacitor for zero	$C1 = \frac{1}{2\pi \times R3 \times 0.1 \times GBW}$	$C1 = \frac{1}{2\pi \times R3 \times 0.1 \times GBW}$	C1 can be also increased 2× for faster small-signal settling at the expense of large step response (slew rate on COMPx).
Compensation capacitor for second pole	$C2 = \frac{1}{\pi \times f_{SW} \times R3}$	$C2 = \frac{1}{\pi \times f_{SW} \times R3}$	The value of C2 is also critical for buffering the noise on the COMPx pin, and so the value of capacitance is a trade-off between noise immunity and phase margin.
Pole at low frequency with high dc gain	$f_{P1} = \frac{1}{2\pi \times C1 \times R_{OUT_OTA}}$	$f_{P1} = \frac{1}{2\pi \times C1 \times R_{OUT_OTA}}$	R_{OUT_OTA} = 1 MΩ minimum
Zero at control-loop pole related to output filter LC	$f_{Z1} = \frac{1}{2\pi \times C1 \times R3}$	$f_{Z1} = \frac{1}{2\pi \times C1 \times R3}$	Place zero at 0.05 to 0.1 × GBW (see comment on C1 above).
Second pole for type 2a	$f_{PZ} = \frac{1}{2\pi \times C2 \times R3}$	$f_{PZ} = \frac{1}{2\pi \times C2 \times R3}$	Place the second pole at or below half of the switching frequency f_{sw}, observing distance to GBW.

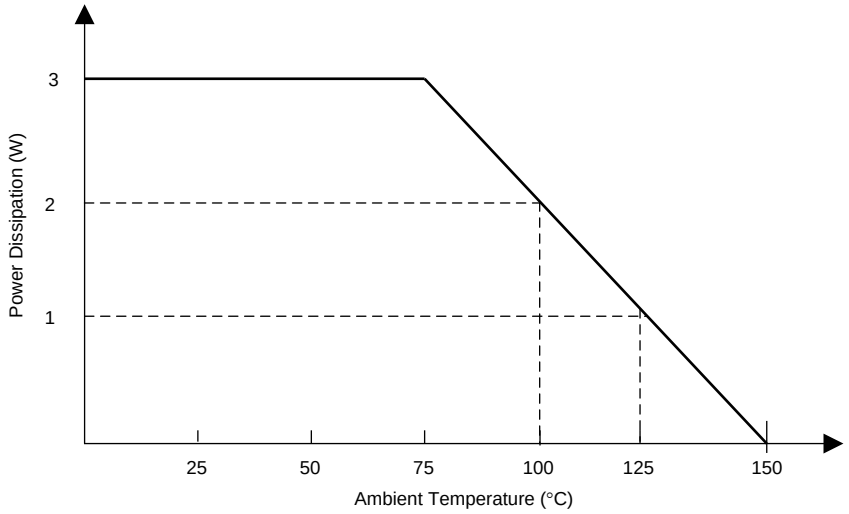


图 23. Power Dissipation Derating Profile Based on High-K JEDEC PCB

10.4 Thermal Considerations

The TPS43340-Q1 device is protected from overtemperature using an internal thermal shutdown circuit. If the die temperature exceeds the thermal shutdown threshold (for example, due to fault conditions such as a short circuit at the gate drivers or VREG), the device turns off, and restarts when the temperature has fallen by the hysteresis.

Thermal Considerations (接下页)

表 3. Low-Power-Mode Operation of the System

SETUP	SYNC	QUIESCENT CURRENT (TYP), NO LOAD, 25°C	DESCRIPTION
Buck1 or Buck2 in LPM mode	Low	Approximately 30 µA	Configuration for ignition-off applications with standby functionality
Buck1 and Buck2 in LPM mode		Approximately 35 µA	
Buck1 or Buck2 in PWM mode	High	Approximately 30-40 mA	Including switching currents
Buck1 and Buck2 in PWM mode		Approximately 30-40 mA	Including switching currents
LREG1	N/A	Approximately 50 µA	Configuration for ignition-off applications with standby functionality
LREG1 and Buck1 or Buck2 in LPM mode	Low	Approximately 55 µA	
LREG1 and Buck1 and Buck2 in LPM mode		Approximately 60 µA	
LREG1 and Buck1 or Buck2 in PWM mode	High	30-40 mA	Including switching currents
LREG1 and Buck1 and Buck2 in PWM mode		30-40 mA	Including switching currents

The synchronous buck converter Buck3 with the integrated FETs does not support LPM. Turning on Buck3 forces the system to operate in normal mode, and the quiescent current consumption increases.

表 4. Input Voltage and Low-Power-Mode Operation

INPUT VOLTAGE AT VIN PIN	LOAD CURRENT OF LREG1	CHARGE PUMP OF LREG1	BUCK CONTROLLERS Buck1 AND Buck2	VIN QUIESCENT CURRENT (TYP), NO LOAD, 25°C	DESCRIPTION
V_{IN} > 9 V	N/A	OFF	LPM allowed	55 µA	Lowest current consumption of the system at VIN (LREG1, Buck1 and Buck2 enabled), typical ignition-off stay-alive mode with up to three voltage rails active
7.5 V < V_{IN} < 9 V	< 2 mA	OFF	LPM allowed	55 µA	
	> 6 mA	ON	LPM allowed	260 µA	
V_{IN} < 7.5 V	N/A	ON	LPM not allowed	2.6 mA	If VIN drops below 7.5 V, the buck controllers Buck1 and Buck2 leave low-power mode (LPM) and start PWM operation, quiescent current of the system increases. For applications that use the LREG1 only as the standby keep-alive supply, quiescent current is still low.

Monitoring of the threshold for the charge pump of the low quiescent linear regulator LREG1 to be turned on occurs at the VIN pin. If using LREG1 as post regulator with an input voltage V_{LR1} of less than 7.5 V, the charge pump still stays off if operating within the required conditions for V_{IN} and the load current. The sampling interval for the foregoing voltage thresholds at the VIN pin is typically 60 µs.

10.4.1 Phase Configuration

The IC configuration has buck controller 1 and buck controller 2 switching 180 degrees out of phase. Buck converter (Buck3) switches in phase with buck controller 1.

CONFIGURATION	Buck1	Buck2	Buck3	DESCRIPTION
Phase	0º	180º	0º	Buck1 and Buck2 out of phase, Buck1 and Buck3 in phase

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11 器件和文档支持

11.1 器件支持

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11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *《TPS4334xEVM 评估模块》*，SLVU463
- *《TPS43340-Q1 系列设计清单》*，SLVA614

11.3 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS43340QPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	43340Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

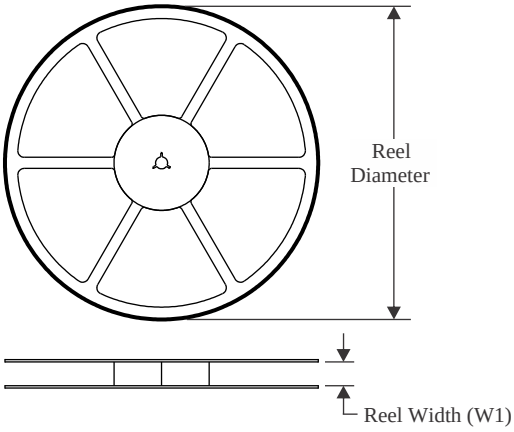
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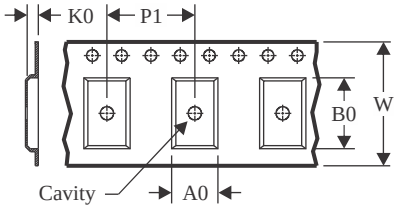
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

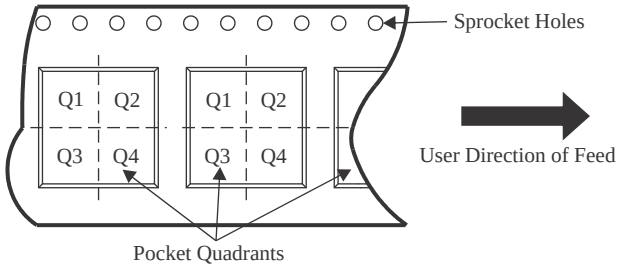


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

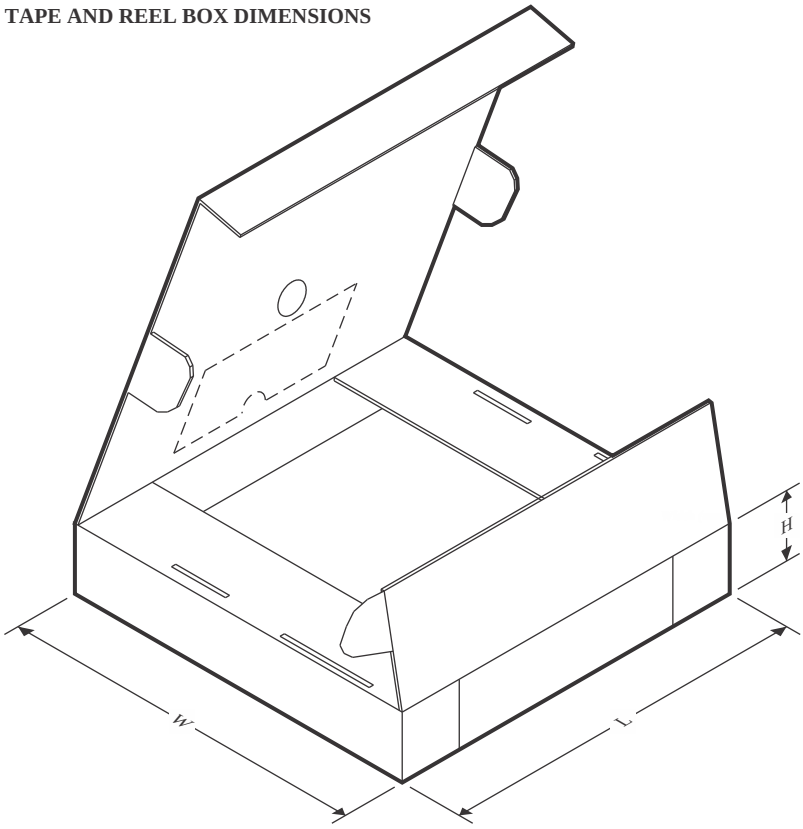
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43340QPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43340QPHPRQ1	HTQFP	PHP	48	1000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

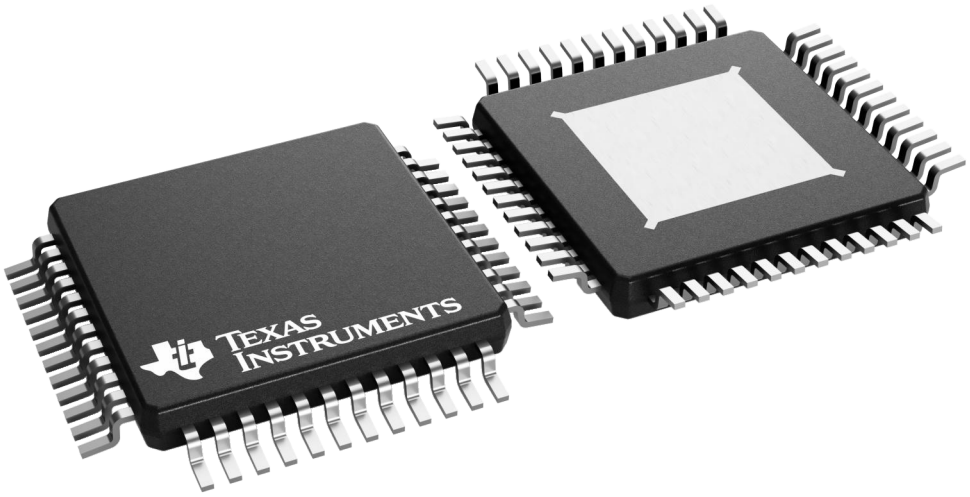
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



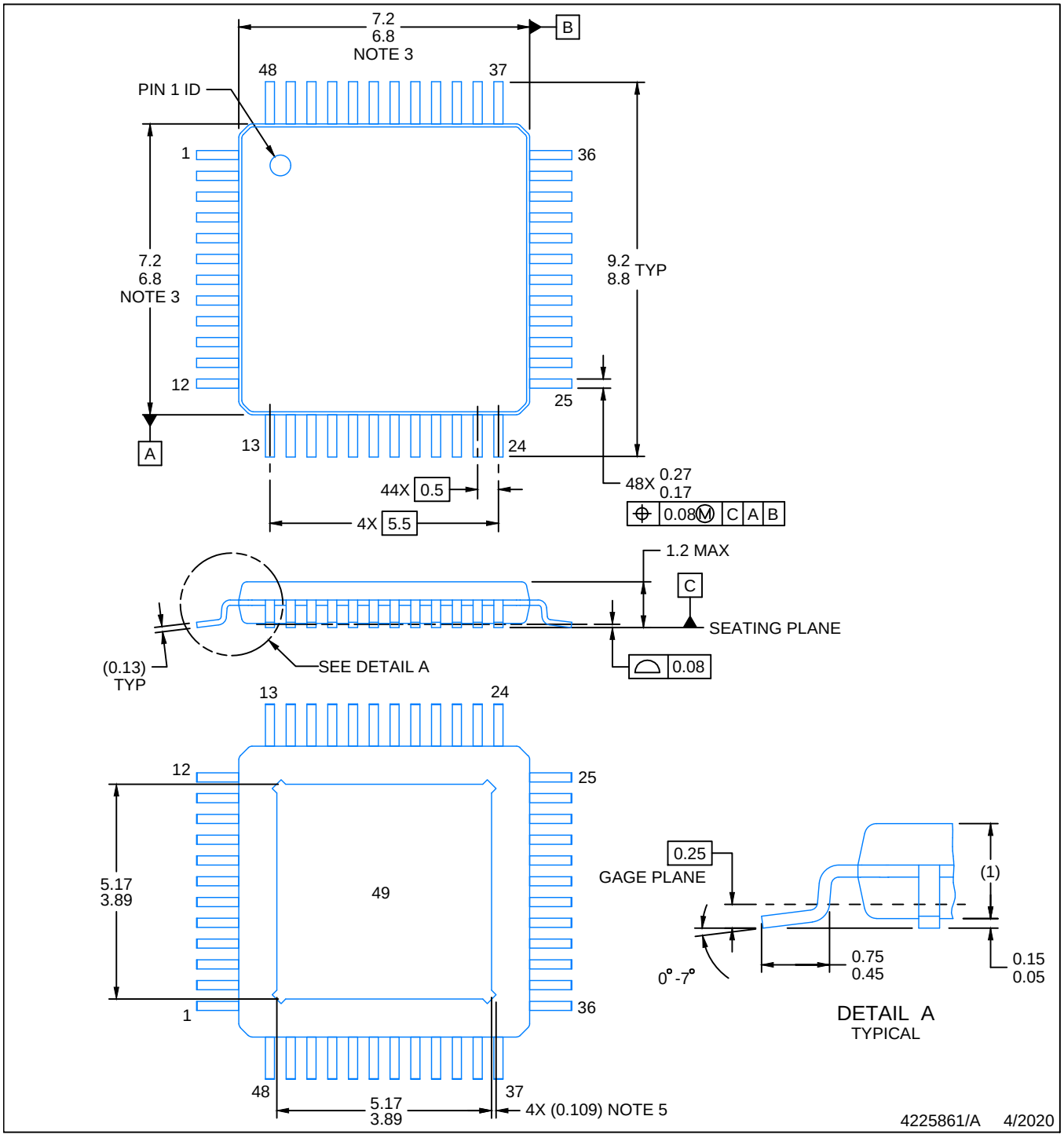
4226443/A

PACKAGE OUTLINE

PHP0048G

PowerPAD™ HTQFP - 1.2 mm max height

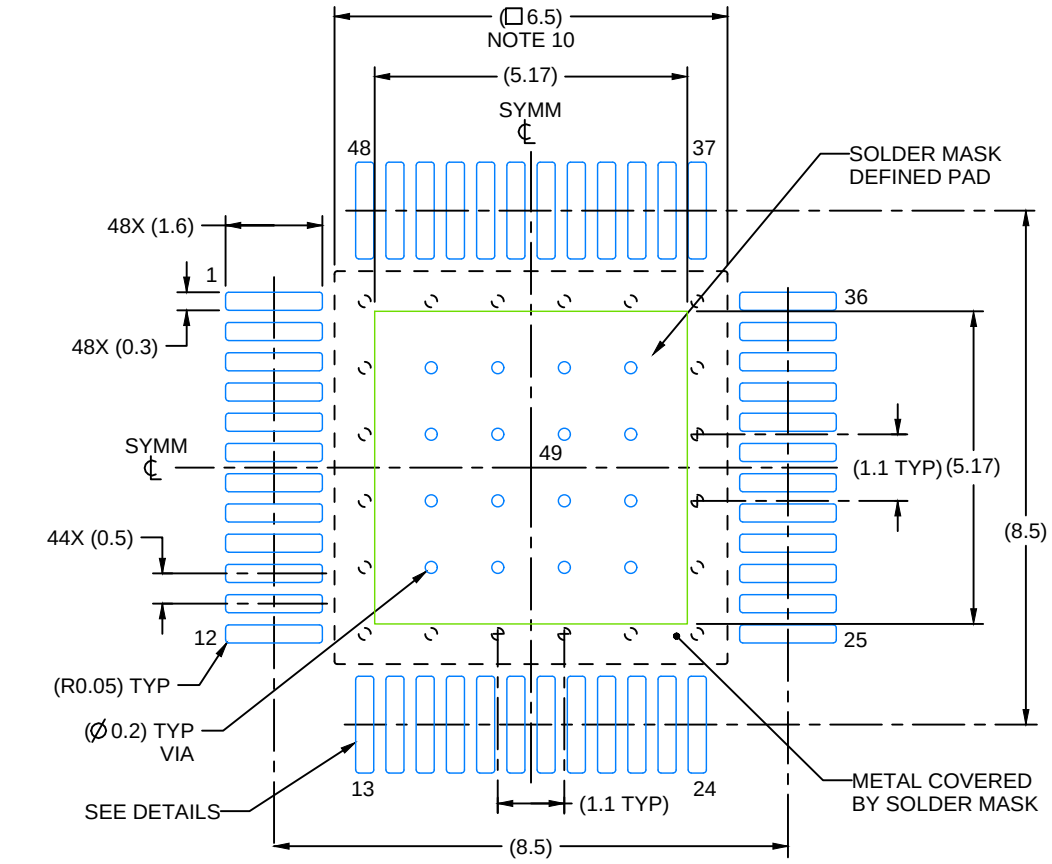
PLASTIC QUAD FLATPACK



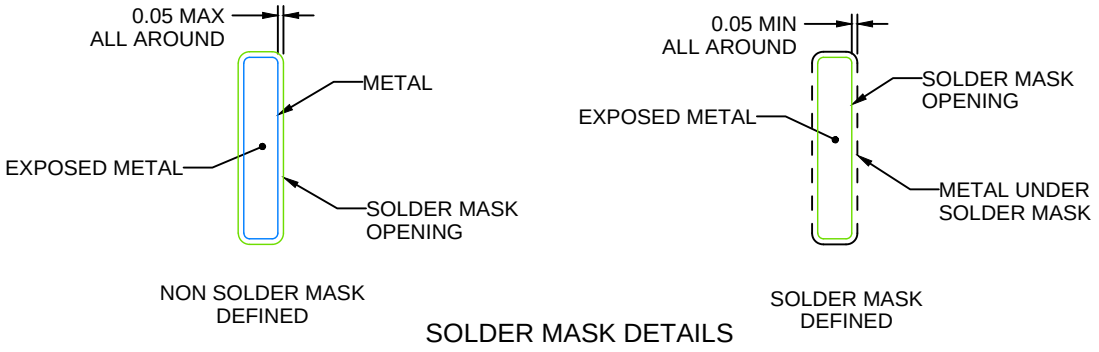
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

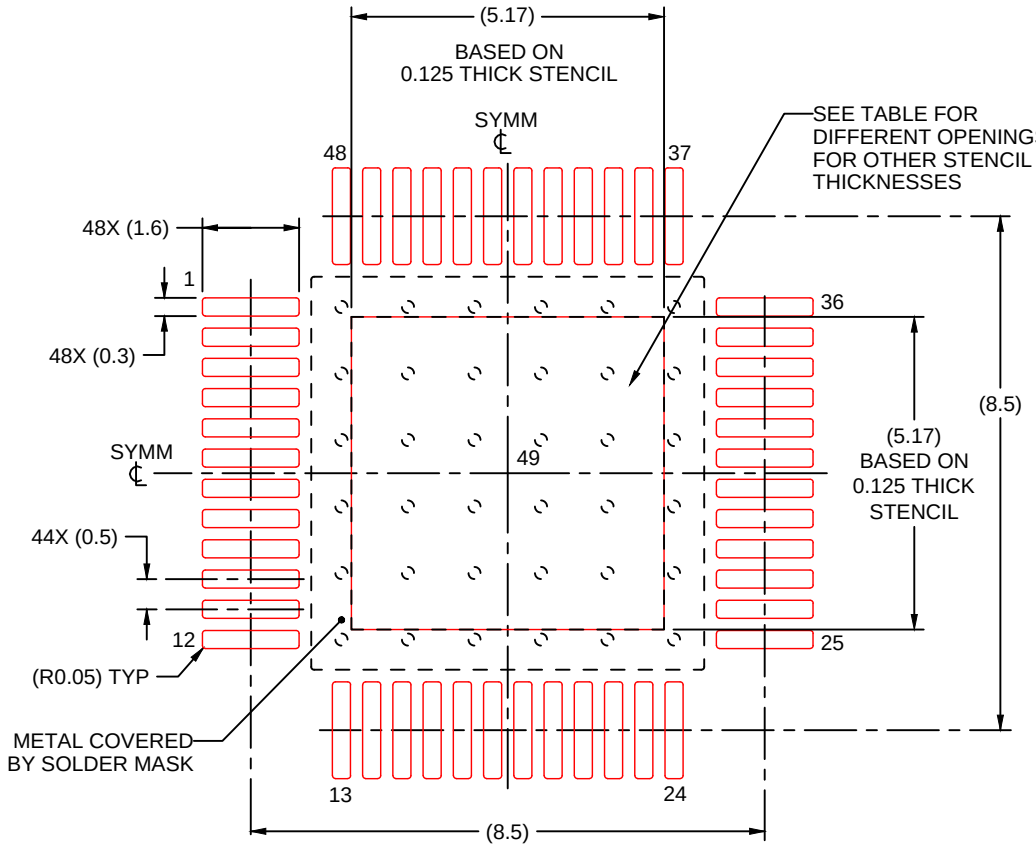


SOLDER MASK DETAILS

4225861/A 4/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4225861/A 4/2020

NOTES: (continued)

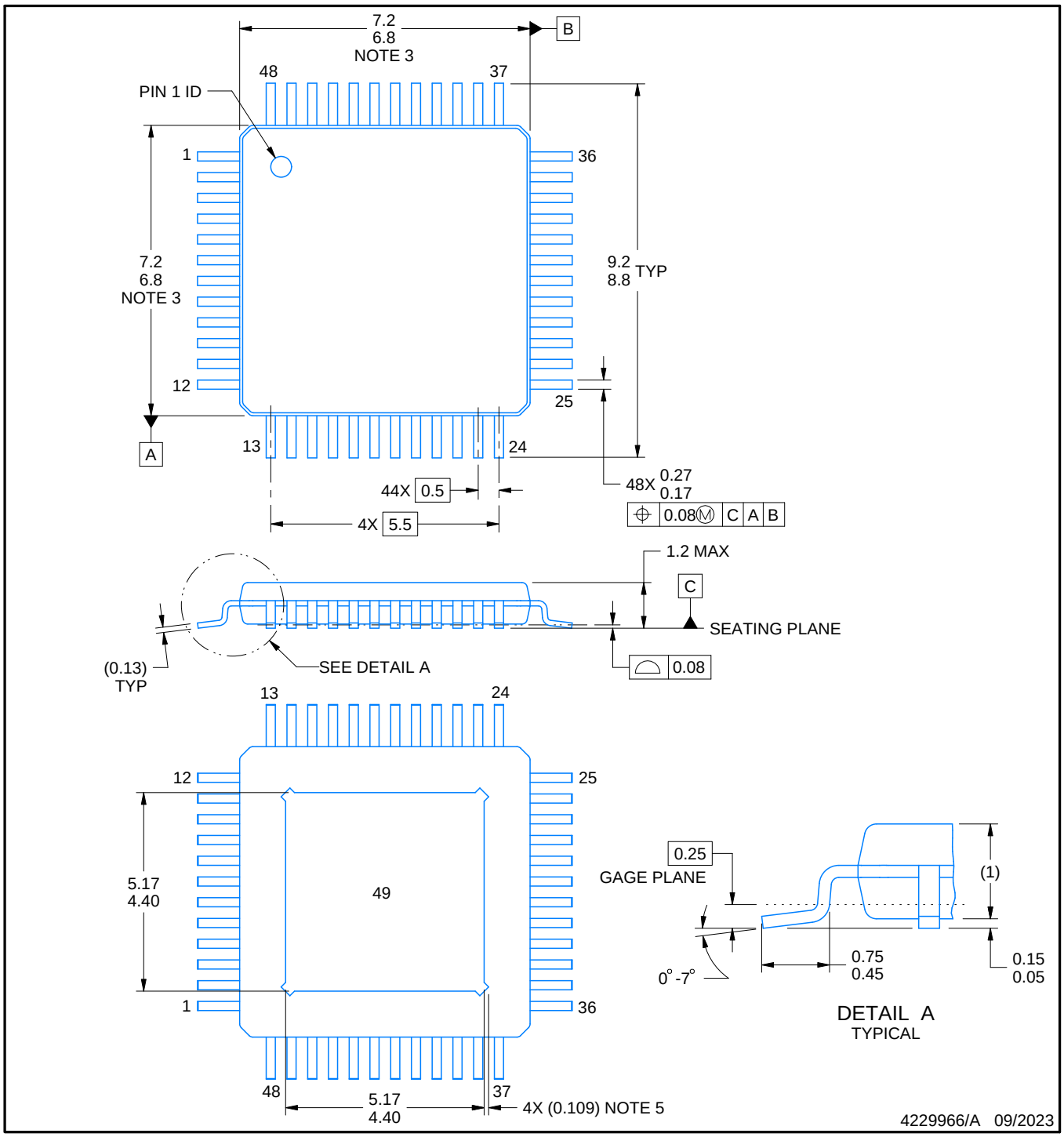
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PHP0048N

PowerPAD™ HTQFP - 1.2 mm max height

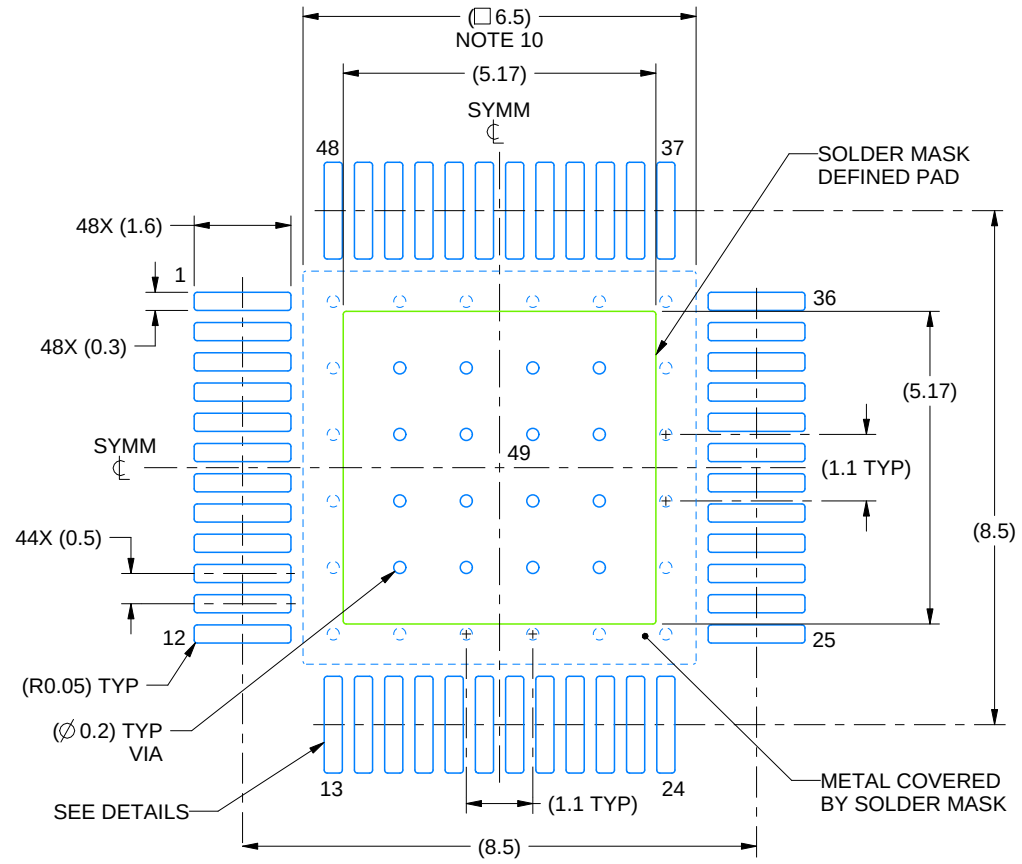
PLASTIC QUAD FLATPACK



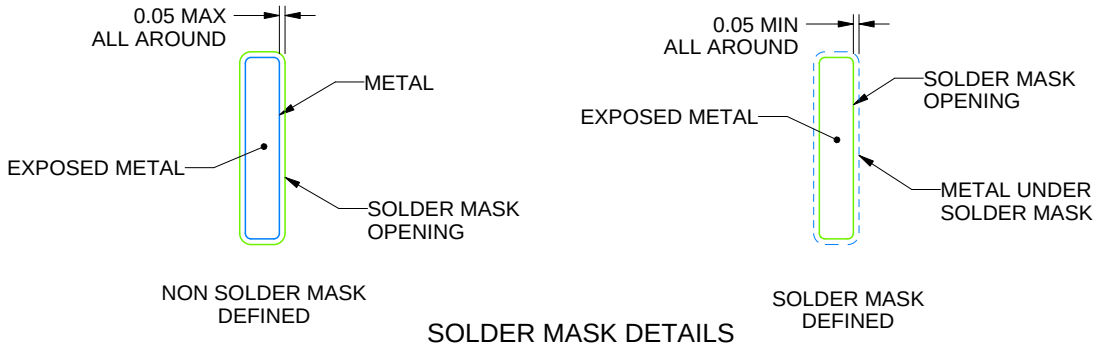
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

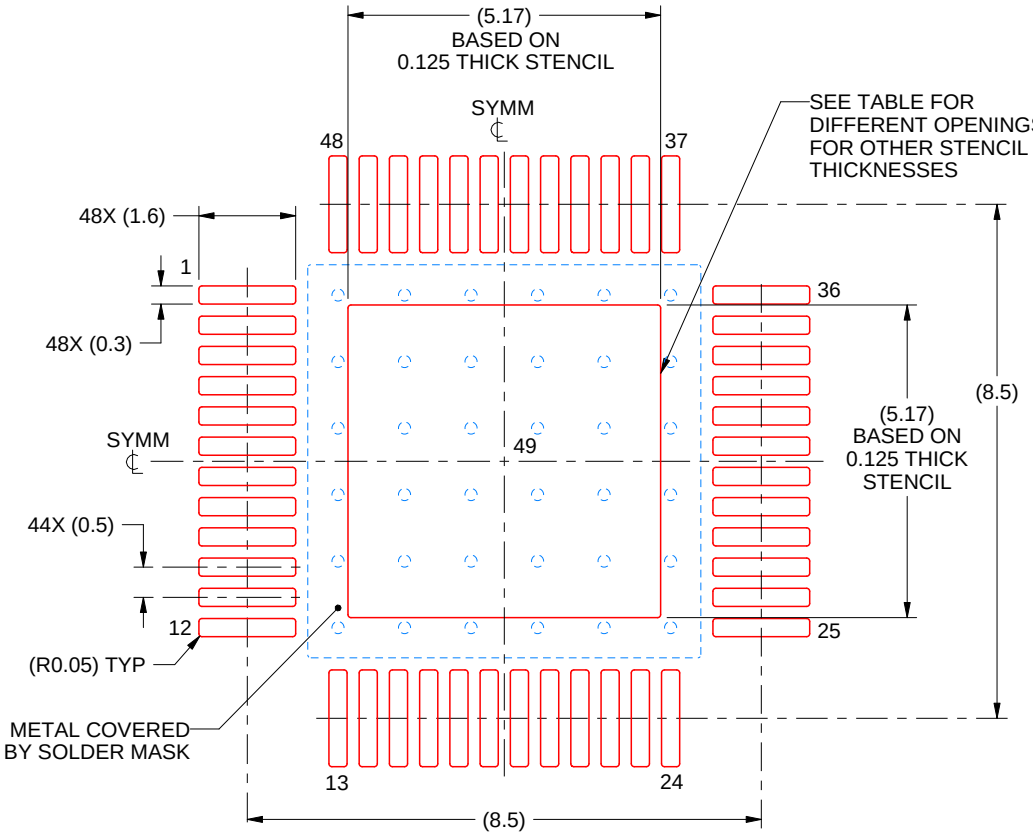


SOLDER MASK DETAILS

4229966/A 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	5.78 X 5.78
0.125	5.17 X 5.17 (SHOWN)
0.150	4.72 X 4.72
0.175	4.37 X 4.37

4229966/A 09/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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