SONY

CXK582000TM/YM/M -85LL/10LL

262144-word × 8-bit High Speed CMOS Static RAM *Preliminary*

For the availability of this product, please contact the sales office.

Description

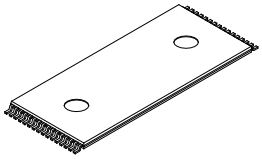
The CXK582000TM/YM/M is a high speed CMOS static RAM organized as 262144-words by 8 bits.

A polysilicon TFT cell technology realized extremely low stand-by current and higher data retention stability.

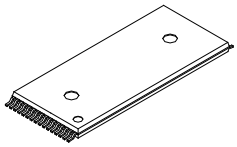
Special feature are low power consumption and high speed and board package line-up.

The CXK582000TM/YM/M is a suitable RAM for portable equipment with battery back up.

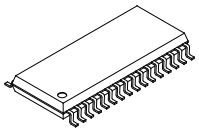
CXK582000TM
32 pin TSOP (Plastic)



CXK582000YM
32 pin TSOP (Plastic)



CXK582000M
32 pin SOP (Plastic)



Features

- Fast access time (Access time)
  - -85LL 85ns (Max.)
  - -10LL 100ns (Max.)
- Low standby current 40µA (Max.)
- Low data retention current 24µA (Max.)
- Single +5V supply: 4.5V to 5.5V.
- Low voltage date retention : 2.0V (Min.)
- Broad package line-up
  - CXK582000TM/YM 8mm × 20mm 32 pin TSOP Package
  - CXK582000M 525mil 32 pin SOP Package

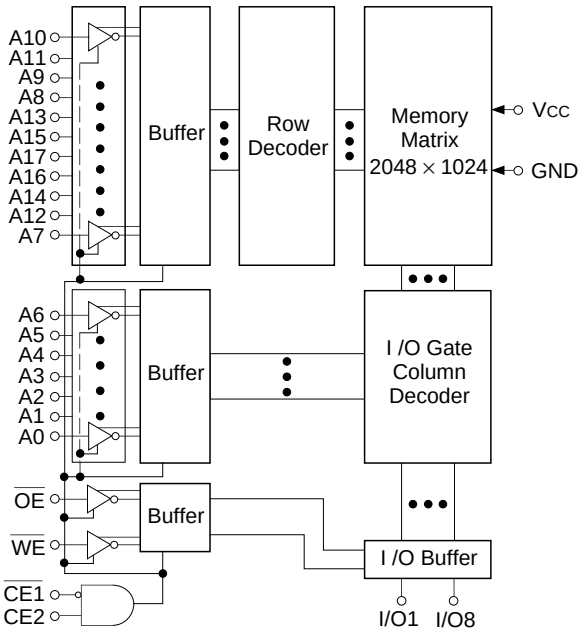
Function

262144 word x 8 bit static RAM

Structure

Silicon gate CMOS IC

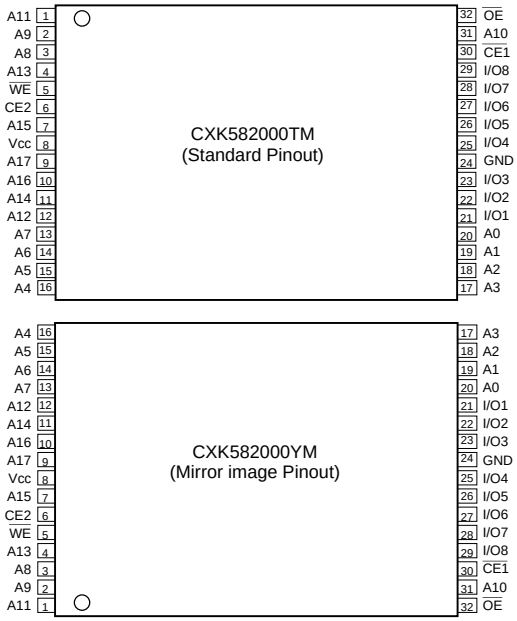
Block Diagram

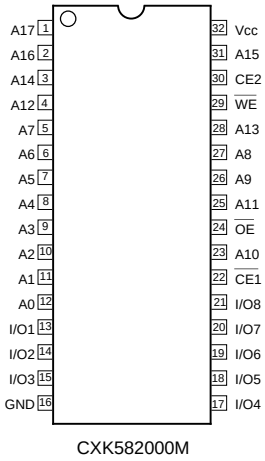


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E94234-ST

Pin Configuration (Top View)





CXK582000M

Pin Description

Symbol	Description
A0 to A17	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5∗ to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	–0.5∗ to V_{CC} + 0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

∗ V_{IN}, $V_{I/O}$ = –3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

×: “H” or “L”

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3∗	—	0.8	V

∗ V_{IL} = –3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC Characteristics (V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.∗	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		–1	—	+1	µA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		–1	—	+1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA		—	7	15	mA
Average operating current	I_{CC2}	Min. cycle duty = 100% I_{OUT} = 0mA	-85LLX	—	45	80	mA
			-10LLX	—	40	70	
	I_{CC3}	Cycle time 1µs duty = 100% I_{OUT} = 0mA $\overline{CE1} \leq 0.2V$ CE2 ≥ Vcc – 0.2V $V_{IL} \leq 0.2V$ $V_{IH} \geq$ Vcc – 0.2V		—	12	24	mA
Standby current	I_{SB1}	CE2 ≤ 0.2V or $\overline{CE1}$ ≥ Vcc – 0.2V, CE2 ≥ Vcc – 0.2V	0 to +70°C	—	—	40	µA
			0 to +40°C	—	—	8	
			+25°C	—	1.4	4	
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.6	3	mA
Output high voltage	V_{OH}	I_{OH} = –1.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 1.0mA		—	—	0.4	V

∗ V_{CC} = 5V, Ta = 25°C

I/O capacitance (Ta = 25°C, f = 1MHz)

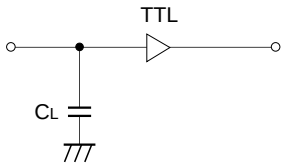
Item	Symbol	Test conditons	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• **AC test conditions** (V_{CC} = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 2.2V
Input pulse low level	V_{IL} = 0.8V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	C_L* = 100pF, 1TTL



* C_L includes scope and jig capacitances.

• **Read cycle** ($\overline{WE}$ = "H") (Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	85	—	100	—	ns
Address access time	t_{AA}	—	85	—	100	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	85	—	100	ns
Chip enable access time (CE2)	t_{CO2}	—	85	—	100	ns
Output enable to output valid	t_{OE}	—	45	—	50	ns
Output hold from address change	t_{OH}	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}, t_{LZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}, t_{HZ2}*	—	25	—	35	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	25	—	35	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

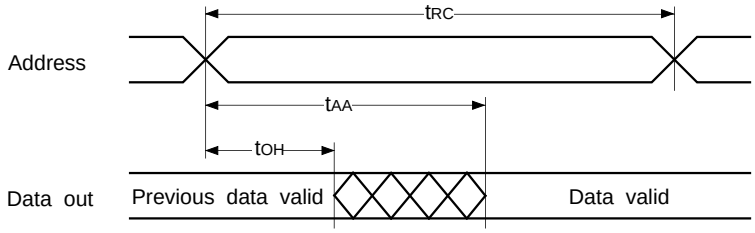
• **Write cycle** (Ta = 0 to +70°C)

Item	Symbol	-85LL		-10LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	85	—	100	—	ns
Address valid to end of write	t_{AW}	65	—	70	—	ns
Chip enable to end of write	t_{CW}	65	—	70	—	ns
Data to write time overlap	t_{DW}	35	—	45	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	5	—	5	—	ns
Output active from end of write	t_{OW}	10	—	10	—	ns
Write to output in high Z	t_{WHZ}*	—	25	—	30	ns

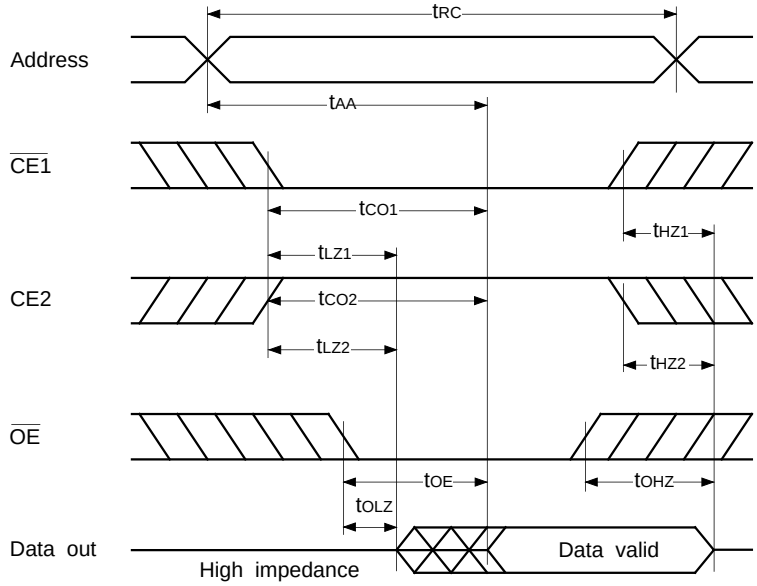
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

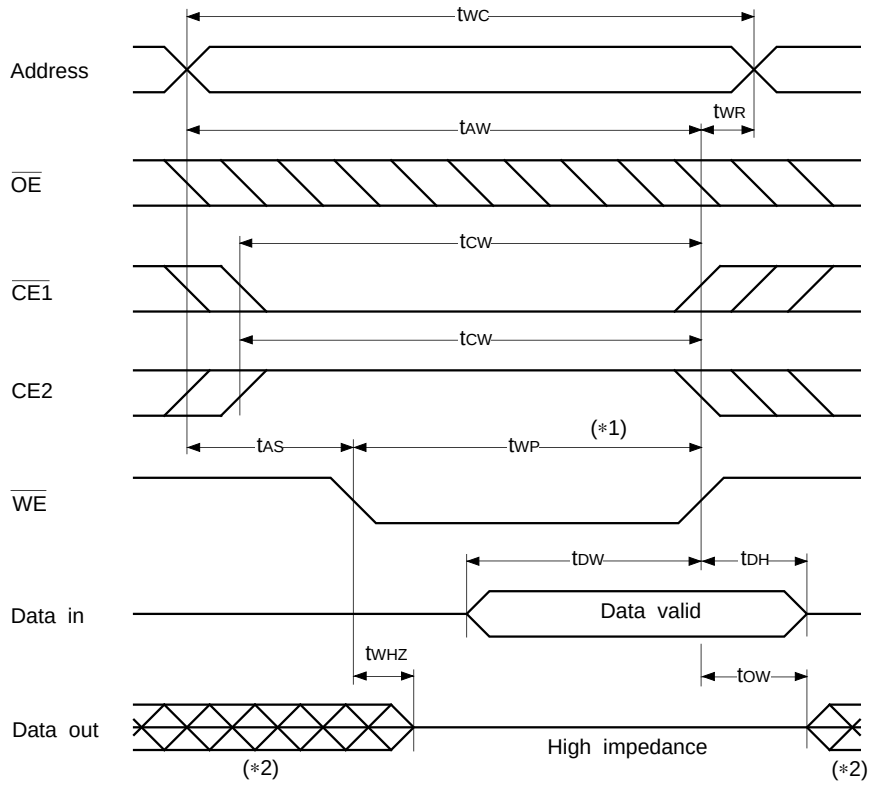
• Read cycle (1) : $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



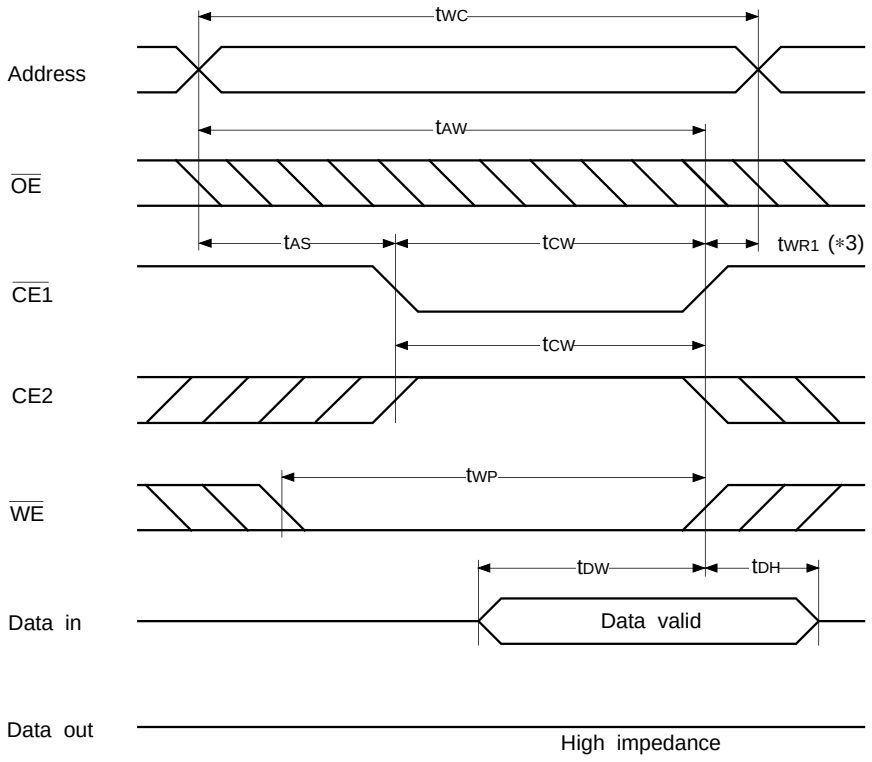
• Read cycle (2) : $\overline{WE}$ = V_{IH}



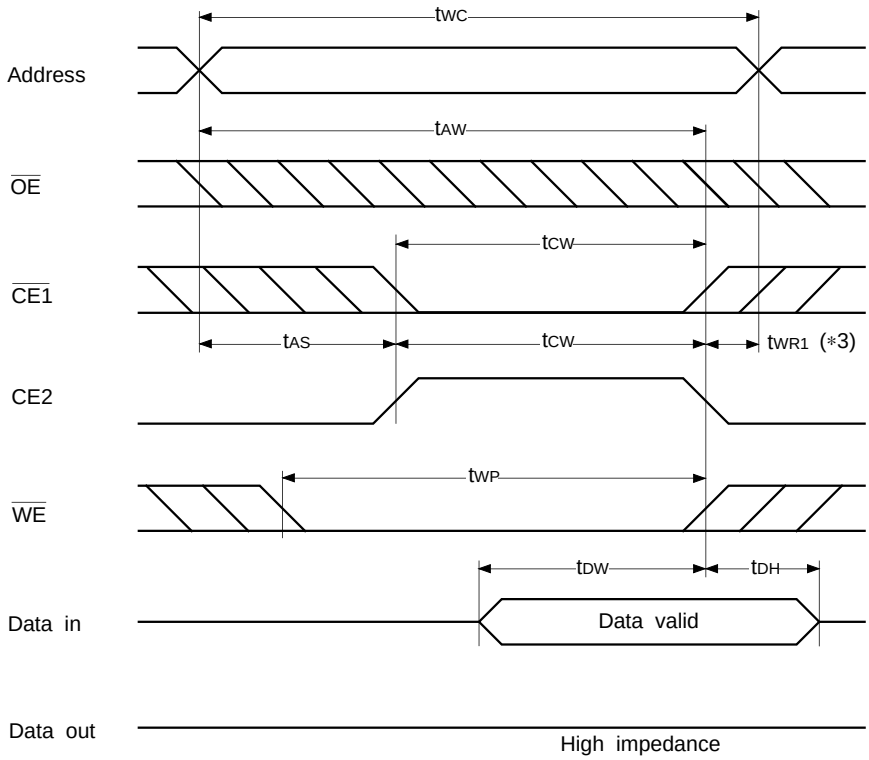
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



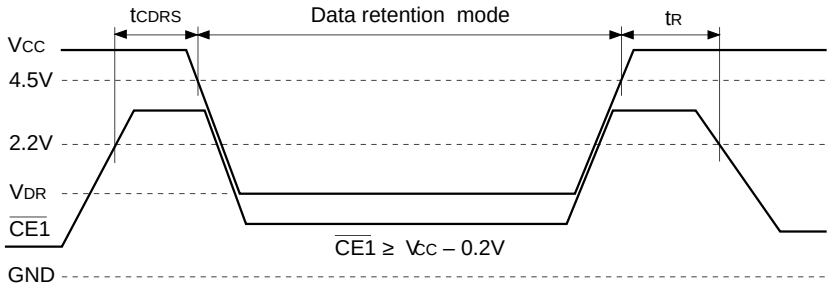
∗1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

∗2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

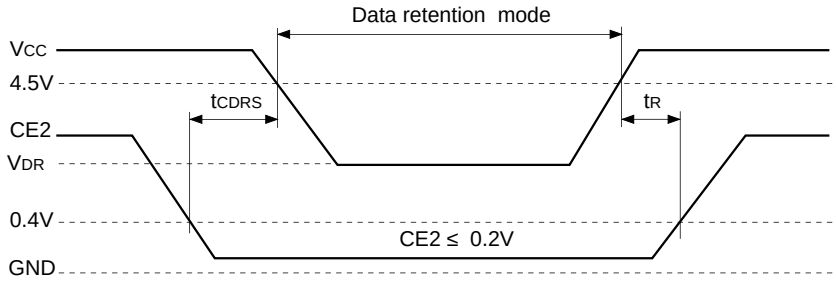
∗3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data retention waveform

• Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



• Low supply voltage data retention waveform (2) (CE2 control)



Data Retention Characteristics (Ta = 0 to +70°C)

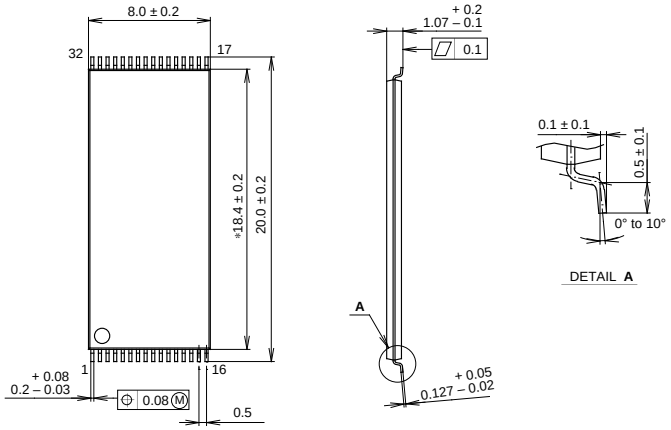
Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*		2.0	—	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V*1	0 to +70°C	—	—	24	µA
			0 to +40°C	—	—	4.8	
			+25°C	—	0.8	2.4	
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V*		—	1.4	40	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ms

* $\overline{CE1}$ ≥ Vcc – 0.2V, CE2 ≥ Vcc – 0.2V ($\overline{CE1}$ control) or CE2 ≤ 0.2V (CE2 control)

Package Outline Unit: mm

CXK582000TM

32PIN TSOP (I) (PLASTIC)



NOTE : *NOT INCLUDE MOLD FINS.

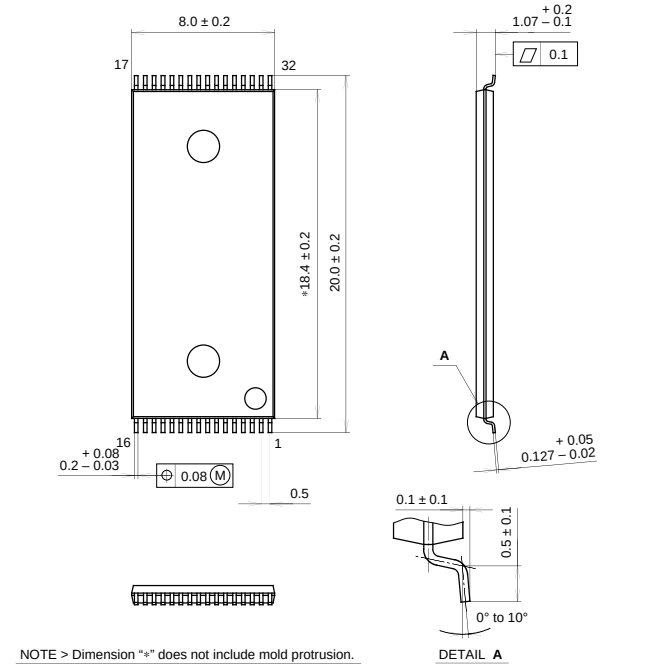
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01
EIAJ CODE	TSOP032-P-0820-A
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	———

CXK582000YM

32PIN TSOP (PLASTIC)



NOTE > Dimension "*" does not include mold protrusion.

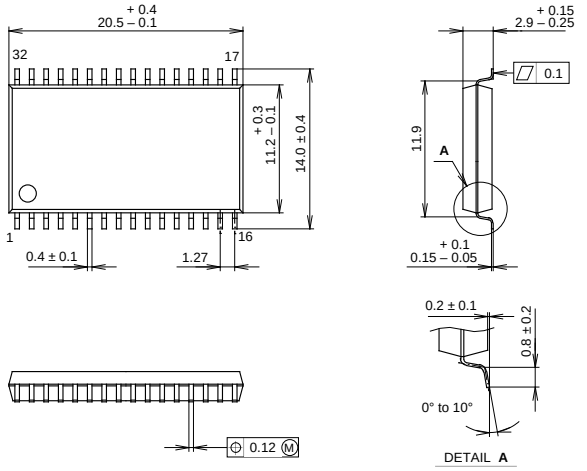
PACKAGE STRUCTURE

SONY CODE	TSOP-32P-L01R
EIAJ CODE	TSOP032-P-0820-B
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g

CXK582000M

32PIN SOP (PLASTIC) 525mil



PACKAGE STRUCTURE

SONY CODE	SOP-32P-L02
EIAJ CODE	*SOP032-P-0525-A
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————