PM0018
Quick reference manual

ST7 Flash programming

Introduction

This quick reference manual is intended for users of ST7 Flash microcontrollers. It is a central source for all device-specific data related to Flash programming for the following documents:

- Flash programming reference manual
- ICC protocol reference manual

The latest document revisions can be obtained on-line at http://www.st.com.

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1 Device specific information

1.1 Flash technology types

Three Flash technologies are available in the ST7 family with different programming methods. Each ST7 Flash microcontroller is associated with one of these three technologies as shown in *Table 1: ST7 Flash microcontroller types*.

- XFlash (Extended): Flash memory based on a EEPROM technology
- HDFlash (High Density): Flash memory based on Flash technology
- CFlash (ST72Cxxx): Flash memory based on a EEPROM technology (see AN1179 for more details)

For further information on XFlash and HDFlash, refer to the Flash programming reference manual.

Table 1. ST7 Flash microcontroller types

ST7 Flash families	Flash technology	ST7 devices	Programming methods	
ST72Fxxx	XFlash	ST7FLITEx, ST7FDALI, ST7FLx ST72F26x, ST72F34x	ICP	IAP
	HDFlash	ST72F32x/F521, ST72F561, ST72F361 ST72F60x, ST72F61x, ST72F62x, ST72F63x, ST72F63Bx,ST72F65, ST72FHUB, ST7FSCR, ST7FMC		
ST72Cxxx	CFlash	ST72C104, ST72C215, ST72C216, ST72C254 ST72C124, ST72C314, ST72C334 ST72C171	ISP	

1.2 RC calibration value addresses

Table 2 holds the addresses of the RC calibration values in the event of removal of readout protection. The full procedure of restoring RC calibration values is described in the Flash programming reference manual. This procedure applies only to the devices listed in the following table. For the other devices, the RC calibration values are not lost if the readout protection is removed.

Table 2. List of RC calibration value addresses

Device	RCCR0	RCCR1
ST7FLITE0/ST7FL0	0xF960	0xF961
ST7FLITE1	0xDEE0	0xDEE1
ST7FLITE2	0xDEE0	0xDEE1

1.3 Implemented ICC features

Table 3 defines the implemented ICC features and their main characteristics for each ST7 device. The data mentioned in this table is described in detail in the ICC protocol reference manual.

Description of legends for *Table 3*

ICC monitor: Three different ICC monitors can be implemented: basic (for ST7 with HDFlash and small XFlash), medium (for ST7 ROM) and advanced (for ST7 XFlash with debug module). Refer to the ICC protocol reference manual for more details.

ICC mode entry: Different methods exists for entering ICC mode. Refer to the ICC protocol reference manual for more details.

IAP:IAP is not available on 4K HDFlash versions.

ICD: ICD can be managed with or without a debug module, refer to the ICC protocol reference manual for more details

DM: The Debug Module (DM) is an ST7 hardware peripheral able to manage instruction stepping, complex breakpoints and abort for ICD development tools. The ST72F325, ST7FSuperlite, ST7FLite2 and ST7FHUB Debug Modules do not feature the WP bit capability and the register protection when MTR=0. Refer to the ICC protocol reference manual for more details.

Ext clock: If this number of pulses is generated, the ST7 does not take into account the option byte configuration stored in the Flash memory, and an external clock has to be provided. In this case, the microcontroller configuration corresponds to the factory default option byte values, see product datasheet for more details. Note that in this mode, reserved Flash locations (which may contain internal oscillator calibration data for example) are not write protected, and could be corrupted if you program the device using a wrong address.

Caution: To know on which pin the external clock must be provided please refer to the section related to the ICC interface in the product datasheet.

Appli clock: If this number of pulses is generated, the ST7 takes into account the option byte configuration (except the watchdog which is always software in this condition). In this case, be sure that the selected clock source is available in the application (see product datasheet for more details).
Note that in this mode, reserved Flash locations are write protected, so this mode is safer than external clock mode.

Table 3. Implemented ICC features in ST7 devices

Devices	ICC monitor	Embedded ICC applications					ICC mode entry				
							Window type	Pulse			
					ICD			Pulse counter reset pin	Pin	Number	
		ICP	IAP	ICT		DM				Ext. clock	Appli clock
ST7FLITE0/ST7FL0, ST7FLITES2/S5(1)	basic	X	X	X	X		Controlled	ICCCLK (2)	ICCDATA	35	38
ST7FLITE2/1/ST7DALI	advanced	X	X	X	X	1					
ST7FLITE4M/3/1B, ST7FL3/1B	advanced	X	X	X	X	1					38(3)
ST7FLITEUS(4), ST7LITEU0	advanced	X	X	X	X	1					38 (5)
ST72F34x (6)	advanced	X	X	X	X	1		ICCSEL (7)			38
ST72F26x	advanced	X	X	X	X						38 (8)
ST7226x(9)	medium			X							38
ST72F561/F361	basic	X	X	X	X						
ST7FHUB	basic	X	X	X	X	1				38 (10)	
ST72F325/F321B	basic	X	X	X		1				36	39
ST72F321/F521 ST72F324BJ6/K6	basic	X	X	X							
ST7232x/521(9) (incl. L and B versions)	medium			X							
ST72F32A ST72F324L ST72F324BJ2/J2 ST72F324BK4/K4	basic	X	X	X							Not supported
ST72F60x/F62x/F63x/ F63Bx/ST7FSCR	basic	X	X	X			Fixed 256.t_{CPU}	Not applicable	ICCSEL	38 (10)	
ST72F651(1)	basic	X	X	X							
ST7260/61x/62x/63x/ 63Bx/65/ ST7SCR(9)	medium			X							
ST7FMC	basic	X	X	X	X	1	Controlled	VPP/ ICCSEL(7)	ICCDATA	38(11)	

1. For these devices, the ST7 has to enter external clock mode in order to be able to reprogram devices with hardware watchdog enabled. Refer to the External Clock/Application Clock ICC modes section of the ICC protocol reference manual for more details.
2. The pulse counter is reset when $\overline{\text{RESET}}$ is low and ICCCLK is high.
3. In 38-pulse ICC mode, the internal RC oscillator is forced as a clock source, regardless of the selection in the option byte.

4. In the ST7FLITEUS, an interrupt is generated in ICC mode due to ICCCLK on PA1, configured as pull-up interrupt by default. The workaround is to enable the interrupt mask before the IRET of the ICC monitor, when executing the GO command.
5. Contrary to the behavior described in “appli clock” legend, the ST7FLITEUS takes into account the option byte configuration including the hardware watchdog if it is enabled. Consequently, 35-pulse mode must be used if hardware watchdog is enabled.
   In addition, when ST7FLITEUS is used in 38-pulse mode, the internal 8 MHz RC is selected as clock source if option CKSEL[1:0]=00h, otherwise, if CKSEL is not 00h, AWU RC is selected as clock source. External clock can not be selected when using 38-pulse mode.
   Limitation: In ST7FLITEUS when programming the LVD option from OFF to ON in 38-pulse mode and if the AVD is OFF, a spurious reset is generated and ICC communication is lost. The workaround is either to use 35-pulse mode or to ensure that the programming tool generates a reset after programming the Option Byte.
6. There are 4 option bytes in this device: Option byte 0 and 1 starting at address E000h and Option byte 2 and 3 starting at C000h. Take care to program Option byte 0, 1, 2 and 3 in the same routine. Then the following steps must be followed to modify the option bytes:
   -Read the 4 bytes in the device
   -Modify as desired
   -Write the 4 bytes in the device
7. The pulse counter is reset when $\overline{\text{RESET}}$ and ICCSEL are both low.
8. If ICC mode is entered using this pulse sequence, the clock source option bits must not be modified during the ICC session. To modify the clock source option bits, use the “external clock” pulse sequence.
9. All ROM devices support the medium variant of the ICC monitor. Hence these devices can be read if the Read-out protection has not been enabled. However it must be noted that only the program memory of these devices can be read but not the option bytes.
10. For these devices, if this number of pulses is generated, the ST7 can be supplied by an external clock source or a resonator. In this case, legends on “ext clock” and “applil clock” are not relevant.
11. For these devices, if this number of pulses is generated, the ST7 will be supplied by its internal clock. No external clock is required in ICC mode.

1.4 System memory addresses

In certain products, the System memory is accessible either in USER or ICC modes. Its address is given in *Table 4* below.

Table 4. System memory addresses

Product		System memory addresses			
Name	**Identifier (1)**	**ICC_mode**	**ICC_monitor_trap**	**ICC_send_byte**	**ICC_receive_byte**
ST7FLITE0/S2/S5/ ST7FL0	819 1	F98Bh	F98Fh	NA	F9A6h
ST7FLITE1B ST7FL1B	829 1	EF2Bh	EF2Fh	EF00h	EF6Bh
ST7FLITE2/1/FDALI	837 1	DF2Bh	DF2Fh	DF00h	DF6Bh
ST7FLITE3/ST7FL3	852 0	DF2Bh	DF2Fh	DF00h	DF6Bh
STFLITE4M	878 0	DF2Bh	DF2Fh	DF00h	DF6Bh
ST7FLITEUS	875 0	DF2Bh	DF2Fh	DF00h	DF6Bh
ST7FLITEU0	876 0	DF2Bh	DF2Fh	DF00h	DF6Bh
ST72F26X	825 1	DF2Bh	DF2Fh	DF00h	DF6Bh
ST7226X	826 1	DF29h	DF2Dh	DF00h	DF47h
ST72F34X	864 1	BF2Bh	BF2Fh	BF00h	BF6Bh

1. For more details, refer to the ICC protocol reference manual.

Appendix A ST7SCR ICC mode entry

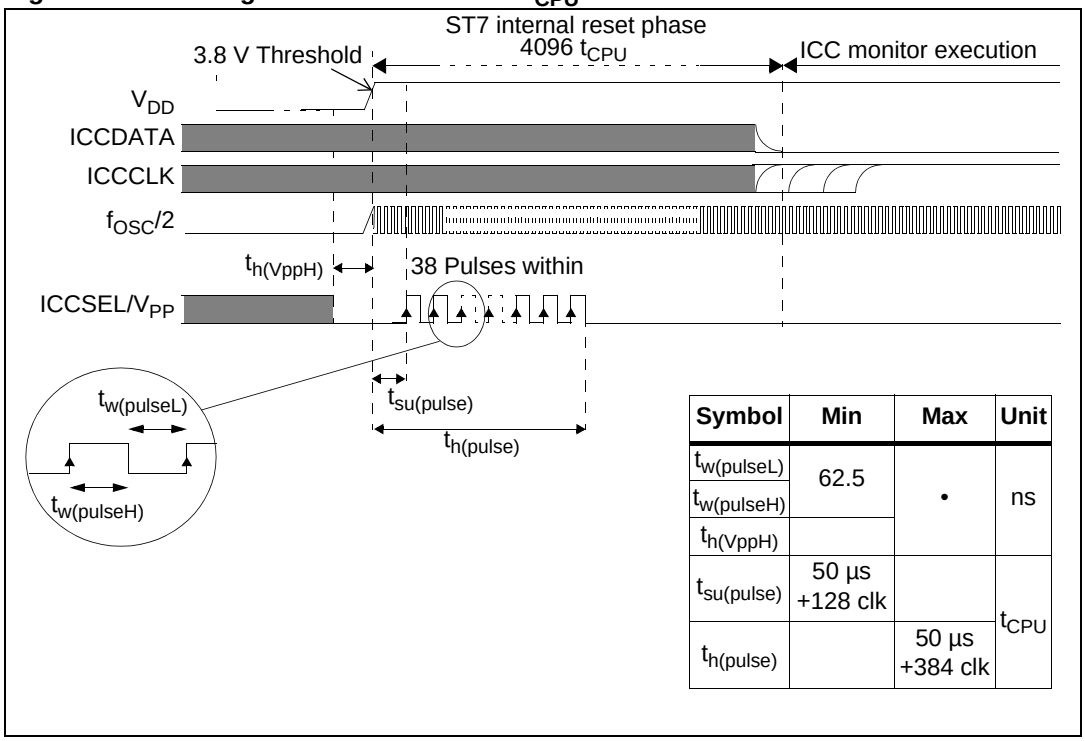
For an external controller to be able to put the ST7SCR into ICC mode, the procedure has to be slightly modified because the ST7SCR has no external $\overline{\text{RESET}}$ pin to synchronize the start of the pulse train that defines ICC mode entry. Instead the synchronization has to be done on the V_{IT+} rising threshold at power on. This can be implemented by a external analog comparator with a threshold of 3.8V.

As shown in *Figure 1*, a startup delay has to be inserted, specified as follows:

$t_{STARTUP}$ min. 50 µs +128 t_{CPU}

$t_{STARTUP}$ max. 50 µs +384 t_{CPU}

Figure 1. Entering ICC mode with fixed t_{CPU} window



Symbol	Min	Max	Unit
$t_{w(pulseL)}$	62.5	•	ns
$t_{w(pulseH)}$			
$t_{h(VppH)}$			
$t_{su(pulse)}$	50 µs +128 clk		t_{CPU}
$t_{h(pulse)}$		50 µs +384 clk	

A.1 ROM product, ICC mode selection

In ROM ST7SCR devices, the V_{PP} pin is replaced by a pin called TM (for Test mode). When this pin is high, the LVD is powered off, pin PA6 becomes a reset pin and pin PA0 becomes the V_{PP} pin.

To enter ICC mode:

1. Hold the TM pin at high level.
2. Reset the chip by applying a low level pulse on PA6
3. Apply 38 pulses on the PA0 pin as shown in *Figure 1*.
4. When the mode entry window is finished, the PA0 port acts as the ICCDATA function.

2 Revision history

Table 5. Document revision history

Date	Revision	Changes
02-May-2005	1	Initial release.
16-Dec-2005	2	Added information for ST72F325, ST72F361, ST7FLITE1B
15-Fev-2006	3	Added information in *Table 3.* for ST72F32A, ST7FL0,ST7FL3 Modified notes 6 and 7 *on page 6*
17-July-2006	4	Added information in *Table 1.* and *Table 3.* for ST72F60, ST7260, ST72F63B, ST7263B, ST72F34x, ST7FLITEUS
23-Mar-2007	5	Modified text in *Chapter 1.2: RC calibration value addresses* ST7LITEU0 added in *Table 3.* and *Table 4.* Added note 11 to *Table 3.* Changed orders of the notes. Modified ST72F34x in *Table 3.* (ICCSEL instead of ICCCLK)
11-May-2007	6	STFLITE4M added to *Table 3: Implemented ICC features in ST7 devices* and *Table 4: System memory addresses*. Other changes in *Table 3*: – information on ST72F32x devices modified, – one Note removed and *Note 3* added, – 39 application clock pulses not supported on ST72F32A, – Notes on legends in *Table 3.* replaced by a section: “description of legends for *Table 3.*”

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