IR3859MPbF

SupIRBuck™

HIGHLY EFFICIENT
INTEGRATED 9A, SYNCHRONOUS BUCK REGULATOR

Features

- Greater than 95% Maximum Efficiency
- Wide Input Voltage Range 1.5V to 21V
- Wide Output Voltage Range 0.7V to 0.9*Vin
- Continuous 9A Load Capability
- Integrated Bootstrap-diode
- High Bandwidth E/A for excellent transient performance
- Programmable Switching Frequency up to 1.5MHz
- Programmable Over Current Protection
- Over Voltage Protection
- Dedicated input for output voltage monitoring
- Programmable PGood output
- Hiccup Current Limit
- Precision Reference Voltage (0.7V, +/-1%)
- Programmable Soft-Start
- Enable Input with Voltage Monitoring Capability
- Enhanced Pre-Bias Start-up
- Seq input for Tracking applications
- External Synchronization
- -40°C to 125°C operating junction temperature
- Thermal Protection
- 4mm x 5mm Power QFN Package
- Halogen Free, Lead Free and RoHS compliant

Description

The IR3859 ***SupIRBuck™*** is an easy-to-use, fully integrated and highly efficient DC/DC synchronous Buck regulator. The MOSFETs co-packaged with the on-chip PWM controller make IR3859 a space-efficient solution, providing accurate power delivery for low output voltage applications.

IR3859 is a versatile regulator which offers programmability of start up time, switching frequency and current limit while operating in wide input and output voltage range.

The switching frequency is programmable from 250kHz to 1.5MHz for an optimum solution.

It also features important protection functions, such as Pre-Bias startup, hiccup current limit and thermal shutdown to give required system level security in the event of fault conditions.

Applications

- Server Applications
- Storage Applications
- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Netcom Applications
- Computing Peripheral Voltage Regulators
- General DC-DC Converters

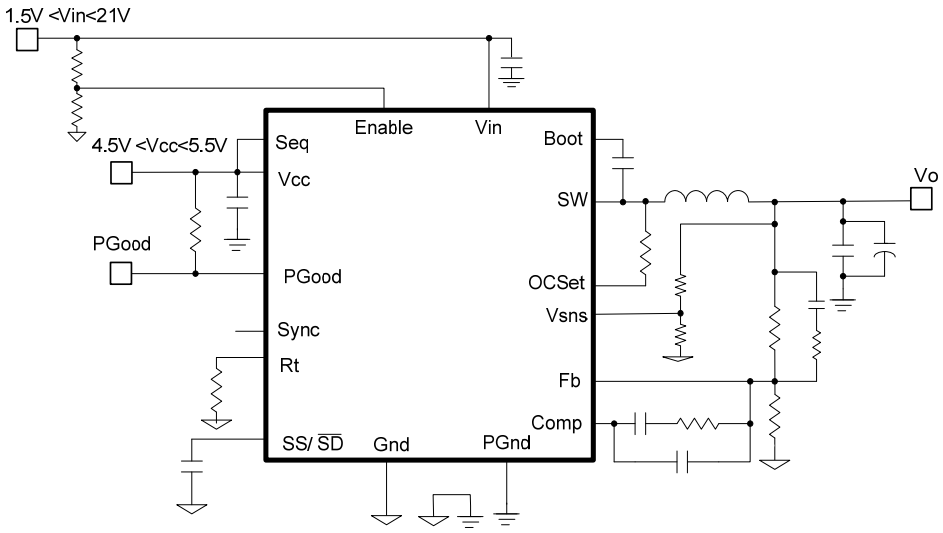


Fig. 1. Typical application diagram

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND unless otherwise specified)

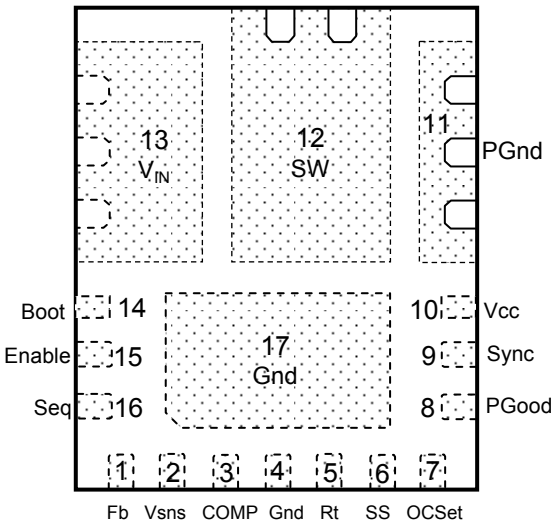
- Vin ..... -0.3V to 25V
- Vcc ..... -0.3V to 8V *(Note2)*
- Boot ..... -0.3V to 33V
- SW ..... -0.3V to 25V(DC), -4V to 25V(AC, 100ns)
- Boot to SW ..... -0.3V to Vcc+0.3V *(Note1)*
- OCSet ..... -0.3V to 30V (Max 30mA)
- Input / output Pins ..... -0.3V to Vcc+0.3V *(Note1)*
- PGND to GND ..... -0.3V to +0.3V
- Storage Temperature Range ..... -55°C To 150°C
- Junction Temperature Range ..... -40°C To 150°C *(Note2)*
- ESD Classification ..... JEDEC Class 1C
- Moisture sensitivity level..... JEDEC Level 3@260 °C *(Note5)*

Note1: *Must not exceed 8V*
Note2: *Vcc must not exceed 7.5V for Junction Temperature between -10°C and -40°C*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

PACKAGE INFORMATION

4mm x 5mm POWER QFN



$\theta_{JA(Sync_FET)} = 45^{o}C/W$ *

$\theta_{JA(Ctrl_FET)} = 45^{o}C/W$ *

$\theta_{J\text{-}PCB} = 2^{o}C/W$

* *Exposed pads on underside are connected to copper pads of a 4-layer (2 oz.) PCB*

ORDERING INFORMATION

PACKAGE DESIGNATOR	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER REEL
M	IR3859MTRPbF	17	4000
M	IR3859MTR1PbF	17	750

Block Diagram

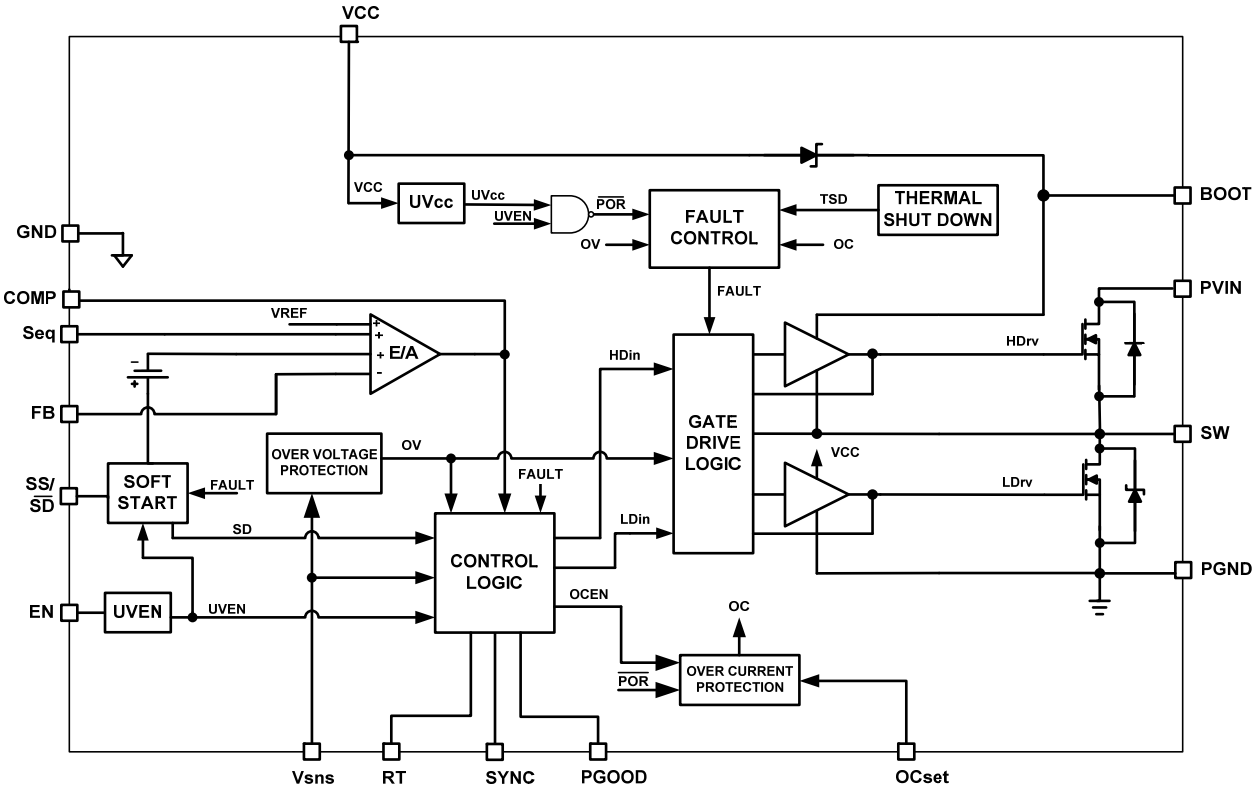


Fig. 2. Simplified block diagram of the IR3859

Pin Description

Pin	Name	Description
1	Fb	Inverting input to the error amplifier. This pin is connected directly to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	Vsns	Sense pin for PGood
3	Comp	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to Fb pin to provide loop compensation.
4;17	Gnd	Signal ground for internal reference and control circuitry.
5	Rt	Set the switching frequency. Connect an external resistor from this pin to Gnd to set the switching frequency. See Table 1 for Fs vs. Rt.
6	SS/SD	Soft start / shutdown. This pin provides user programmable soft-start function. Connect an external capacitor from this pin to Gnd to set the start up time of the output voltage. The converter can be shutdown by pulling this pin below 0.3V.
7	OCSet	Current limit set point. A resistor from this pin to SW pin will set the current limit threshold.
8	PGood	Power Good status pin. Output is open drain. Connect a pull up resistor from this pin to Vcc.
9	Sync	Sync pin, connect external system clock to synchronize multiple POLs with the same frequency
10	V_{CC}	This pin powers the internal IC and the drivers. A minimum of 1uF high frequency capacitor must be connected from this pin to the power ground (PGnd).
11	PGnd	Power Ground. This pin serves as a separated ground for the MOSFET drivers and should be connected to the system's power ground plane.
12	SW	Switch node. This pin is connected to the output inductor.
13	V_{IN}	Input voltage connection pin.
14	Boot	Supply voltage for high side driver. A 0.1uF capacitor must be connected from this pin to SW.
15	Enable	Enable pin to turn on and off the device. Use two external resistors to set the turn on threshold (see Enable section). Connect this pin to Vcc if it is not used.
16	Seq	Sequence pin. Use two external resistors to set Simultaneous Power up sequencing. If this pin is not used connect to Vcc.

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{in}	Input Voltage	1.5	21*	V
V_{cc}	Supply Voltage	4.5	5.5	
Boot to SW	Supply Voltage	4.5	5.5	
V_o	Output Voltage	0.7	0.9*Vin	
I_o	Output Current	0	9	A
Fs	Switching Frequency	225	1650	kHz
T_j	Junction Temperature	-40	125	°C

* Note: SW node should not exceed 25V

Electrical Specifications

Unless otherwise specified, these specification apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0°C<T_j< 125°C.
Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
POWER STAGE						
Power Losses	P_{loss}	Vcc=5V, V_{in}=12V, V_o=1.8V, I_o=9A, Fs=600kHz, L=0.68uH, *Note4*		2.1		W
Top Switch	$R_{ds(on)_Top}$	V_{Boot} -V_{sw} =5V, I_D=9A, Tj=25°C		21	29	mΩ
Bottom Switch	$R_{ds(on)_Bot}$	V_{cc}=5V, I_D=9A, T_j=25°C		11	16	
Deadband Time	T_{db}	Note4	5	10	30	ns
Bootstrap Diode Forward Voltage		I(Boot)= 30mA	180	260	470	mV
SW leakage Current	Isw	SW=0V, Enable=0V			6	uA
		SW=0V, Enable=high, SS=3V, Vseq=0V, Note4				
SUPPLY CURRENT						
V_{CC} Supply Current (Standby)	$I_{CC(Standby)}$	SS=0V, Vcc=5V, Enable low , No Switching			500	uA
V_{CC} Supply Current (Dyn)	$I_{CC(Dyn)}$	SS=3V, Vcc=5V, Enable high, Fs=500kHz	5.5	9.97	14	mA
REFERENCE VOLTAGE						
Feedback Voltage	VFB			0.7		V
Accuracy		0°C<Tj<125°C	-1.0		+1.0	%
		-40°C<Tj<125°C, Note3	-2.0		-2.0	
SOFT START / SD						
Soft Start Current	ISS	Source	14	20	26	uA
Soft Start Clamp Voltage	Vss(clamp)		2.7	3.0	3.3	V
Shutdown Output Threshold	SD				0.3	

Electrical Specifications (continued)

Unless otherwise specified, these specifications apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0°C<T_j< 125°C.
Typical values are specified at T_a = 25°C.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
Input Offset Voltage	Vos	Vfb-Vseq, Vseq=0.8V	-10		+10	mV
Input Bias Current	IFb(E/A)		-1		+1	µA
Input Bias Current	IVseq(E/A)		-1		+1	
Sink Current	Isink(E/A)		0.40	0.85	1.2	mA
Source Current	Isource(E/A)		8	10	13	
Slew Rate	SR	*Note4*	7	12	20	V/µs
Gain-Bandwidth Product	GBWP	*Note4*	20	30	40	MHz
DC Gain	Gain	*Note4*	100	110	120	dB
Maximum Voltage	Vmax(E/A)	Vcc=4.5V	3.4	3.5	3.75	V
Minimum Voltage	Vmin(E/A)			120	220	mV
Seq Common Mode Voltage		*Note4*	0		1	V
OSCILLATOR						
Rt Voltage	Vrt		0.665	0.7	0.735	V
Frequency Range	F_S	Rt=59K	225	250	275	kHz
		Rt=28.7K	450	500	550	
		Rt=9.31K, Note4	1350	1500	1650	
Ramp Amplitude	Vramp	*Note4*		1.8		Vp-p
Ramp Offset	Ramp(os)	*Note4*		0.6		V
Min Pulse Width	Dmin(ctrl)	*Note4*		50		ns
Max Duty Cycle	Dmax	Fs=250kHz	92			%
Fixed Off Time	Toff	*Note4*		130	200	ns
Sync Frequency Range	Fsync		225		1650	kHz
Sync Pulse Duration	Tsync		100	200		ns
Sync Level Threshold	High		2			V
	Low				0.6	

Electrical Specifications (continued)

Unless otherwise specified, these specification apply over 4.5V< V_{cc}<5.5V, V_{in}=12V, 0ºC<T_j< 125ºC.
Typical values are specified at T_a = 25ºC.

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
FAULT PROTECTION						
OCSET Current	I_{OCSET}	Fs=250kHz	20.8	23.6	26.4	uA
		Fs=500kHz	43	48.8	54.6	
		Fs=1500kHz	136	154	172	
OC comp Offset Voltage	V_{OFFSET}	*Note4*	-10	0	+10	mV
SS off time	SS_Hiccup			4096		Cycles
OVP Trip Threshold	OVP(trip)	Vsns Rising	110	115	120	%Vref
OVP Fault Prop. Delay	OVP(delay)	*Note4*			150	ns
Thermal Shutdown		*Note4*		140		°C
Thermal Hysteresis		*Note4*		20		
V_{CC}-Start-Threshold	V_{CC}_UVLO_Start	Vcc Rising Trip Level	3.95	4.15	4.35	V
V_{CC}-Stop-Threshold	V_{CC}_UVLO_Stop	Vcc Falling Trip Level	3.65	3.85	4.05	
INPUT/OUTPUT SIGNAL						
Enable-Start-Threshold	Enable_UVLO_Start	Supply ramping up	1.14	1.2	1.36	V
Enable-Stop-Threshold	Enable_UVLO_Stop	Supply ramping down	0.9	1.0	1.06	
Enable leakage current	Ien	Enable=3.3V			15	uA
Power Good Threshold	VPG	Vsns Rising	80	85	90	%Vref
PGood Comparator Delay	PG(Delay)	Vsns Rising		256/Fs		s
PGood Delay Comparator Threshold	SS(Delay)	Relative to charge voltage, SS rising	2	2.1	2.3	V
PGood Delay Comparator Hysteresis	Delay(SShys)	*Note4*	260	300	340	mV
PGood Leakage Current	I(PGDlk)			0	10	uA
PGood Voltage Low	PG(voltage)	I_{Pgood}=-5mA			0.5	V

Note3: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.

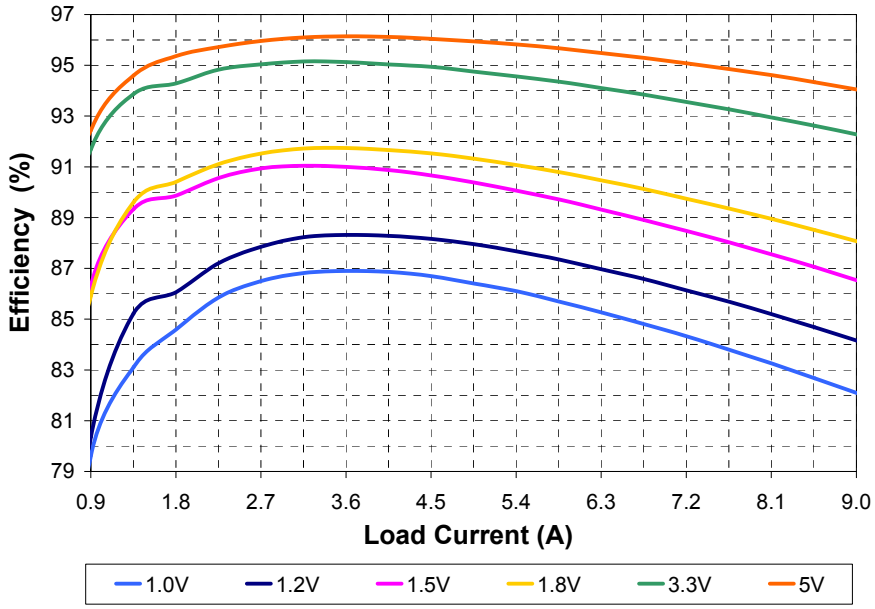
Note4: Guaranteed by Design but not tested in production.

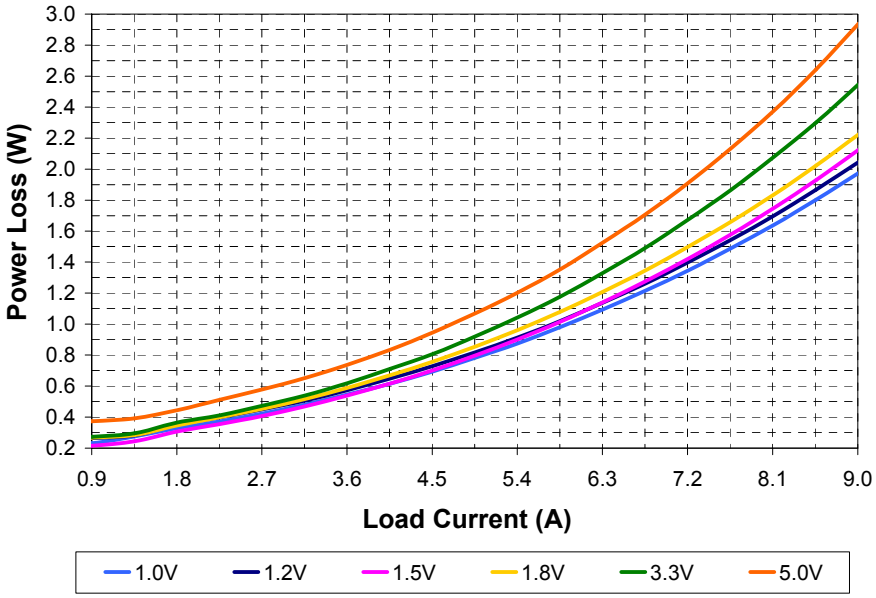
Note5: Upgrade to industrial/MSL2 level applies from date codes 1227 (marking explained on application note AN1132 page 2). Products with prior date code of 1227 are qualified with MSL3 for Consumer market.

Typical Efficiency and Power Loss Curves
Vin=12V, Vcc=5V, Io=0.9A- 9A, F_s=600kHz, Room Temperature, No Air Flow

The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vo (V)	L (uH)	P/N	DCR (mOhm)
1	0.51	59PR9876N	0.29
1.2	0.51	59PR9876N	0.29
1.5	0.68	ETQP4LR68XFC	1.58
1.8	0.68	ETQP4LR68XFC	1.58
3.3	1.2	MPL105-1R2	2.9
5	1.2	MPL105-1R2	2.9

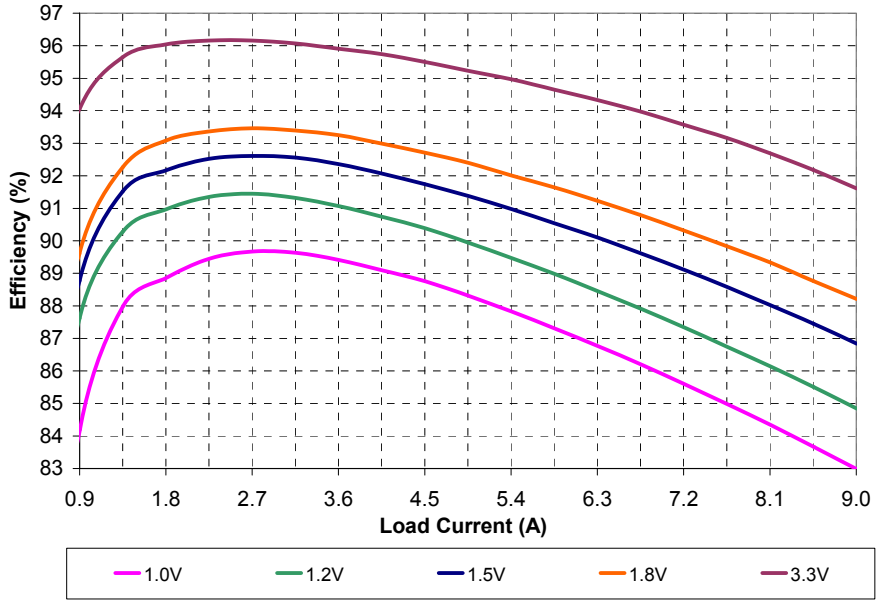


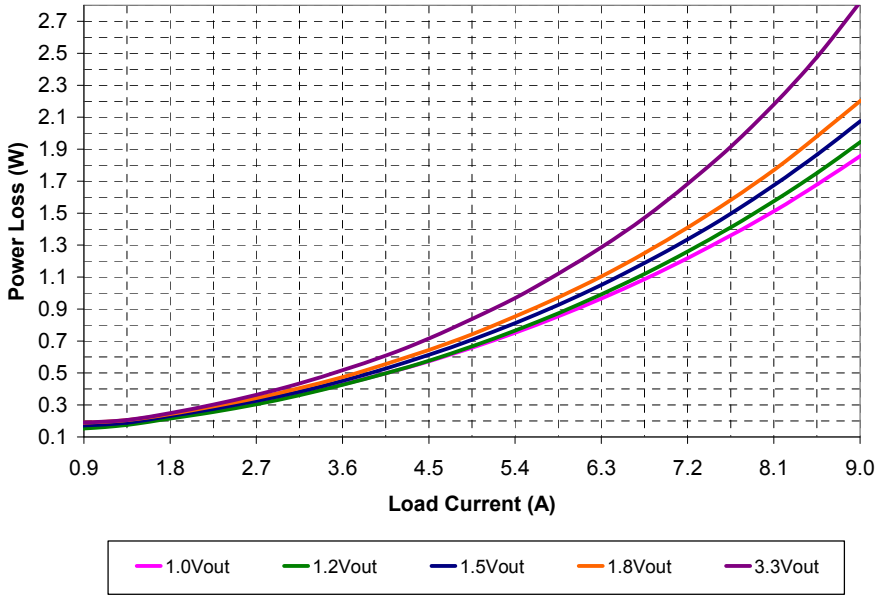


Typical Efficiency and Power Loss Curves
Vin=5V, Vcc=5V, Io=0.9A- 9A, Fs=600kHz, Room Temperature, No Air Flow

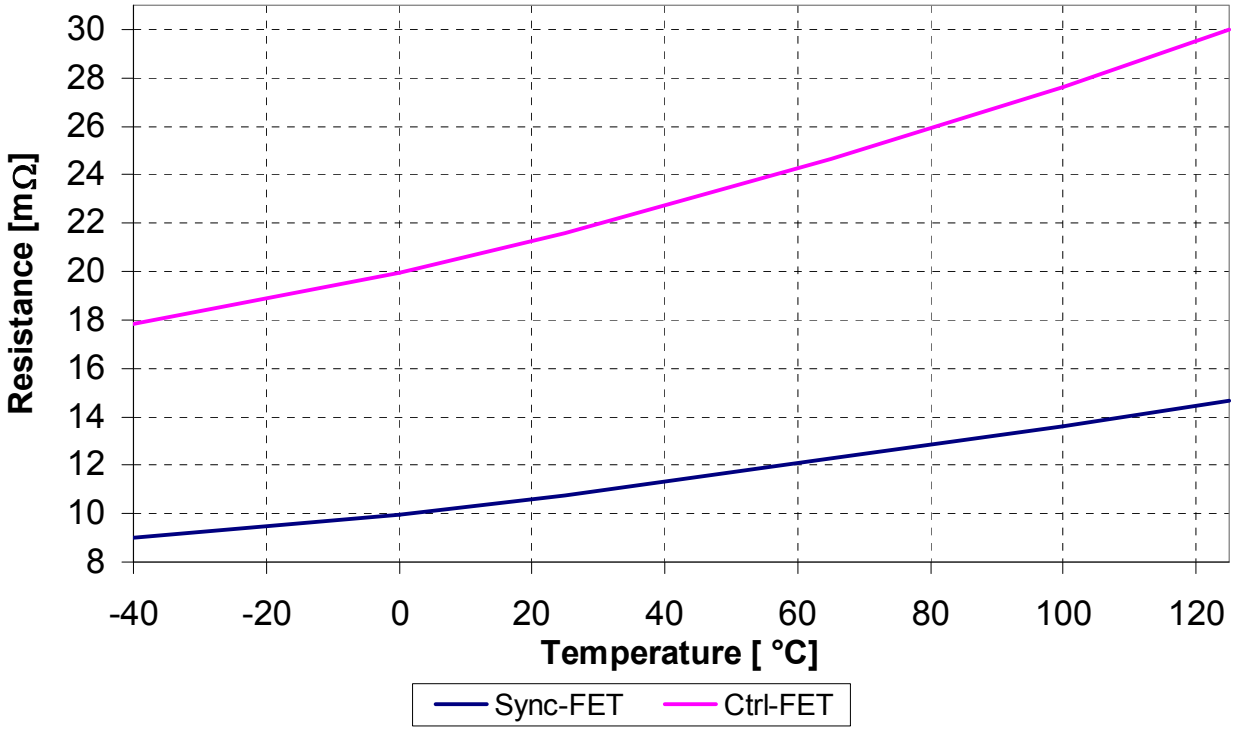
The table below shows the inductors used for each of the output voltages in the efficiency measurement.

Vo (V)	L (uH)	P/N	DCR (mOhm)
1	0.4	59PR9875N	0.29
1.2	0.51	59PR9876N	0.29
1.5	0.51	59PR9876N	0.29
1.8	0.51	59PR9876N	0.29
3.3	0.51	59PR9876N	0.29



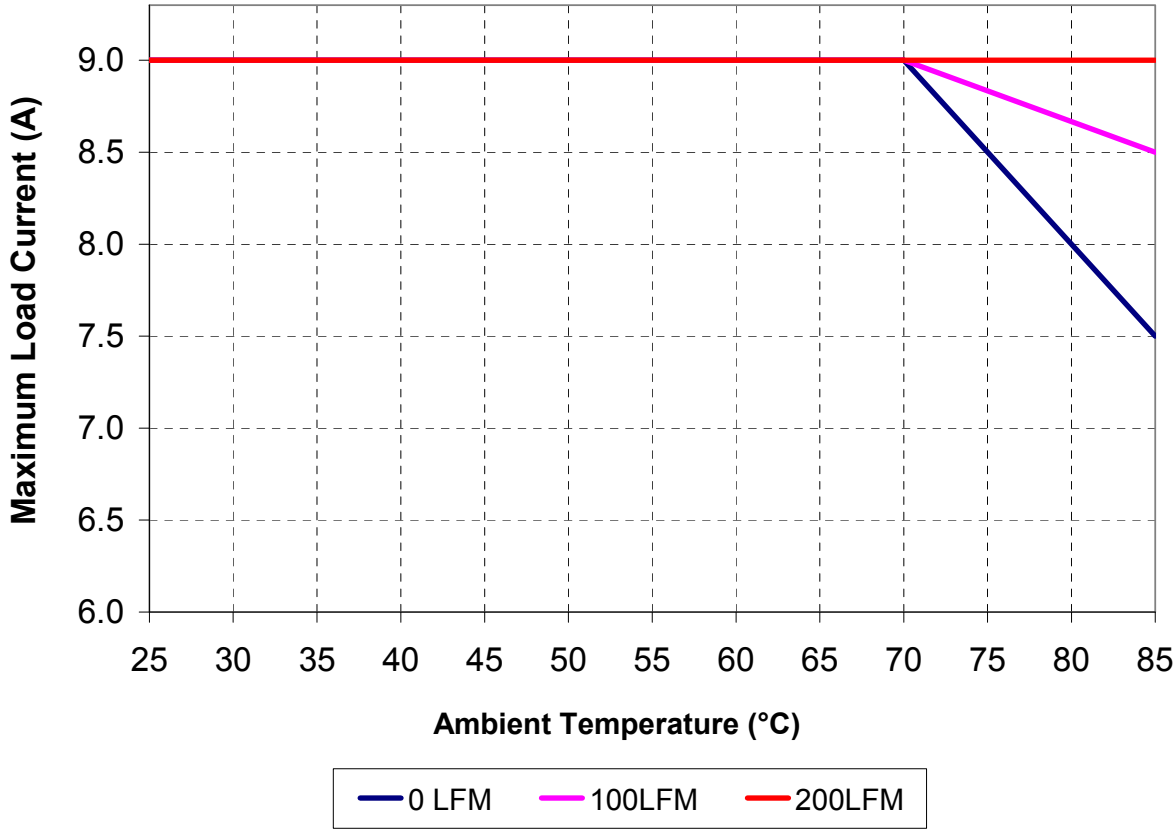


Rdson of MOSFETs Over Temperature at Vcc=5V



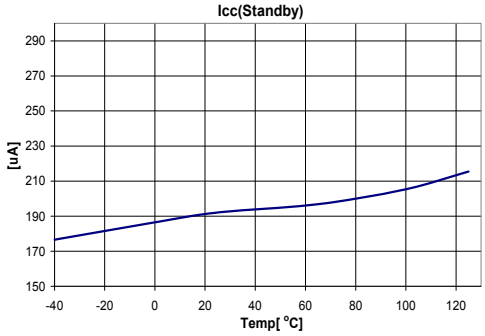
Thermal De-rating Curves

Test Conditions: Vin=12V, Vout=1.8V, Vcc=5V, Fs=600kHz, 0- 200LFM
L=0.68uH (ETQP4LR68XFC)

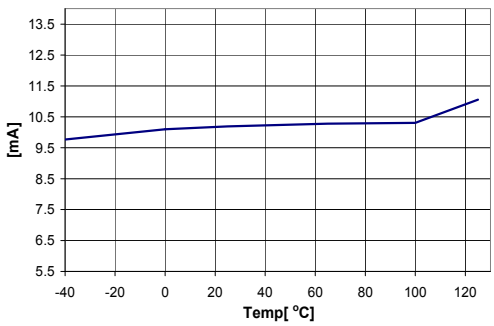


TYPICAL OPERATING CHARACTERISTICS (-40°C - 125°C) F_s=500 kHz

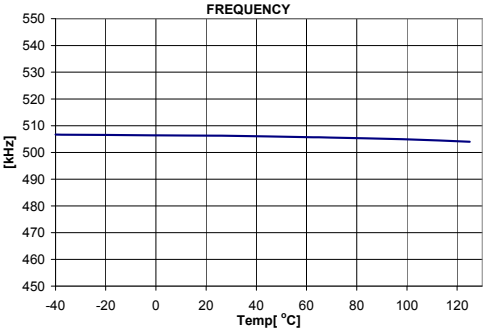
Icc(Standby)



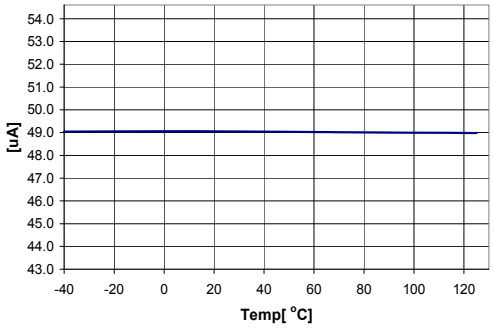
Icc(Dyn)



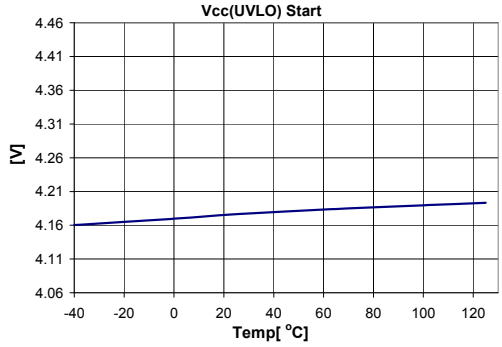
FREQUENCY



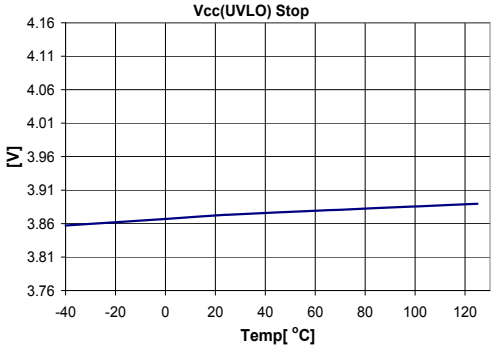
IOCSET(500kHz)



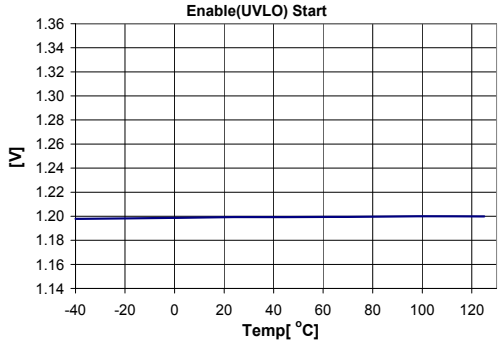
Vcc(UVLO) Start



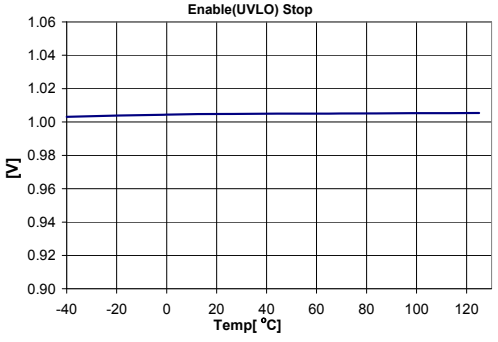
Vcc(UVLO) Stop



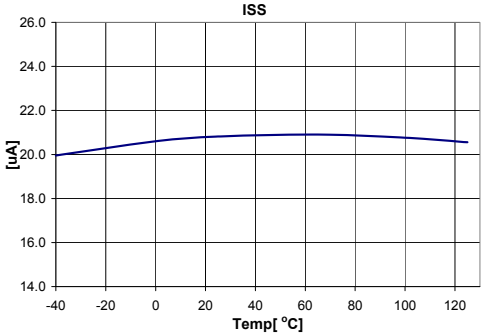
Enable(UVLO) Start



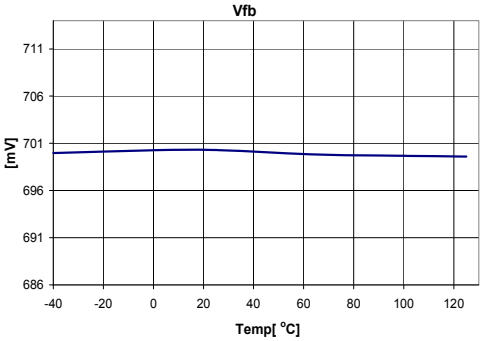
Enable(UVLO) Stop



ISS



Vfb



Circuit Description

THEORY OF OPERATION

Introduction

The IR3859 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types.

The switching frequency is programmable from 250kHz to 1.5MHz and provides the capability of optimizing the design in terms of size and performance.

IR3859 provides precisely regulated output voltage programmed via two external resistors from 0.7V to 0.9*Vin.

The IR3859 operates with an external bias supply from 4.5V to 5.5V, allowing an extended operating input voltage range from 1.5V to 21V.

The device utilizes the on-resistance of the low side MOSFET as current sense element, this method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistor.

IR3859 includes two low $R_{ds(on)}$ MOSFETs using IR's HEXFET technology. These are specifically designed for high efficiency applications.

Under-Voltage Lockout and POR

The under-voltage lockout circuit monitors the input supply Vcc and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drop below the set thresholds. Normal operation resumes once Vcc and Enable rise above their thresholds.
The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram). When the POR is asserted the soft start sequence starts (see soft start section).

Enable

The Enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3859 will turn on only when the voltage at the Enable pin exceeds this threshold, typically, 1.2V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3859 does not turn on until the bus voltage reaches the desired level. Only after the bus voltage reaches or exceeds this level will the voltage at Enable pin exceed its threshold, thus enabling the IR3859. Therefore, in addition to being a logic input pin to enable the IR3859, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage V_{in}. This is desirable particularly for high output voltage applications, where we might want the IR3859 to be disabled at least until V_{in} exceeds the desired output voltage level.

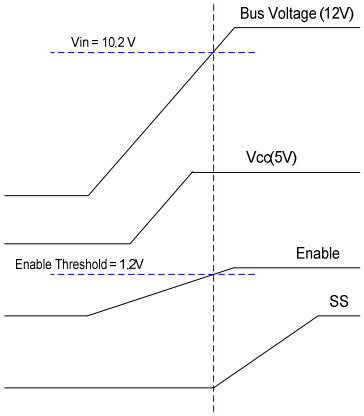


Fig. 3a. Normal Start up, Device turns on when the Bus voltage reaches 10.2V

Figure 3b. shows the recommended start-up sequence for the non-sequenced operation of IR3859, when Enable is used as a logic input.

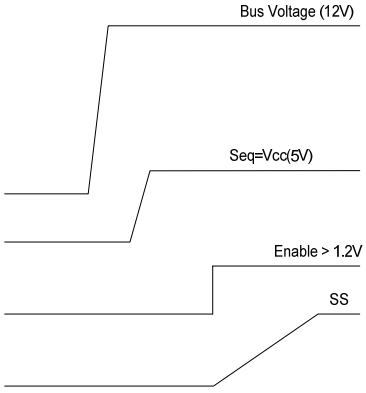


Fig. 3b. Recommended startup sequence, Non-Sequenced operation

Figure 3c. shows the recommended startup sequence for sequenced operation of IR3859 with Enable used as logic input.

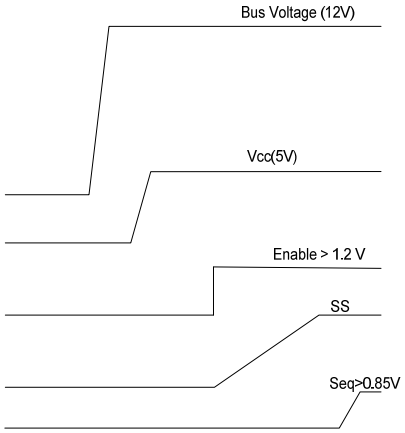


Fig. 3c. Recommended startup sequence, Sequenced operation

Pre-Bias Startup

IR3859 is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure 4 shows a typical Pre-Bias condition at start up.

The synchronous MOSFET always starts with a narrow pulse width and gradually increases its duty cycle with a step of 25%, 50%, 75% and 100% until it reaches the steady state value. The number of these startup pulses for the synchronous MOSFET is internally programmed. Figure 5 shows a series of 32, 16, 8 startup pulses.

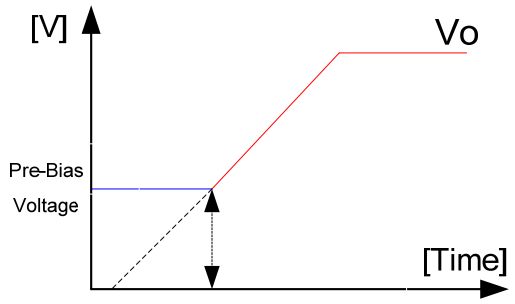


Fig. 4. Pre-Bias startup

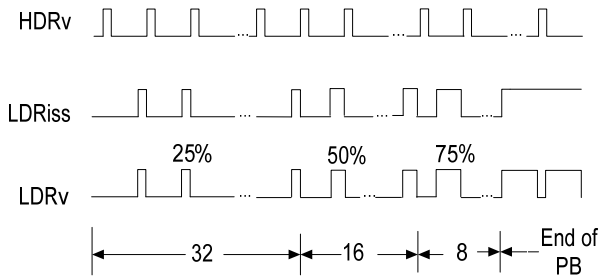


Fig. 5. Pre-Bias startup pulses

Soft-Start

The IR3859 has a programmable soft-start to control the output voltage rise and to limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and Vcc rise above their UVLO thresholds and generate the Power On Ready (POR) signal. The internal current source (typically 20uA) charges the external capacitor C_{ss} linearly from 0V to 3V. Figure 6 shows the waveforms during the soft start.

The start up time can be estimated by:

$$T_{start} = \frac{(1.4 - 0.7) * C_{SS}}{20\mu A} \qquad \text{----------(1)}$$

During the soft start the OCP is enabled to protect the device for any short circuit and over current condition.

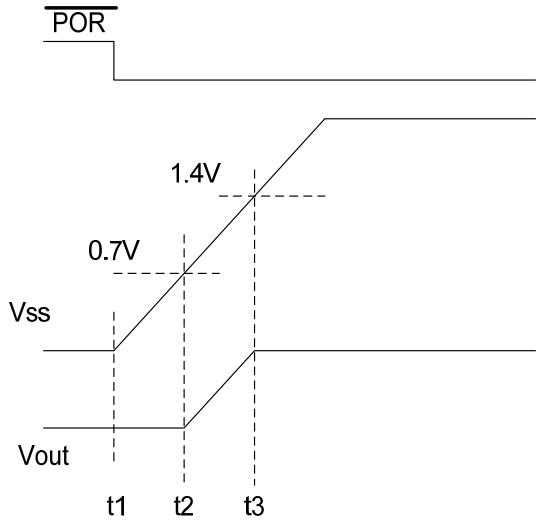


Fig. 6. Theoretical operation waveforms during soft-start

Operating Frequency

The switching frequency can be programmed between 250kHz – 1500kHz by connecting an external resistor from R_t pin to Gnd. Table 1 tabulates the oscillator frequency versus R_t.

Table 1. Switching Frequency and I_{OCSet} vs. External Resistor (R_t)

R_t (kΩ)	F_s (kHz)	I_{ocset} (µA)
47.5	300	29.4
35.7	400	39.2
28.7	500	48.7
23.7	600	59.07
20.5	700	68.2
17.8	800	78.6
15.8	900	88.6
14.3	1000	97.9
12.7	1100	110.2
11.5	1200	121.7
10.7	1300	130.8
9.76	1400	143.4
9.31	1500	150.3

Shutdown

The IR3859 can be shutdown by pulling the Enable pin below its 1 V threshold. This will tri-state both, the high side driver as well as the low side driver. Alternatively, the output can be shutdown by pulling the soft-start pin below 0.3V. Normal operation is resumed by cycling the voltage at the Soft Start pin.

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduces cost by eliminating a current sense resistor. As shown in figure 7, an external resistor (R_{OCSet}) is connected between OCSet pin and the switch node (SW) which sets the current limit set point.

An internal current source sources current (I_{OCSet}) out of the *OCSet* pin. This current is a function of Rt and hence, of the free-running switching frequency.

$$I_{OCSet}(\mu A) = \frac{1400}{R_t(k\Omega)} \quad \text{.....(2)}$$

Table 1. shows I_{OCSet} at different switching frequencies. The internal current source develops a voltage across R_{OCSet}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results in a voltage at OCSet which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \quad \text{.....(3)}$$

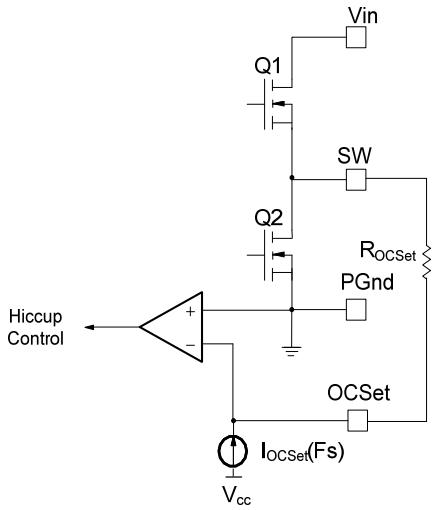


Fig. 7. Connection of over current sensing resistor

An over current is detected if the OCSet pin goes below ground. Hence, at the current limit threshold, V_{OCset}=0. Then, for a current limit setting I_{Limit}, R_{OCSet} is calculated as follows:

$$R_{OCSet} = \frac{R_{DS(on)} * I_{Limit}}{I_{OCSet}} \quad \text{.....(4)}$$

An overcurrent detection trips the OCP comparator, latches OCP signal and cycles the soft start function in hiccup mode.

The hiccup is performed by shorting the soft-start capacitor to ground and counting the number of switching cycles. The Soft Start pin is held low until 4096 cycles have been completed. The OCP signal resets and the converter recovers. After every soft start cycle, the converter stays in this mode until the overload or short circuit is removed.

The OCP circuit starts sampling current typically 160 ns after the low gate drive rises to about 3V. This delay functions to filter out switching noise.

Thermal Shutdown

Temperature sensing is provided inside IR3859. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs and discharges the soft start capacitor.

Automatic restart is initiated when the sensed temperature drops within the operating range. There is a 20°C hysteresis in the thermal shutdown threshold.

Output Voltage Sequencing

The IR3859 can accommodate user programmable sequencing options using Seq, Enable and Power Good pins.

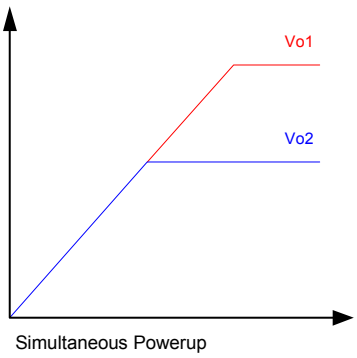


Fig. 8a. Simultaneous Power-up of the slave with respect to the master.

Through these pins, voltage sequencing such as simultaneous and sequential can be implemented. Figure 8. shows simultaneous sequencing configurations. In simultaneous power-up, the voltage at the Seq pin of the slave reaches 0.7V before the Fb pin of the master. For $R_E/R_F = R_C/R_D$, therefore, the output voltage of the slave follows that of the master until the voltage at the Seq pin of the slave reaches 0.7 V. After the voltage at the Seq pin of the slave exceeds 0.85V, the internal 0.7V reference of the slave dictates its output voltage.

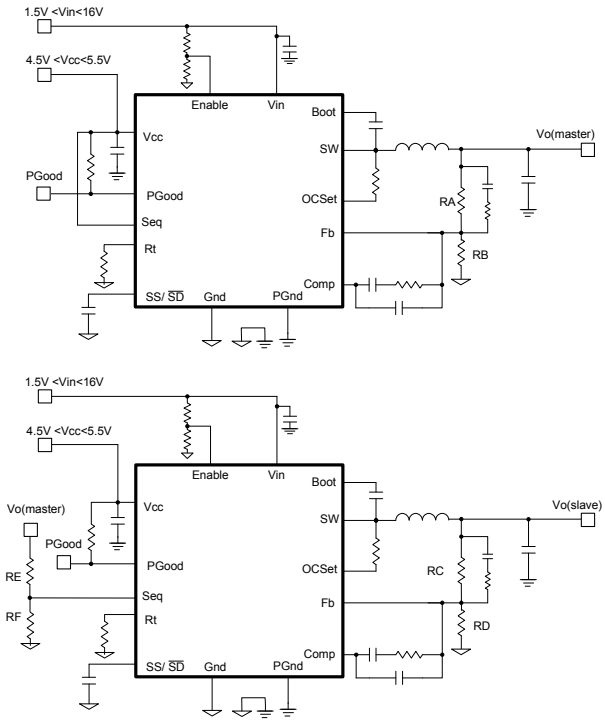


Fig. 8b. Application Circuit for Simultaneous Sequencing

Power-Good and Over-voltage Protection

The V_{sns} pin forms an input to a window comparator whose upper and lower thresholds are 0.805V and 0.595V, respectively. Hence, the Power Good signal is flagged when the V_{sns} pin voltage is within the PGood window, i.e. between 0.595V to 0.805V, as shown in figure 9. The PGood pin is open drain and it needs to be externally pulled high. High state indicates that output is in regulation. Figure 9a shows the PGood timing diagram for non-tracking operation. In this case, during startup, PGood goes high after the SS voltage reaches 2.1V if the Vsns voltage is within the PGood comparator window. Figure 9.a and Figure 9.b also show a 256 cycle delay between the Vsns voltage entering within the thresholds defined by the PGood window and PGood going high.

If the output voltage exceeds the over voltage threshold, an over voltage trip signal asserts, this will result to turn off the high side driver and turn on the low side driver until the Vsns voltage drops below 1.15*Vref threshold. Both drivers are latched off until a reset performed by cycling either Vcc or Enable.

The OVP threshold can be externally programmed to user defined value. Figure 10 shows the response in over-voltage condition.

TIMING DIAGRAM OF PGOOD FUNCTION

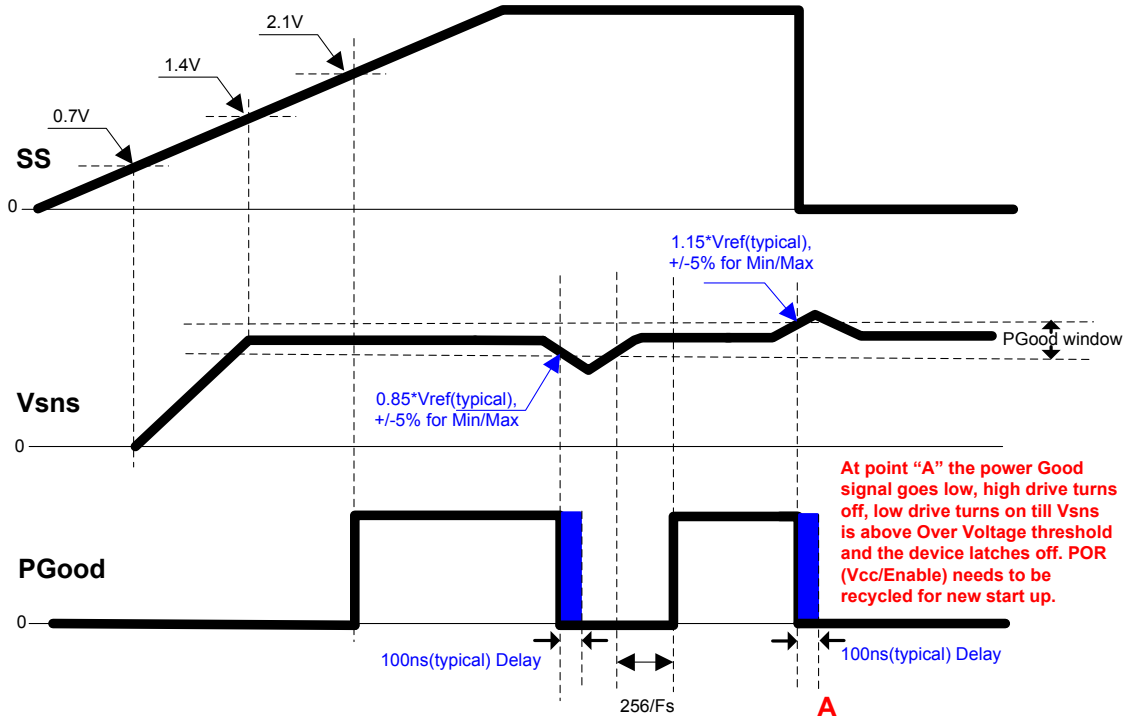


Fig.9a IR3859 Non-Tracking Operation (Seq=Vcc)

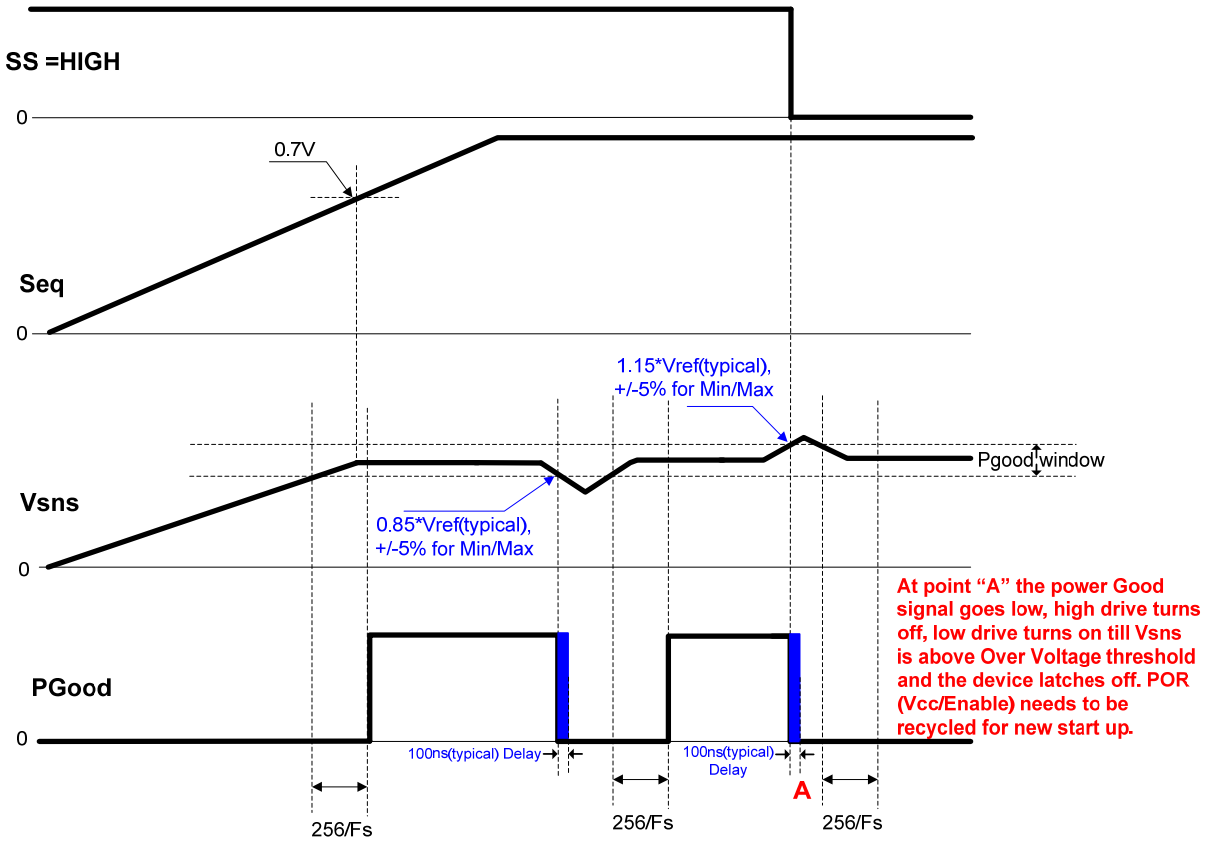
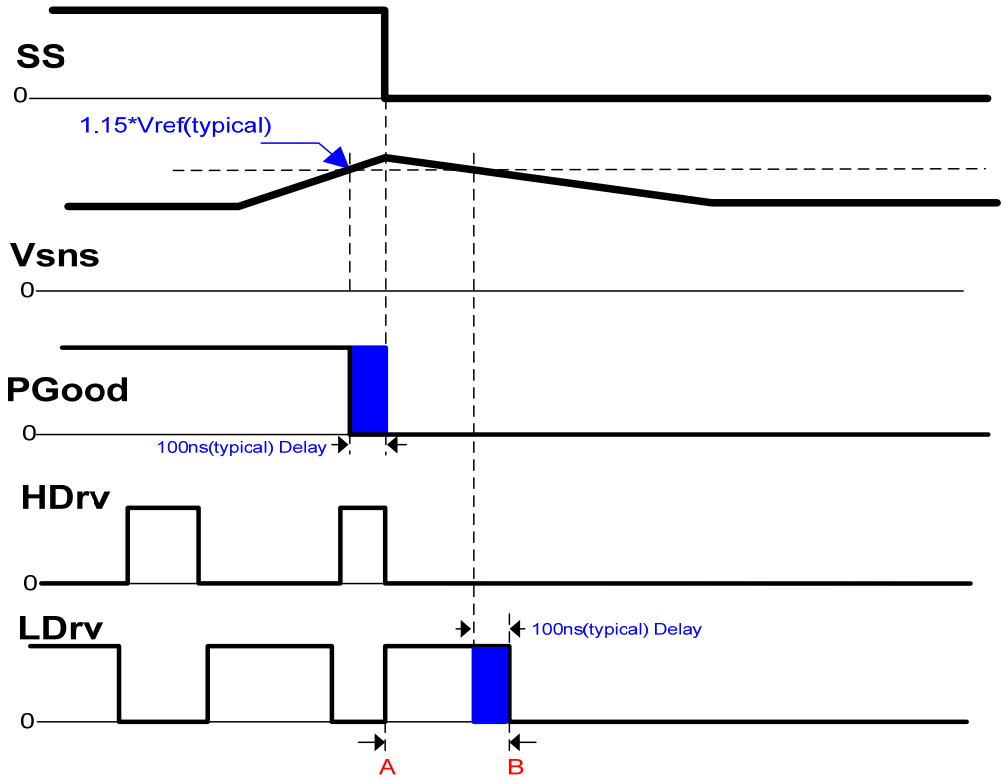


Fig.9b IR3859 Tracking Operation

TIMING DIAGRAM OF Over Voltage Protection



After Vsns gets above the Over Voltage threshold, upper Switch stays off and lower switch stays ON as long as the Vsns voltage is above the over voltage threshold. (i.e. from point A to point B). After point B, both switched stays off till /POR recycles.

Fig.10 IR3859 Over Voltage Timing Diagram

External Synchronization

The IR3859 incorporates an internal circuit which enables synchronization of the internal oscillator (using rising edge) to an external clock. An external resistor from Rt pin to Gnd is still required to set the free-running frequency close to the Sync input frequency. This function is important to avoid sub-harmonic oscillations due to beat frequency for embedded systems when multiple POL (point of load) regulators are used.

The synchronization clock can be applied during IR3859 normal operation or before IR3859 start-up. In any case, IR3859 will perform with the external after the end of the PreBias cycle.

Applying the external signal to the Sync input changes the effective value of the ramp signal (Vramp/Vosc).

$$V_{osc(eff)} = 1.8 \times f_{Free_Run} / f_{Sync} \quad \text{.....(5)}$$

Equation (5) shows that the effective amplitude of the ramp ($V_{osc(eff)}$) is reduced after the external Sync signal is applied. More difference between the frequency of the Sync (f_{Sync}) and the free-running frequency (f_{Free_Run}) results in more change in the effective amplitude of the ramp signal.

Therefore, since the ramp amplitude takes part in calculating the loop-gain and bandwidth of the regulator, it is recommended not to use a Sync frequency which is much higher than the free-running frequency. In addition, the effective value of the ramp signal, given by equation (5), should be used when the compensator is designed for the regulator.

The pulse width of the external clock, which is applied to the sync, should be greater than 100ns and its high level should be greater than 2V, while its lower level is less than 0.6V. If this pin is left floating, the IC will run with the free running frequency set by the resistor Rt.

Minimum on time Considerations

The minimum ON time is the shortest amount of time for which the Control FET may be reliably turned on, and this depends on the internal timing delays. For the IR3859, the typical minimum on-time is specified as 50 ns.
Any design or application using the IR3859 must ensure operation with a pulse width that is higher than this minimum on-time and preferably higher than 100 ns. This is necessary for the circuit to operate without jitter and pulse-skipping, which can cause high inductor current ripple and high output voltage ripple.

$$t_{on} = \frac{D}{F_s} = \frac{V_{out}}{V_{in} \times F_s}$$

In any application that uses the IR3859, the following condition must be satisfied:

$$t_{on(min)} \le t_{on}$$

$$\therefore t_{on(min)} \le \frac{V_{out}}{V_{in} \times F_s}$$

$$\therefore V_{in} \times F_s \le \frac{V_{out}}{t_{on(min)}}$$

The minimum output voltage is limited by the reference voltage and hence $V_{out(min)}$ = 0.7 V. Therefore, for $V_{out(min)}$ = 0.7 V,

$$\therefore V_{in} \times F_s \le \frac{V_{out(min)}}{t_{on(min)}}$$

$$\therefore V_{in} \times F_s \le \frac{0.7\ V}{100\ ns} = 7 \times 10^6\ V/s$$

Therefore, at the maximum recommended input voltage 21V and minimum output voltage, the converter should be designed at a switching frequency that does not exceed 333 kHz. Conversely, for operation at the maximum recommended operating frequency 1.65 MHz and minimum output voltage, any voltage above 4.2 V may not be stepped down without pulse-skipping.

Maximum Duty Ratio Considerations

A fixed off-time of 200 ns maximum is specified for the IR3859. This provides an upper limit on the operating duty ratio at any given switching frequency. It is clear, that higher the switching frequency, the lower is the maximum duty ratio at which the IR3859 can operate. To allow a margin of 50ns, the maximum operating duty ratio in any application using the IR3859 should still accommodate about 250 ns off-time. Fig 10. shows a plot of the maximum duty ratio v/s the switching frequency, with 250 ns off-time.

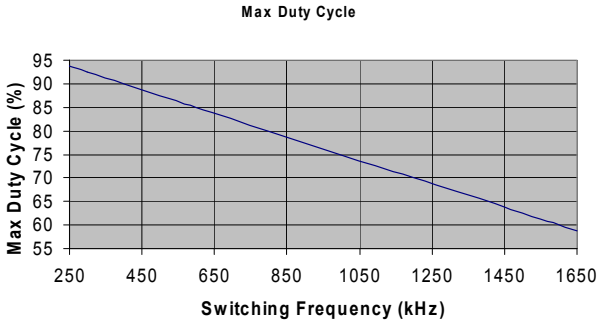


Fig. 11. Maximum duty cycle v/s switching frequency.

Application Information

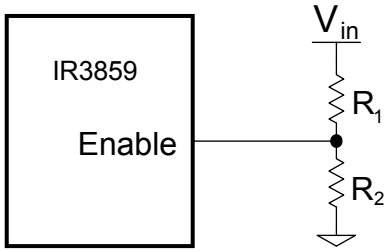
Design Example:

The following example is a typical application for IR3859. The application circuit is shown on page 25.

V_{in} = 12 V (13.2V max)
V_o = 1.8 V
I_o = 9 A
$\Delta V_o \leqslant \pm 5\%$ of V_o
F_s = 600 kHz

Enabling the IR3859

As explained earlier, the precise threshold of the Enable lends itself well to implementation of a UVLO for the Bus Voltage.



For a maximum Enable threshold of V_{EN} = 1.36 V

$$V_{in(min)} * \frac{R_2}{R_1 + R_2} = V_{EN} = 1.36V \quad \text{.....(6)}$$

$$R_2 = R_1 \frac{V_{EN}}{V_{in(min)} - V_{EN}} \quad \text{.....(7)}$$

For a $V_{in\ (min)}$=10.2V, R_1=49.9K and R_2=7.5K is a good choice.

Programming the frequency

For F_s = 600 kHz, select R_t = 23.7 kΩ, using Table. 1.

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.7V. The divider is ratioed to provide 0.7V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{ref} * \left(1 + \frac{R_8}{R_9}\right) \quad \text{..... ..... .(8)}$$

When an external resistor divider is connected to the output as shown in figure 12.
Equation (6) can be rewritten as:

$$R_9 = R_8 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad \text{.....(9)}$$

For the calculated values of R8 and R9 see feedback compensation section.

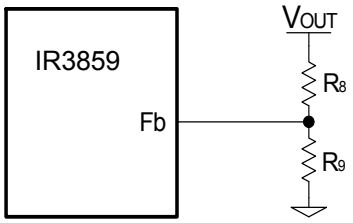


Fig. 12. Typical application of the IR3859 for programming the output voltage

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. From (1), for a desired start-up time of the converter, the soft start capacitor can be calculated by using:

$$C_{SS}(\mu F) = T_{start}\ (\text{ms}) \times 0.02857 \quad \text{.....(10)}$$

Where T_{start} is the desired start-up time (ms).
For a start-up time of 3.5ms, the soft-start capacitor will be 0.099µF. Choose a 0.1µF ceramic capacitor.

Bootstrap Capacitor Selection

To drive the Control FET, it is necessary to supply a gate voltage at least 4V greater than the voltage at the SW pin, which is connected the source of the Control FET . This is achieved by using a bootstrap configuration, which comprises the internal bootstrap diode and an external bootstrap capacitor (C6), as shown in Fig. 13. The operation of the circuit is as follows: When the lower MOSFET is turned on, the capacitor node connected to SW is pulled down to ground. The capacitor charges towards V_{cc} through the internal bootstrap diode, which has a forward voltage drop V_D. The voltage V_c across the bootstrap capacitor C6 is approximately given as

$$V_c \cong V_{cc} - V_D \quad \text{.....(11)}$$

When the upper MOSFET turns on in the next cycle, the capacitor node connected to SW rises to the bus voltage V_{in}. However, if the value of C6 is appropriately chosen, the voltage *Vc*

across C6 remains approximately unchanged and the voltage at the Boot pin becomes:

$$V_{Boot} \cong V_{in} + V_{cc} - V_D \quad \text{.....(12)}$$

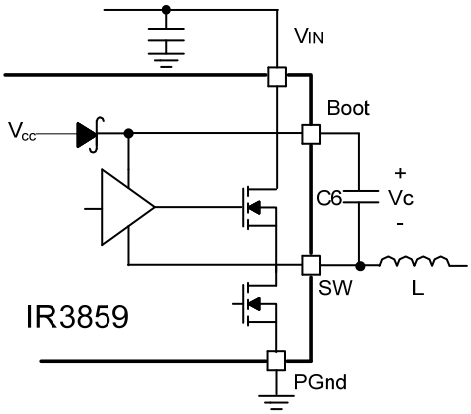


Fig. 13. Bootstrap circuit to generate Vc voltage

A bootstrap capacitor of value 0.1uF is suitable for most applications.

Input Capacitor Selection

The ripple current generated during the on time of the upper MOSFET should be provided by the input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_o * \sqrt{D*(1-D)} \quad \text{.....(13)}$$

$$D = \frac{V_o}{V_{in}} \quad \text{.....(14)}$$

Where:

D is the Duty Cycle

I_{RMS} is the RMS value of the input capacitor current.

Io is the output current.

For I_o=9A and D = 0.15, the I_{RMS} = 3.21A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency which enables better efficiency. For this application, it is advisable to have 4x10uF 25V ceramic capacitors C3216X5R1E106M from TDK. In addition to these, although not mandatory, a 1X330uF, 25V SMD capacitor EEV-FK1E331P may also be used as a bulk capacitor and is recommended if the input power supply is not located close to the converter.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of the inductor value can be reduced to the desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for the desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t}; \quad \Delta t = D * \frac{1}{F_s}$$
$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{..... (15)}$$

Where:

V_{in} = Maximum input voltage

V_o = Output Voltage

Δi = Inductor ripple current

F_s = Switching frequency

Δt = Turn on time

D = Duty cycle

If $\Delta i \approx 42\%(I_o)$, then the output inductor is calculated to be 0.69µH. Select L=0.68 µH.

The ETQP4LR68XFC from Panasonic provides a compact inductor suitable for this application.

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors type and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components. These components can be described as

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in} - V_o}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s} \quad \text{.....(16)}$$

ΔV_o = Output voltage ripple

ΔI_L = Inductor ripple current

Since the output capacitor has a major role in the overall performance of the converter and determines the result of transient response, selection of the capacitor is critical. The IR3859 can perform well with all types of capacitors.

As a rule, the capacitor must have low enough ESR to meet output ripple and load transient requirements.

The goal for this design is to meet the voltage ripple requirement in the smallest possible capacitor size. Therefore it is advisable to select ceramic capacitors due to their low ESR and ESL and small size. Six of the TDK C2102X5R0J226M (22uF, 6.3V, 3mOhm) capacitors is a good choice.

Feedback Compensation

The IR3859 is a voltage mode controller. The control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed-loop transfer function with the highest 0 dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 13). The resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2 * \pi \sqrt{L_o * C_o}} \quad \text{.....(17)}$$

Figure 14 shows gain and phase of the LC filter. Since we already have 180º phase shift from the output filter alone, the system runs the risk of being unstable.

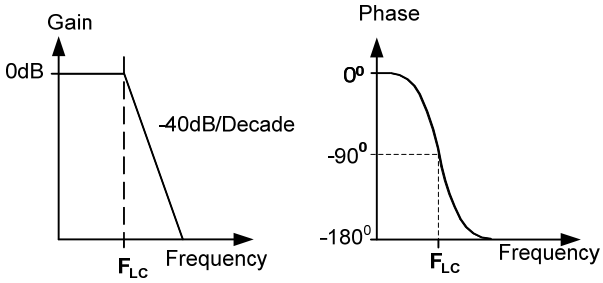


Fig. 14. Gain and Phase of LC filter

The IR3859 uses a voltage-type error amplifier with high-gain (110dB) and wide-bandwidth. The output of the amplifier is available for DC gain control and AC phase compensation.

The error amplifier can be compensated either in Type-II or Type-III compensation.

Local feedback with Type-II compensation is shown in figure 14.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, for Type-II compensation the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor is expressed as follows:

$$F_{ESR} = \frac{1}{2 * \pi * ESR * C_o} \quad \text{.....(18)}$$

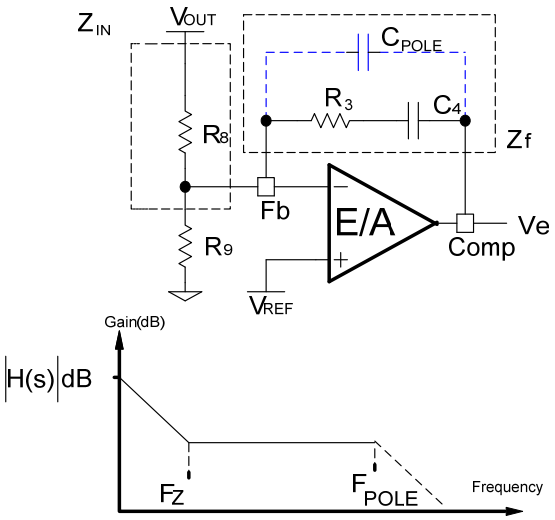


Fig. 15. Type II compensation network and its asymptotic gain plot

The transfer function (V_e/V_o) is given by:

$$\frac{V_e}{V_o} = H(s) = -\frac{Z_f}{Z_{IN}} = -\frac{1+sR_3C_4}{sR_8C_4} \quad .....(19)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$\left|H(s)\right| = \frac{R_3}{R_8} \quad ..... (20)$$

$$F_z = \frac{1}{2\pi * R_3 * C_4} \quad ..... (21)$$

First select the desired zero-crossover frequency (F_o):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R3:

$$R_3 = \frac{V_{osc} * F_o * F_{ESR} * R_8}{V_{in} * F_{LC}^2} \quad .....(22)$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_8 = Feedback Resistor

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$
$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad .....(23)$$

Use equations (21), (22) and (23) to calculate C4.
One more capacitor is sometimes added in parallel with C4 and R3. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_3 * \frac{C_4 * C_{POLE}}{C_4 + C_{POLE}}} \quad .....(24)$$

The pole sets to one half of the switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_3 * F_s - \frac{1}{C_4}} \cong \frac{1}{\pi * R_3 * F_s} \quad .....(25)$$

For a general solution for unconditional stability for any type of output capacitors, and a wide range of ESR values, we should implement local feedback with a Type-III compensation network. The typically used compensation network for voltage-mode controller is shown in figure 16.

Again, the transfer function is given by:

$$\frac{V_e}{V_o} = H(s) = -\frac{Z_f}{Z_{IN}}$$

By replacing Z_{in} and Z_f according to figure 16, the transfer function can be expressed as:

$$H(s) = \frac{-(1+sR_3C_4)[1+sC_7(R_8+R_{10})]}{sR_8(C_4+C_3)\left[1+sR_3\left(\frac{C_4*C_3}{C_4+C_3}\right)\right](1+sR_{10}C_7)}$$
$$.....(26)$$

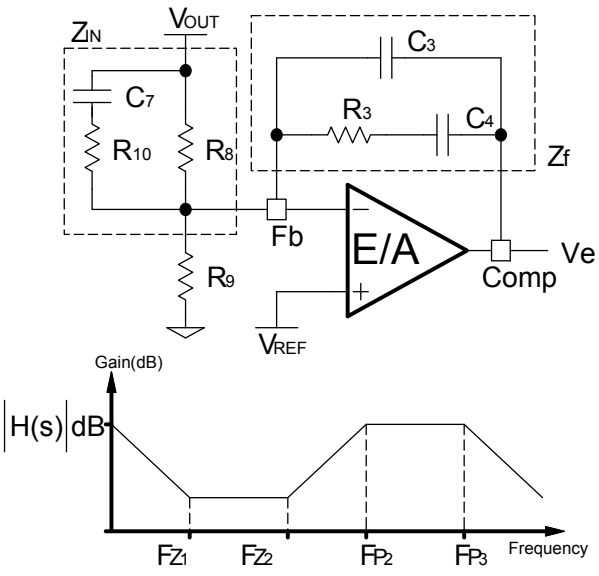


Fig.16. Type III Compensation network and its asymptotic gain plot

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0 \quad \text{.....(27)}$$

$$F_{P2} = \frac{1}{2\pi * R_{10} * C_7} \quad \text{.....(28)}$$

$$F_{P3} = \frac{1}{2\pi * R_3 \left(\frac{C_4 * C_3}{C_4 + C_3} \right)} \cong \frac{1}{2\pi * R_3 * C_3} \quad \text{.....(29)}$$

$$F_{Z1} = \frac{1}{2\pi * R_3 * C_4} \quad \text{.....(30)}$$

$$F_{Z2} = \frac{1}{2\pi * C_7 * (R_8 + R_{10})} \cong \frac{1}{2\pi * C_7 * R_8} \quad \text{.....(31)}$$

Cross over frequency is expressed as:

$$F_o = R_3 * C_7 * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o} \quad \text{.....(32)}$$

Based on the frequency of the zero generated by the output capacitor and its ESR, relative to crossover frequency, the compensation type can be different. The table below shows the compensation types for relative locations of the crossover frequency.

Compensator Type	F_{ESR} vs F_o	Output Capacitor
Type II	$F_{LC}<F_{ESR}<F_o<F_s/2$	Electrolytic Tantalum
Type III	$F_{LC}<F_o<F_{ESR}$	Tantalum Ceramic

The higher the crossover frequency, the potentially faster the load transient response. However, the crossover frequency should be low enough to allow attenuation of switching noise. Typically, the control loop bandwidth or crossover frequency is selected such that

$$F_o \leq (1/5 \sim 1/10) * F_s$$

The DC gain should be large enough to provide high DC-regulation accuracy. The phase margin should be greater than 45º for overall stability.

For this design we have:
V_{in}=12V
V_o=1.8V
V_{osc}=1.8V
V_{ref}=0.7V
L_o=0.68uH
C_o=6x22uF, ESR=3mOhm each

It must be noted here that the value of the capacitance used in the compensator design must be the small signal value. For instance, the small signal capacitance of the 22uF capacitor used in this design (i.e. C3216X5R1E106M from TDK) is 9.5uF at 1.8 V DC bias and 600 kHz frequency. It is this value that must be used for all computations related to the compensation. The small signal value may be obtained from the manufacturer's datasheets, design tools or SPICE models. Alternatively, they may also be inferred from measuring the power stage transfer function of the converter and measuring the double pole frequency F_{LC} and using equation (16) to compute the small signal C_o.

These result to:
F_{LC}=25.5 kHz
F_{ESR}=5.5 MHz
$F_s/2$=300 kHz

Select crossover frequency **F_o=100 kHz**
Since $F_{LC}<F_o<F_s/2<F_{ESR}$, Type-III is selected to place the pole and zeros.

Detailed calculation of compensation Type-III

Desired Phase Margin $\Theta = 70^{o}$

$$F_{Z2} = F_o\sqrt{\frac{1-sin\,\Theta}{1+sin\,\Theta}} = 17.63\ \text{kHz}$$

$$F_{P2} = F_o\sqrt{\frac{1+sin\,\Theta}{1-sin\,\Theta}} = 567.1\text{kHz}$$

Select: $F_{Z1} = 0.5 * F_{Z2} = 8.82\ \text{kHz}$ and

$F_{P3} = 0.5 * F_s = 300\ \text{kHz}$

Select $C_7 = 2.2\text{nF}$

Calculate R_3, C_3 and C_4:

$$R_3 = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{C_7 * V_{in}};\ R_3 = 1.66\ \text{k}\Omega$$

Select: $R_3 = 1.65\,\text{k}\Omega$

$$C_4 = \frac{1}{2\pi * F_{Z1} * R_3};\ C_4 = 10.94\ \text{nF},\ \text{Select}\ C_4 = 10\ \text{nF}$$

$$C_3 = \frac{1}{2\pi * F_{P3} * R_3};\ C_3 = 321\,\text{pF},\ \text{Select}\ C_3 = 270\ \text{pF}$$

Calculate R_{10}, R_8 and R_9:

$$R_{10} = \frac{1}{2\pi * C_7 * F_{P2}};\ R_{10} = 128\ \Omega,\ \text{Select}\ R_{10} = 130\ \Omega$$

$$R_8 = \frac{1}{2\pi * C_7 * F_{Z2}} - R_{10};\ R_8 = 3.97\ \text{k}\Omega,$$

Select $R_8 = 4.02\,\text{k}\Omega$

$$R_9 = \frac{V_{ref}}{V_o - V_{ref}} * R_8;\ R_9 = 2.56\,\text{k}\Omega\ \ \text{Select}\ R_9 = 2.55\,\text{k}\Omega$$

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{OCSET}) from the SW pin to the OCSet pin. The resistor can be calculated by using equation (4). This resistor R_{OCSET} must be placed close to the IC.

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worst case operation.

$$I_{SET} = I_{L\,(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS\,(on)}} \quad \text{.....(32)}$$

$$R_{DS(on)} = 11\ \text{m}\Omega * 1.25 = 13.75\ \text{m}\Omega$$

$$I_{SET} \cong I_{o(LIM)} = 9\ \text{A} * 1.5 = 13.5\ \text{A}$$
(50% over nominal output current)

$I_{OCSet} = 59.07\ \mu\text{A}$ (at $F_s = 600\,\text{kHz}$)

$R_{OCSet} = 3.14\ \text{k}\Omega$ Select $R_7 = 3.16\ \text{k}\Omega$

Setting the Power Good Threshold

Power Good threshold can be programmed by using two external resistors (R5, R7 on Page 24).

The following formula can be used to set the threshold:

$$R_6 = \left(\frac{V_{o(PGood_TH)}}{0.85 * V_{ref}} - 1\right) * R_7 \quad \text{--(33)}$$

Where: 0.85*Vref is reference of the internal comparator, for IR3859.
$V_{o(PGood_TH)}$ is the selectable output voltage threshold for power good, for this design it is 1.53V (i.e. 0.85*1.8V).

Select R_7=2.55KOhm

Using (24): R_5=3.97KOhm

Select R_6=4.02KOhm

The PGood is an open drain output. Hence, it is necessary to use a pull up resistor R_{PG} from PGood pin to Vcc. The value of the pull-up resistor must be chosen such as to limit the current flowing into the PGood pin, when the output voltage is not in regulation, to less than 5 mA. A typical value used is 10kΩ.

Application Diagram:

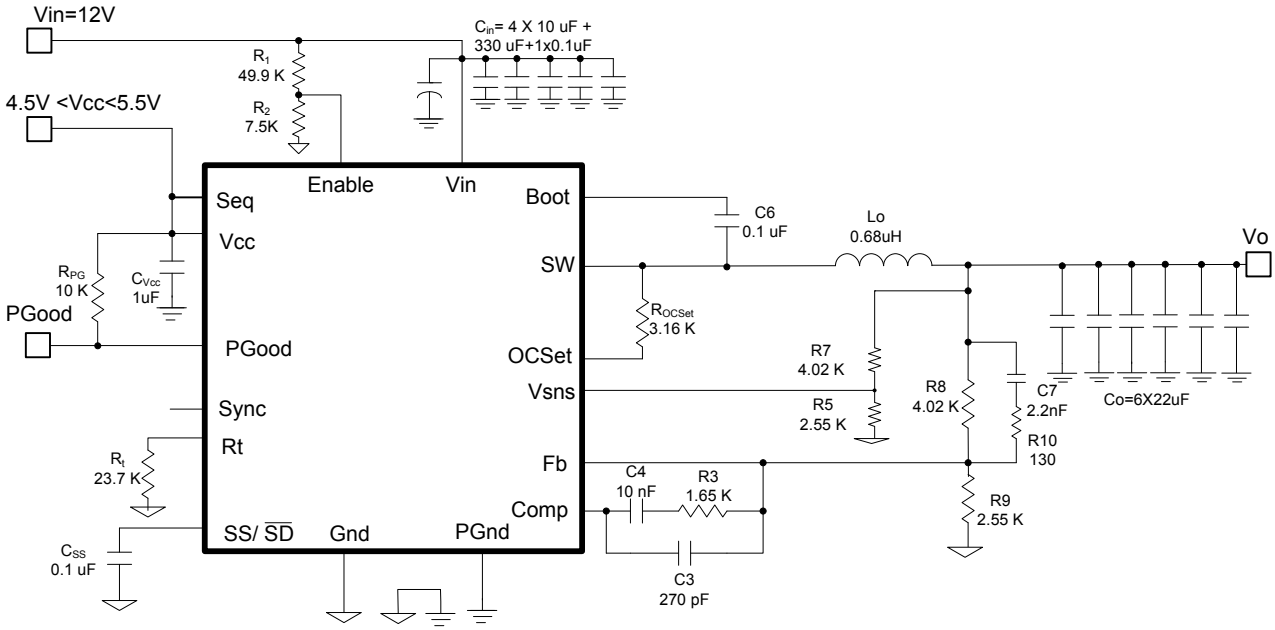


Fig. 17. Application circuit diagram for a 12V to 1.8 V, 9A Point Of Load Converter

Suggested Bill of Materials for the application circuit:

Part Reference	Quantity	Value	Description	Manufacturer	Part Number
Cin	1	330uF	SMD Elecrolytic, Fsize, 25V, 20%	Panasonic	EEV-FK1E331P
	4	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
	1	0.1uF	0603, 25V, X7R, 10%	Panasonic	ECJ-1VB1E104K
Lo	1	0.68uH	11.7x10x4mm, 20%, 1.58mOhm	Panasonic	ETQP4LR68XFC
Co	6	22uF	0805, 6.3V, X5R, 20%	TDK	C2102X5R0J226M
R1	1	49.9k	Thick Film, 0603,1/10 W,1%	Rohm	MCR03EZPFX4992
R2	1	7.5k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX7501
R_t	1	23.7k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2372
R_{PG}	1	10k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1002
C_{ss} C6	2	0.1uF	0603, 25V, X7R, 10%	Panasonic	ECJ-1VB1E104K
R3	1	1.65k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX1651
C3	1	270pF	50V, 0603, NPO, 5%	Panasonic	ECJ-1VC1H271J
C4	1	10nF	0603, 50V, X7R, 10%	Panasonic	ECJ-1VB1H103K
R8 R6	2	4.02k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX4021
R9 R5	2	2.55k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX2551
Rocset	1	3.16k	Thick Film, 0603,1/10W,1%	Rohm	MCR03EZPFX3161
R10	1	130	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1300V
C7	1	2200pF	0603, 50V, X7R, 10%	Panasonic	ECJ-1VB1H222K
C_{Vcc}	1	1.0uF	0603, 16V, X5R, 20%	Panasonic	ECJ-BVB1C105M
U1	1	IR3859	SupIRBuck, 9A, PQFN 4x5mm	International Rectifier	IR3859MPbF

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vcc=5V, Vo=1.8V, Io=0-9A, Room Temperature, No Air Flow

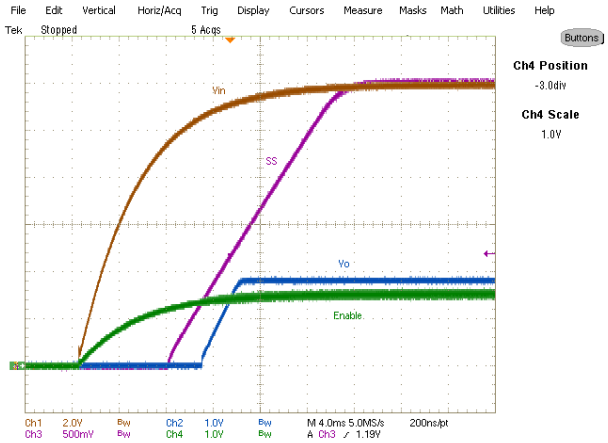


Fig. 18: Start up at 9A Load
Ch_1:V_{in}, Ch_2:V_{out}, Ch_3:V_{ss}, Ch_4:Enable

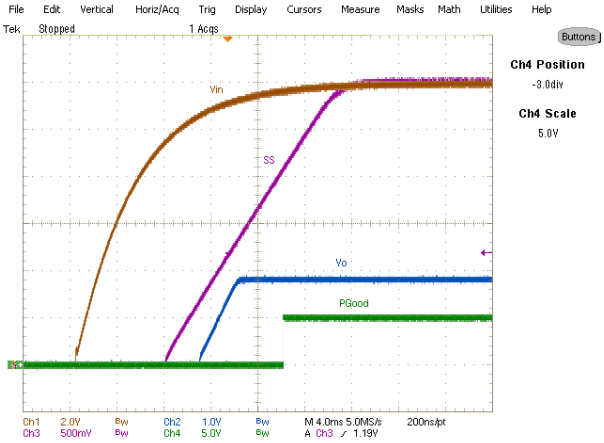


Fig. 19: Start up at 9A Load,
Ch_1:V_{in}, Ch_2:V_{out}, Ch_3:V_{ss}, Ch_4:V_{PGood}

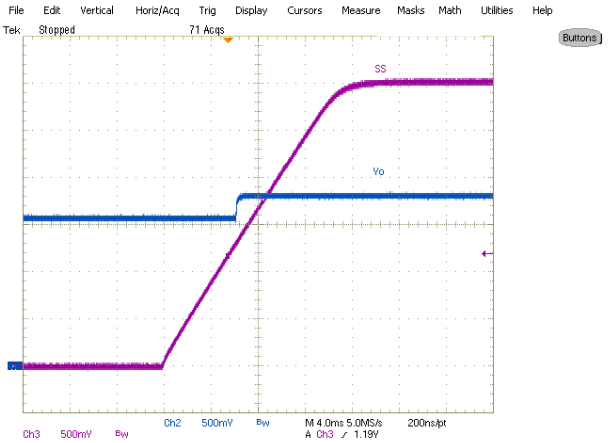


Fig. 20: Start up with 1.62V Pre-Bias, 0A Load, Ch_2:V_{out}, Ch_3:V_{SS}

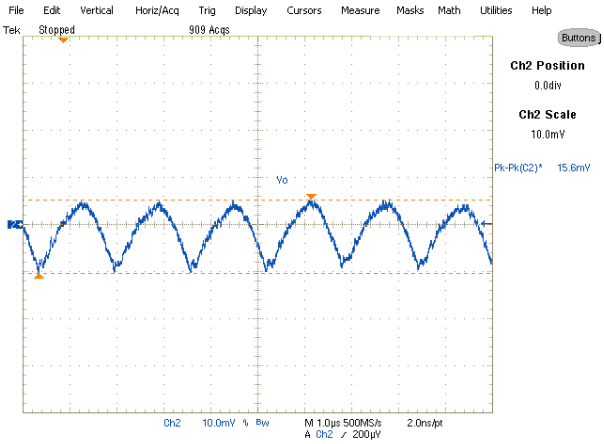


Fig. 21: Output Voltage Ripple, 9A load Ch_2: V_{out}

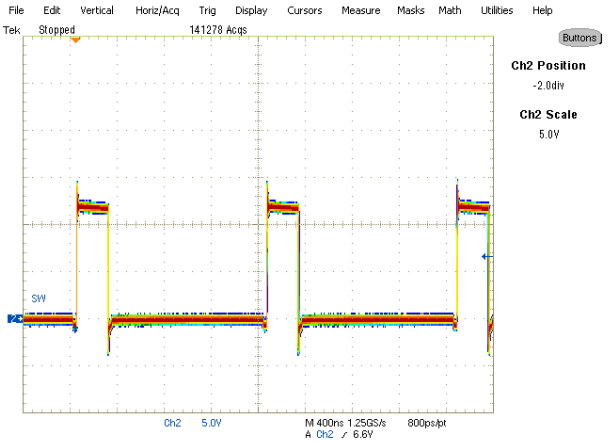


Fig. 22: Inductor node at 9A load
Ch_2: Switch Node

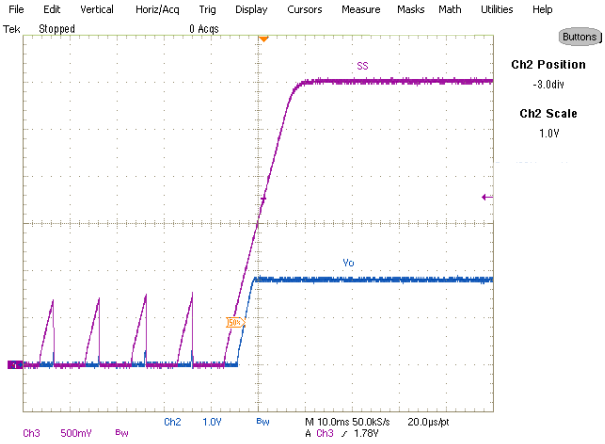


Fig. 23: Short (Hiccup) Recovery
Ch_2:V_{out} , Ch_3:V_{ss}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=4.5A- 9A, Room Temperature, No Air Flow

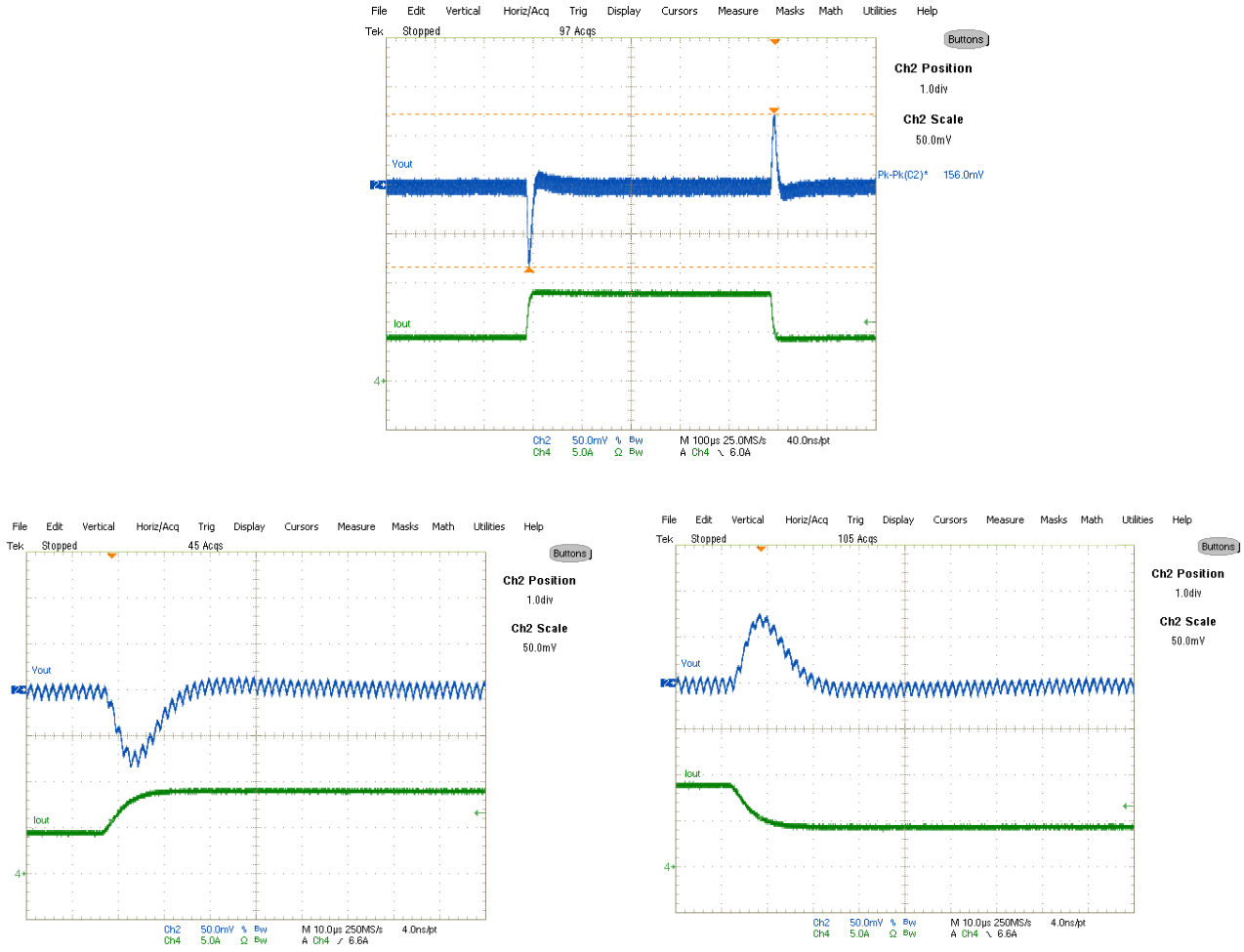


Fig. 24: Transient Response, 4.5A to 9A step 2.5A/µs
Ch_2:V_{out}, Ch_4:I_{out}

TYPICAL OPERATING WAVEFORMS
Vin=12V, Vcc=5V, Vo=1.8V, Io=9A, Room Temperature, No Air Flow

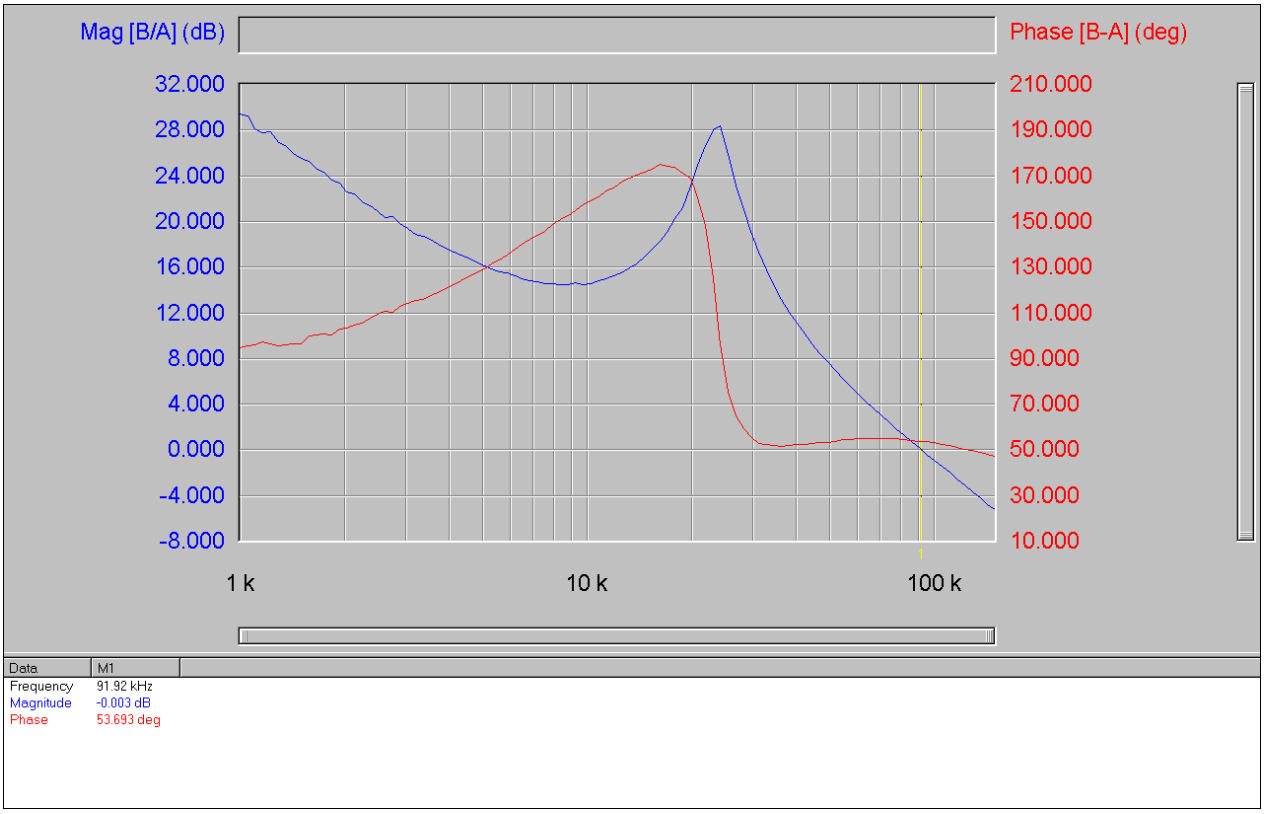


Fig. 25: Bode Plot at 9A load shows a bandwidth of 92kHz and phase margin of 54 degrees

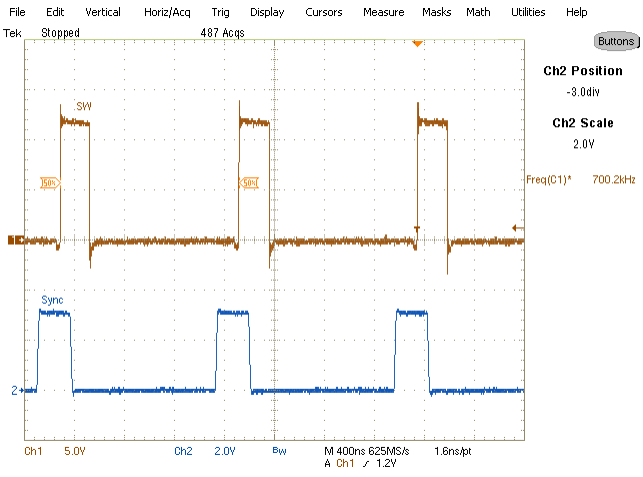
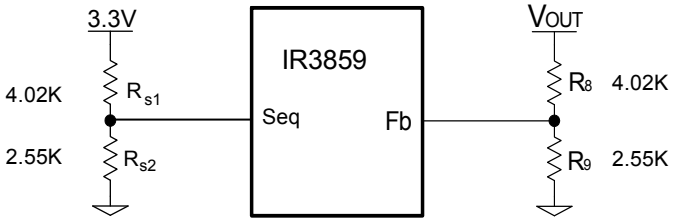
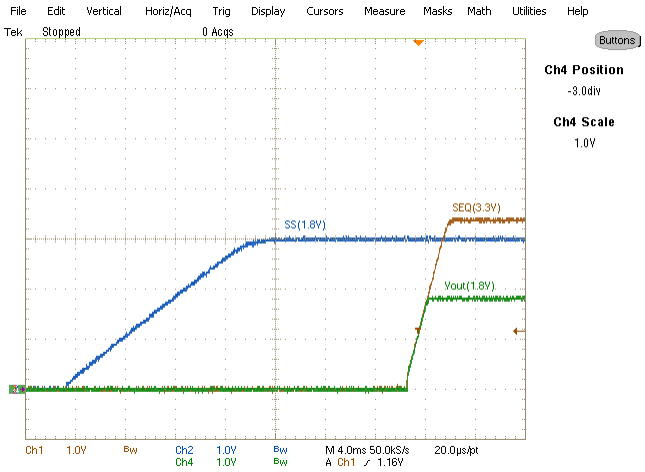


Fig. 26: Synchronization to 700kHz external clock signal at 9A load
Ch_1: SW (Switch Node) Ch_2:Sync

TYPICAL OPERATING WAVEFORMS
Simultaneous Tracking at Power Up and Power Down
Vin=12V, Vo=1.8V, Io=9A, Room Temperature, No Air Flow





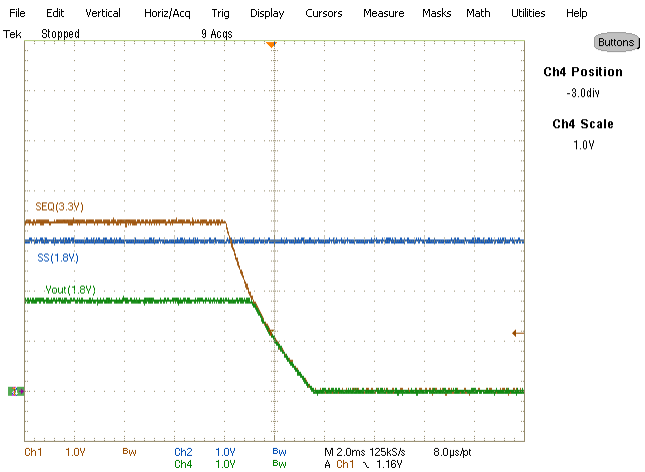


Fig. 27: Simultaneous Tracking a 3.3V input at power-up and shut-down
Ch_1: SEQ(3.3V) Ch_2:SS(1.8V) Ch_4: Vout(1.8V)

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make all the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

The inductor, output capacitors and the IR3859 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the Vin pin of IR3859.

The feedback part of the system should be kept away from the inductor and other noise sources.

The critical bypass components such as capacitors for Vcc should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

The connection between the OCSet resistor and the SW pin should not share any trace with the connection between the bootstrap capacitor and the SW pin. Instead, it is recommended to use a Kelvin connection of the trace from the OCSet resistor and the trace from the bootstrap capacitor at the SW pin.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figure 28 illustrates the implementation of the layout guidelines outlined above, on the IRDC3859 4 layer demoboard.

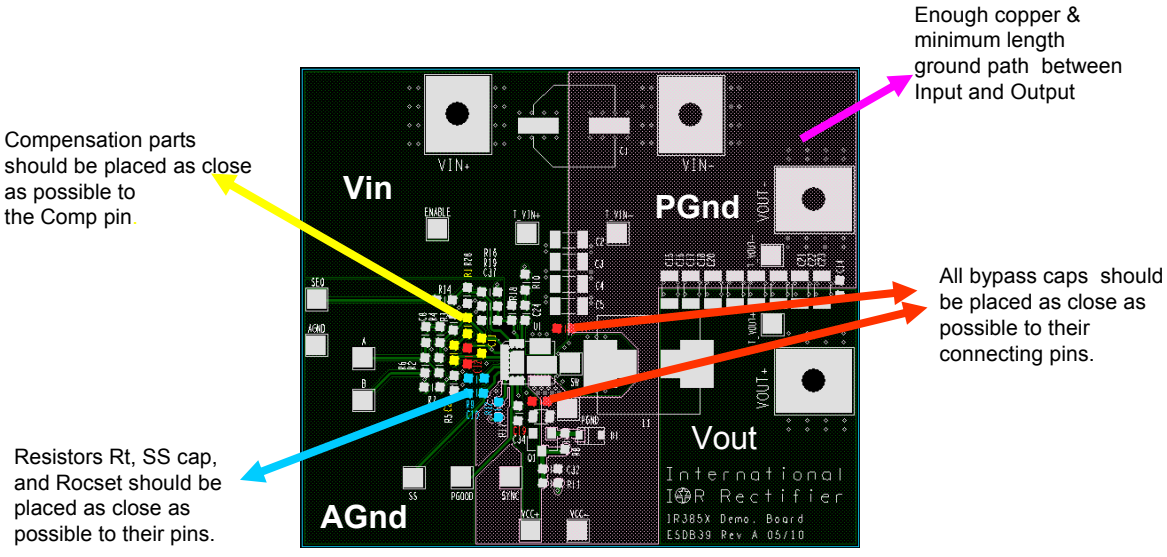
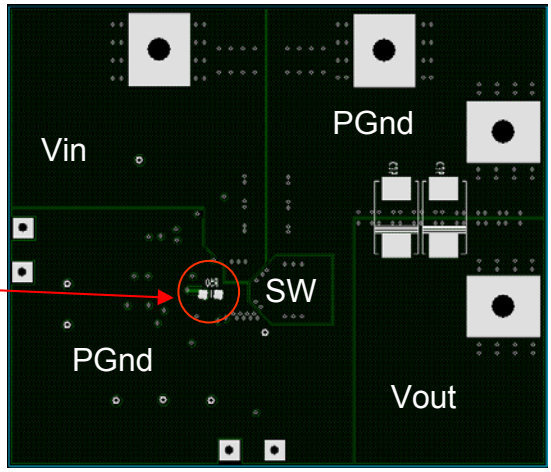


Fig. 28a. IRDC3859 demoboard layout considerations – Top Layer



Single point connection between AGND & PGND; It should be close to the SupIRBuck, kept away from noise sources.

Fig. 28b. IRDC3859 demoboard layout considerations – Bottom Layer

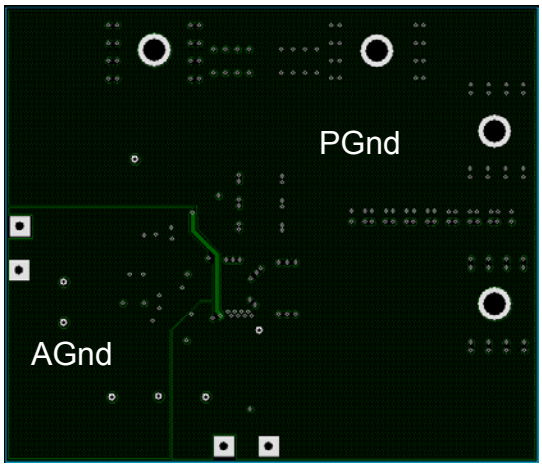
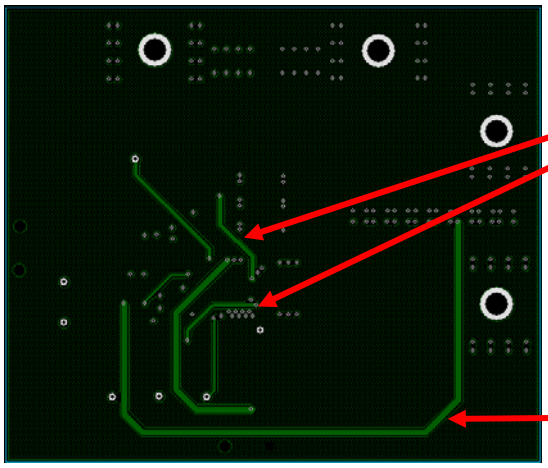


Fig. 28c. IRDC3859 demoboard layout considerations – Mid Layer 1



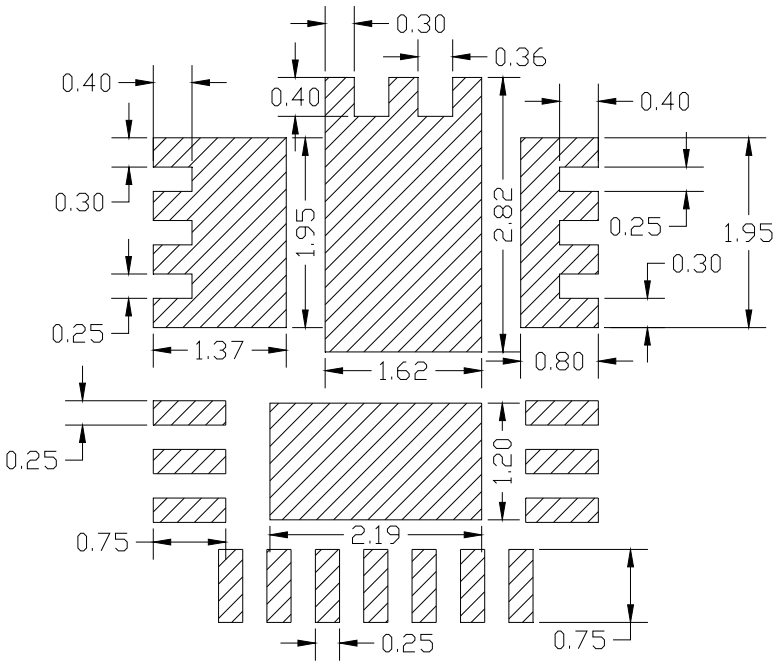
Use separate trace for connecting Boost cap and Rocset to the switch node and with the minimum length traces. Avoid big loops.

Feedback trace should be kept away form noise sources

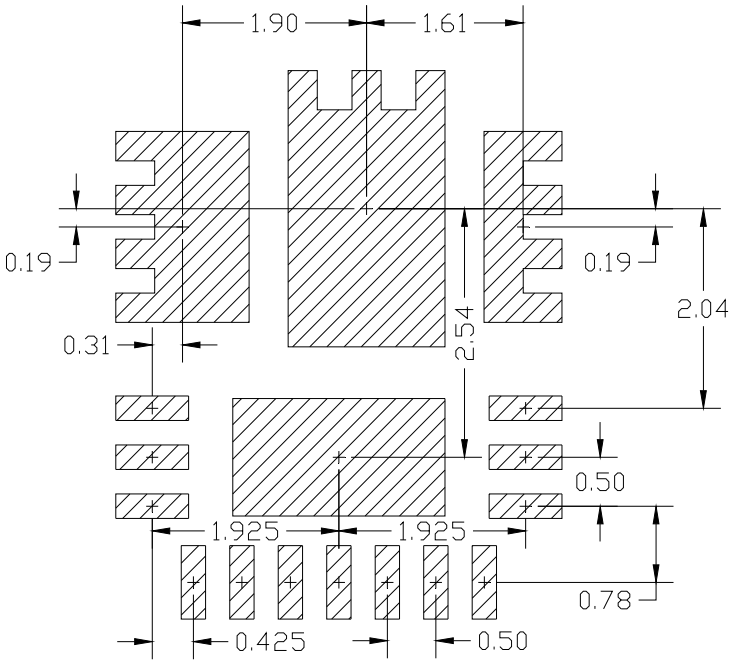
Fig. 28d. IRDC3859 demoboard layout considerations – Mid Layer 2

PCB Metal and Components Placement

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to "SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note." (AN-1132)



PCB metal pad sizing (all dimensions in mm)



PCB metal pad spacing (all dimensions in mm)

Solder Resist

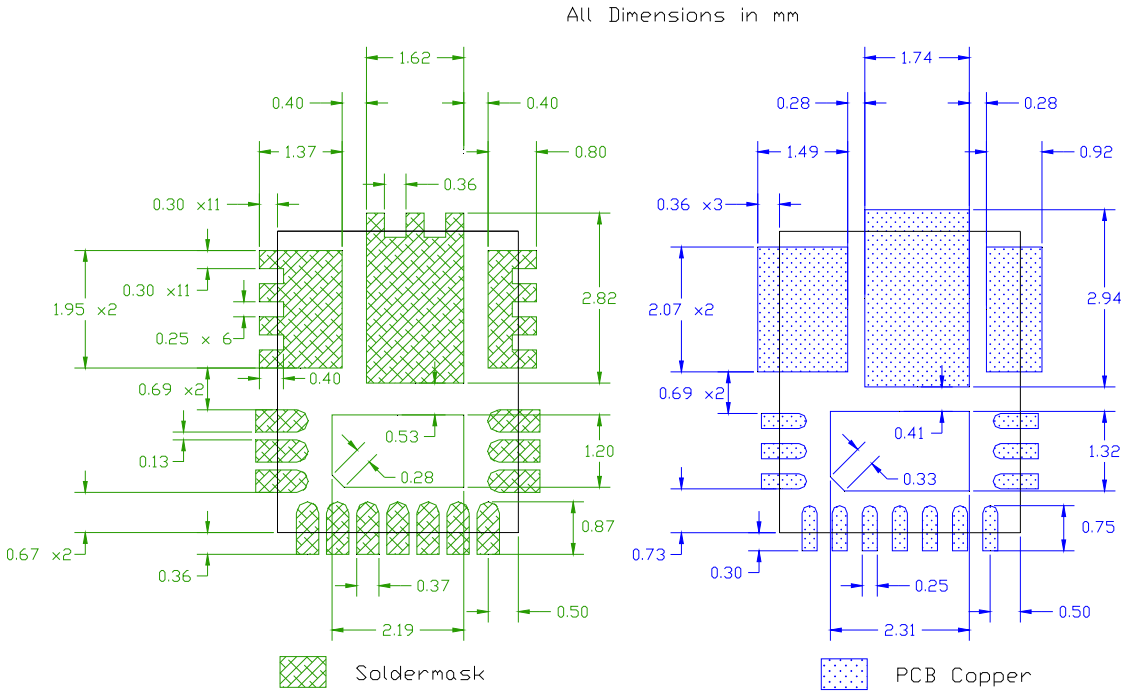
IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability.

When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)

However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined or Copper Defined.

When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment.

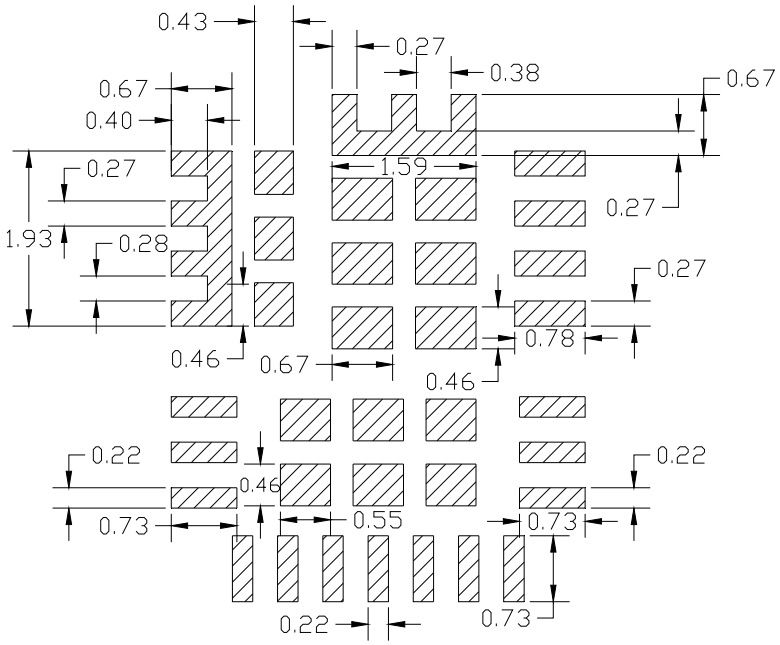
Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.



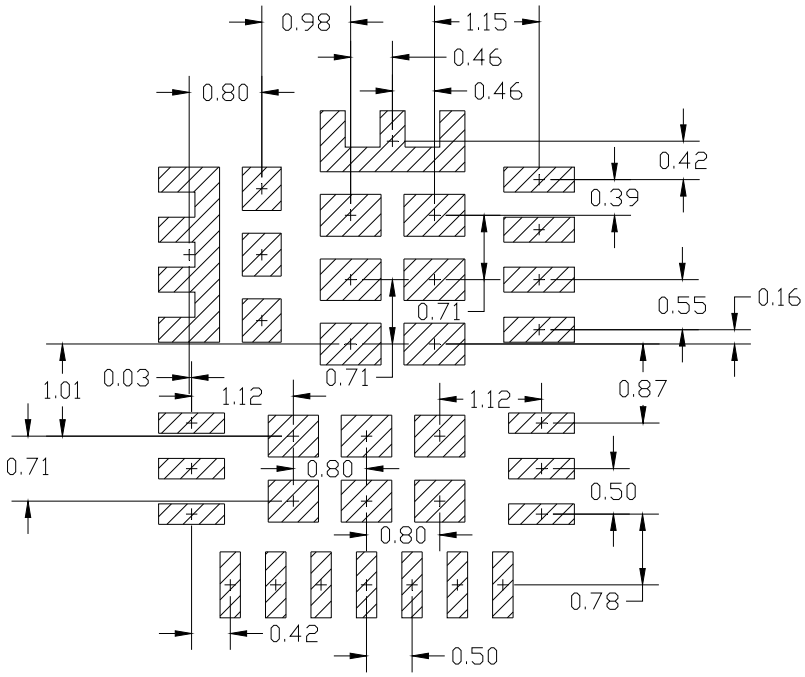
Stencil Design

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

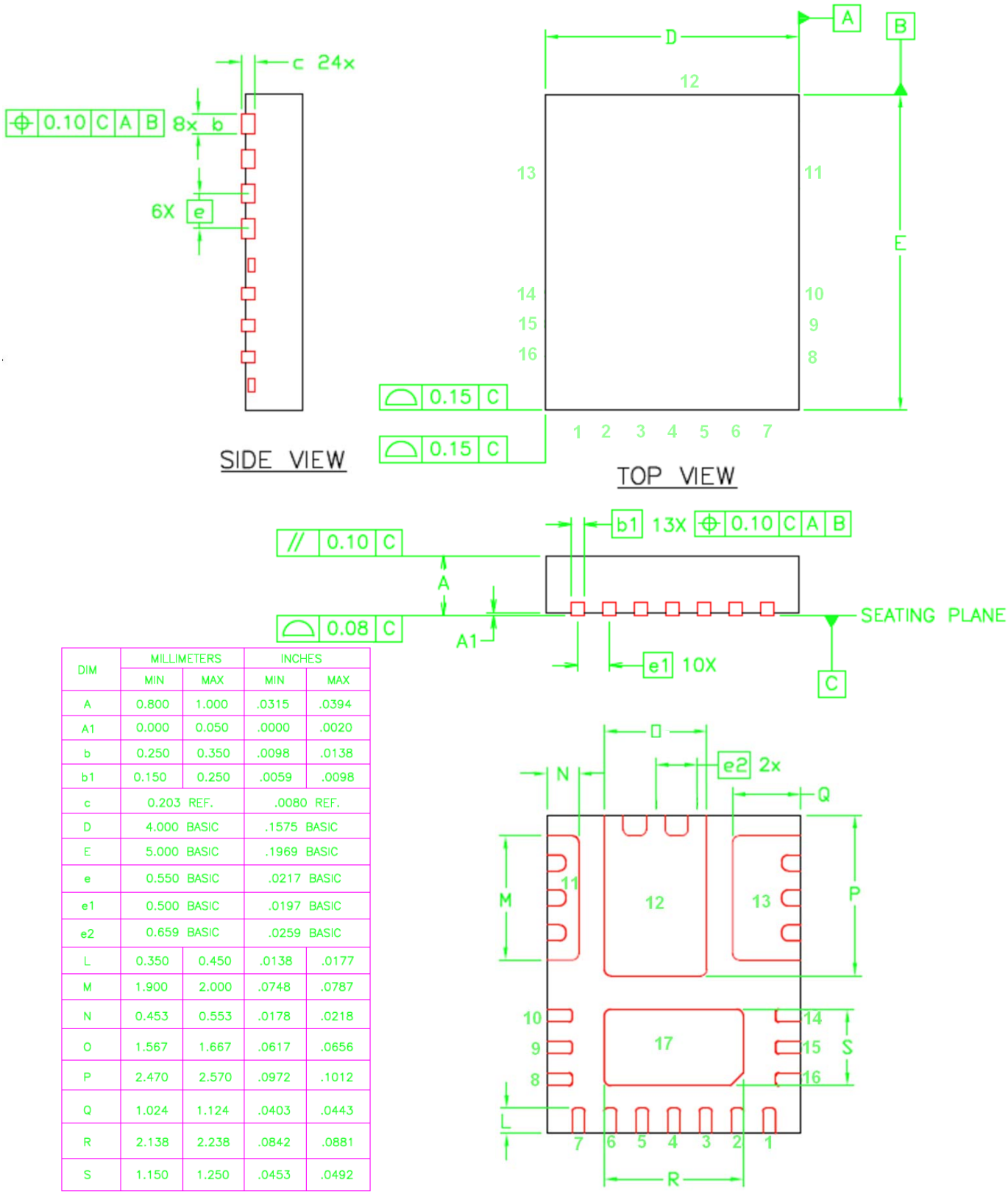
Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.



Stencil pad sizing (all dimensions in mm)



Stencil pad spacing (all dimensions in mm)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.250	0.350	.0098	.0138
b1	0.150	0.250	.0059	.0098
c	0.203 REF.		.0080 REF.	
D	4.000 BASIC		.1575 BASIC	
E	5.000 BASIC		.1969 BASIC	
e	0.550 BASIC		.0217 BASIC	
e1	0.500 BASIC		.0197 BASIC	
e2	0.659 BASIC		.0259 BASIC	
L	0.350	0.450	.0138	.0177
M	1.900	2.000	.0748	.0787
N	0.453	0.553	.0178	.0218
O	1.567	1.667	.0617	.0656
P	2.470	2.570	.0972	.1012
Q	1.024	1.124	.0403	.0443
R	2.138	2.238	.0842	.0881
S	1.150	1.250	.0453	.0492

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