FAIRCHILD SEMICONDUCTOR™

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# DM74ALS533
# Octal D-Type Transparent Latch with 3-STATE Outputs

## General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the DM74ALS533 are transparent D-type latches. While the enable (G) is HIGH the Q outputs will follow the complement of the data (D) inputs. When the enable is taken LOW the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (HIGH or LOW logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are OFF.

## Features

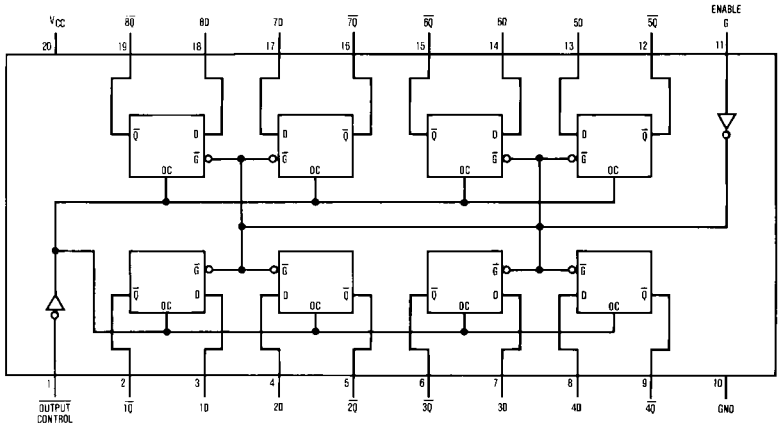
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and $V_{CC}$ range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM74ALS533WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| DM74ALS533N | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




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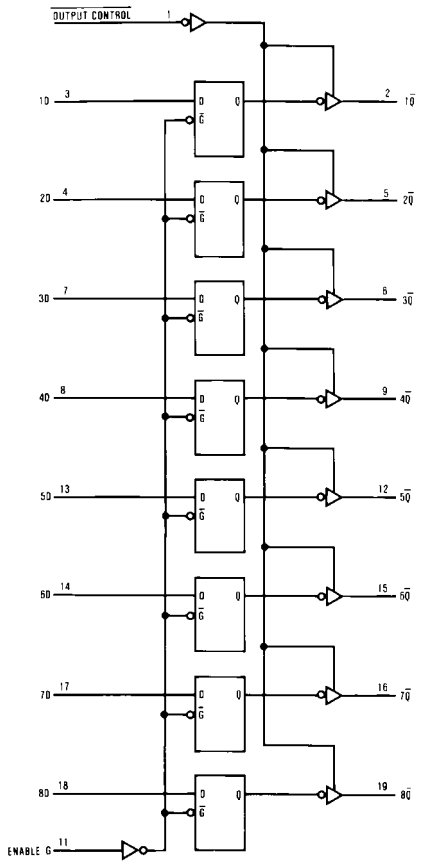
## Function Table

| $\overline{\text{Output}}$ Control | Enable G | D | Output $\overline{Q}$ |
|---|---|---|---|
| L | H | H | L |
| L | H | L | H |
| L | L | X | $\overline{Q}_0$ |
| H | X | X | Z |

L = LOW State
H = HIGH State
X = Don't Care
Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

## Logic Diagram



## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Voltage Applied to Disabled Output | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Typical $\theta_{JA}$ | |
| N Package | 57.0°C/W |
| M Package | 76.0°C/W |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | HIGH Level Input Voltage | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | −2.6 | mA |
| $I_{OL}$ | LOW Level Output Current | | | 24 | mA |
| $t_W$ | Width of Enable Pulse, HIGH or LOW | 15 | | | ns |
| $t_{SU}$ | Data Setup Time (Note 2) | 15↓ | | | ns |
| $t_H$ | Data Hold Time (Note 2) | 7↓ | | | ns |
| $T_A$ | Free Air Operating Temperature | 0 | | 70 | °C |

**Note 2:** The (↓) arrow indicates the negative edge of the enable is used for reference.

## Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

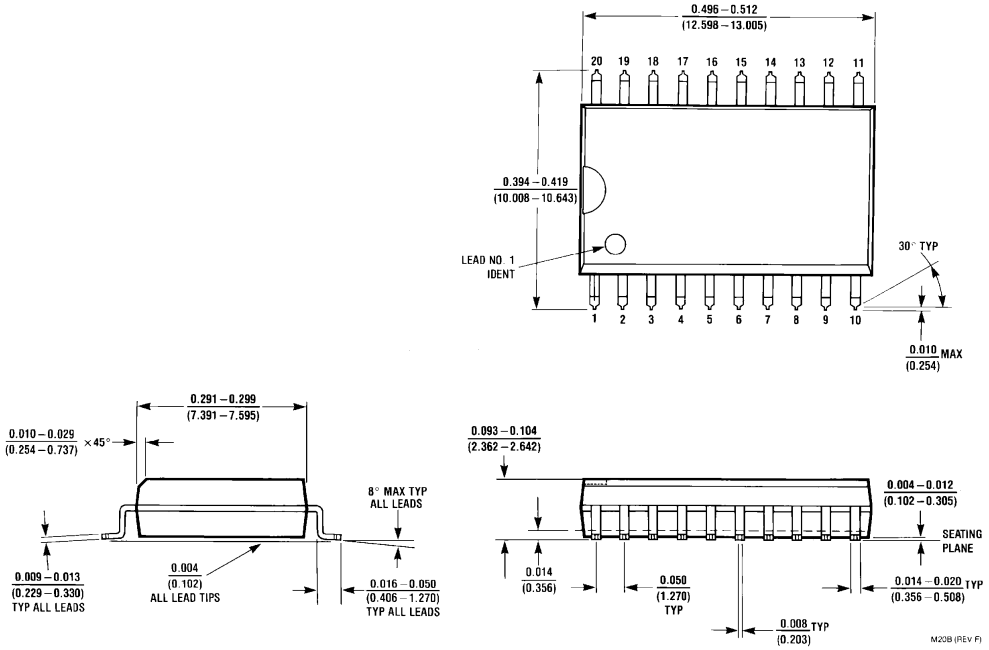
| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 4.5V, $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = 4.5V | $I_{OH}$ = −2.6 mA | 2.4 | 3.3 | | V |
| | | $V_{CC}$ = 4.5V to 5.5V | $I_{OH}$ = −400 µA | $V_{CC}$ − 2 | | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = 4.5V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | 0.35 | 0.5 | V |
| $I_I$ | Input Current @ Maximum Input Voltage | $V_{CC}$ = 5.5V, $V_{IH}$ = 7V | | | | 0.1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = 5.5V, $V_{IH}$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = 5.5V, $V_{IL}$ = 0.4V | | | | −0.1 | mA |
| $I_O$ | Output Drive Current | $V_{CC}$ = 5.5V | $V_O$ = 2.25V | −30 | | −112 | mA |
| $I_{OZH}$ | OFF-State Output Current HIGH Level Voltage Applied | $V_{CC}$ = 5.5V, $V_O$ = 2.7V | | | | 20 | µA |
| $I_{OZL}$ | OFF-State Output Current LOW Level Voltage Applied | $V_{CC}$ = 5.5V, $V_O$ = 0.4V | | | | −20 | µA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5.5V, Outputs OPEN | Outputs HIGH | | 10 | 17 | mA |
| | | | Outputs LOW | | 17 | 26 | mA |
| | | | Outputs Disabled | | 18.5 | 28 | mA |

## Switching Characteristics

over recommended operating free air temperature range

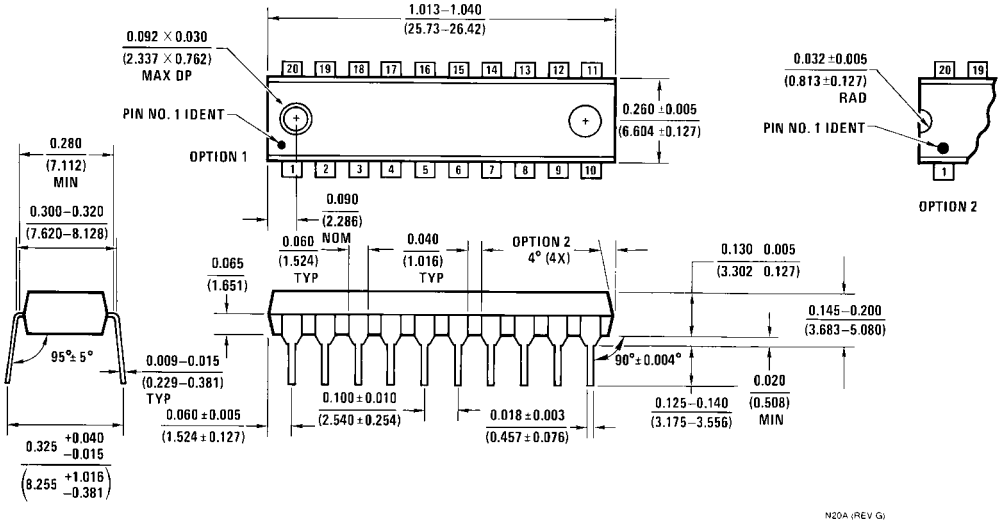
| Symbol | Parameter | Conditions | From | To | Min | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | $V_{CC}$ = 4.5V to 5.5V<br>$R_L$ = 500Ω<br>$C_L$ = 50 pF | Data | Any $\overline{Q}$ | 4 | 19 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | | Data | Any $\overline{Q}$ | 4 | 13 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | | Enable | Any $\overline{Q}$ | 5 | 23 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | | Enable | Any $\overline{Q}$ | 4 | 18 | ns |
| $t_{PZH}$ | Output Enable Time to HIGH Level Output | | Output Control | Any $\overline{Q}$ | 4 | 17 | ns |
| $t_{PZL}$ | Output Enable Time to LOW Level Output | | Output Control | Any $\overline{Q}$ | 4 | 18 | ns |
| $t_{PHZ}$ | Output Disable Time from HIGH Level Output | | Output Control | Any $\overline{Q}$ | 2 | 10 | ns |
| $t_{PLZ}$ | Output Disable Time from LOW Level Output | | Output Control | Any $\overline{Q}$ | 3 | 16 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N20A**

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