DATA SHEET

CBTD3306
Dual bus switch with level shifting

Product data

2001 Nov 08

File under Integrated Circuits — ICL03

Philips
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Dual bus switch with level shifting CBTD3306

FEATURES

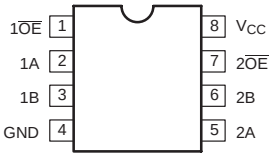
- Designed to be used in 5 V to 3.3 V level shifting applications with internal diode.
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Package options include plastic small outline (SO) and thin shrink small outline (TSSOP)
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

DESCRIPTION

The CBTD3306 Dual FET Bus Switch features independent line switches. Each switch is disabled with the associated Output Enable ($\overline{OE}$) input is high.

The CBTD3306 is characterized for operation from –40 to +85 °C.

PIN CONFIGURATION



SA00535

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 7	1$\overline{OE}$, 2$\overline{OE}$	Output enable
2, 5	1A, 2A	A port inputs
3, 6	1B, 2B	B port outputs
4	GND	Ground (0V)
8	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

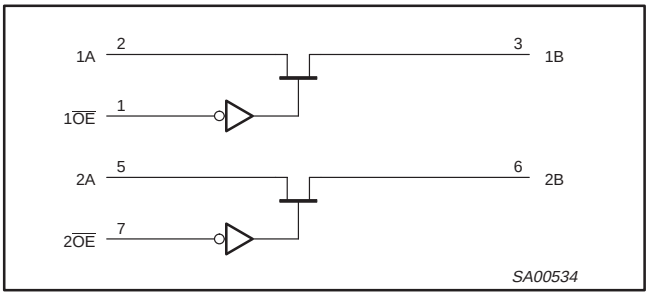
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A to B or B to A	C_L = 50 pF; V_{CC} = +5.0 V ±0.5 V	0.25 (MAX)	ns
$C_{IO(OFF)}$	Pin capacitance (OFF state)	V_O = 3 V or 0; $\overline{OE}$ = V_{CC}	6.50	pF
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND	3	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
8-pin plastic SO	–40 to 85 °C	CBTD3306D	SOT96-1
8-pin plastic TSSOP	–40 to 85 °C	CBTD3306PW	SOT530-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

LOGIC DIAGRAM (positive logic)



SA00534

FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

ABSOLUTE MAXIMUM RATINGS[1]

T_{amb} = –40 to +85 °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
V_I	DC input voltage[2]		–0.5 to +7.0	V
I_{OUT}	DC output current		128	mA
I_{IK}	Input diode current	$V_{I/O} < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The package thermal impedance is calculated in accordance with JESD 51.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

NOTE:
1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = –40 to +85 °C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = –40 to +85 °C			
			MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_I = –18 mA	—	—	–1.2	V
I_I	Input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±1	µA
I_{CC}	Quiescent supply current	V_{CC} = 5.5 V; I_O = 0, V_I = V_{CC} or GND	—	—	1.5	mA
V_P	Output high pass voltage	See Figure 1	—	—	—	V
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Control pins capacitance	V_I= 3 V or 0	—	3.20	—	pF
$C_{IO(OFF)}$	Port off capacitance	V_O = 3 V or 0; $\overline{OE}$ = V_{CC}	—	6.50	—	pF
r_{on} [3]	On-resistance	V_{CC} = 4.5 V; V_I = 0V; I_I = 64 mA	—	3.6	5	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	—	3.6	5	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	—	17	35	Ω

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

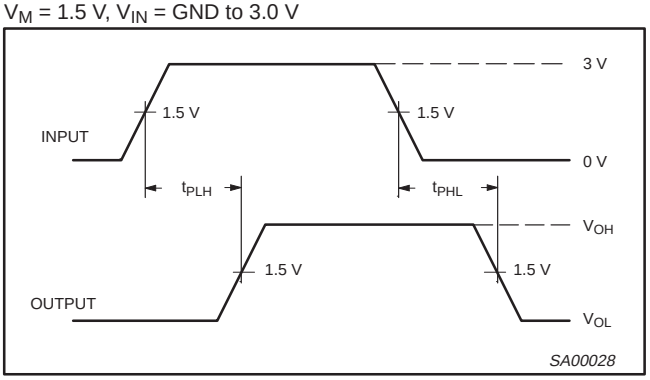
T_{amb} = –40 to +85 °C; C_L = 50 pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V_{CC} = +5.0 V ±0.5 V		
				MIN	MAX	
t_{pd}	Propagation delay[1]	A or B	B or A	—	0.25	ns
t_{en}	Output enable time to High and Low level	$\overline{OE}$	A or B	1	5	ns
t_{dis}	Output disable time from High and Low level	$\overline{OE}$	A or B	1	4.9	ns

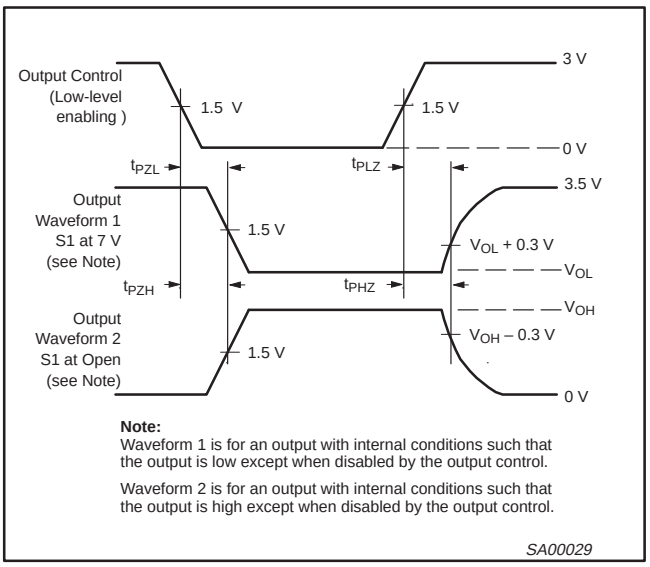
NOTE:
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5 V, V_{IN} = GND to 3.0 V



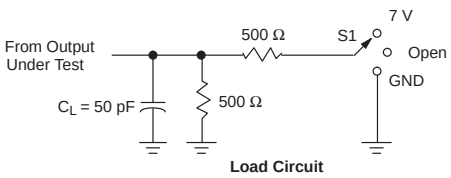
Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

NOTES:
1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. t_{PLH} and t_{PHL} are the same as t_{pd}.

TEST CIRCUIT AND WAVEFORMS



Load Circuit

TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
2. The outputs are measured one at a time with one transition per measurement.

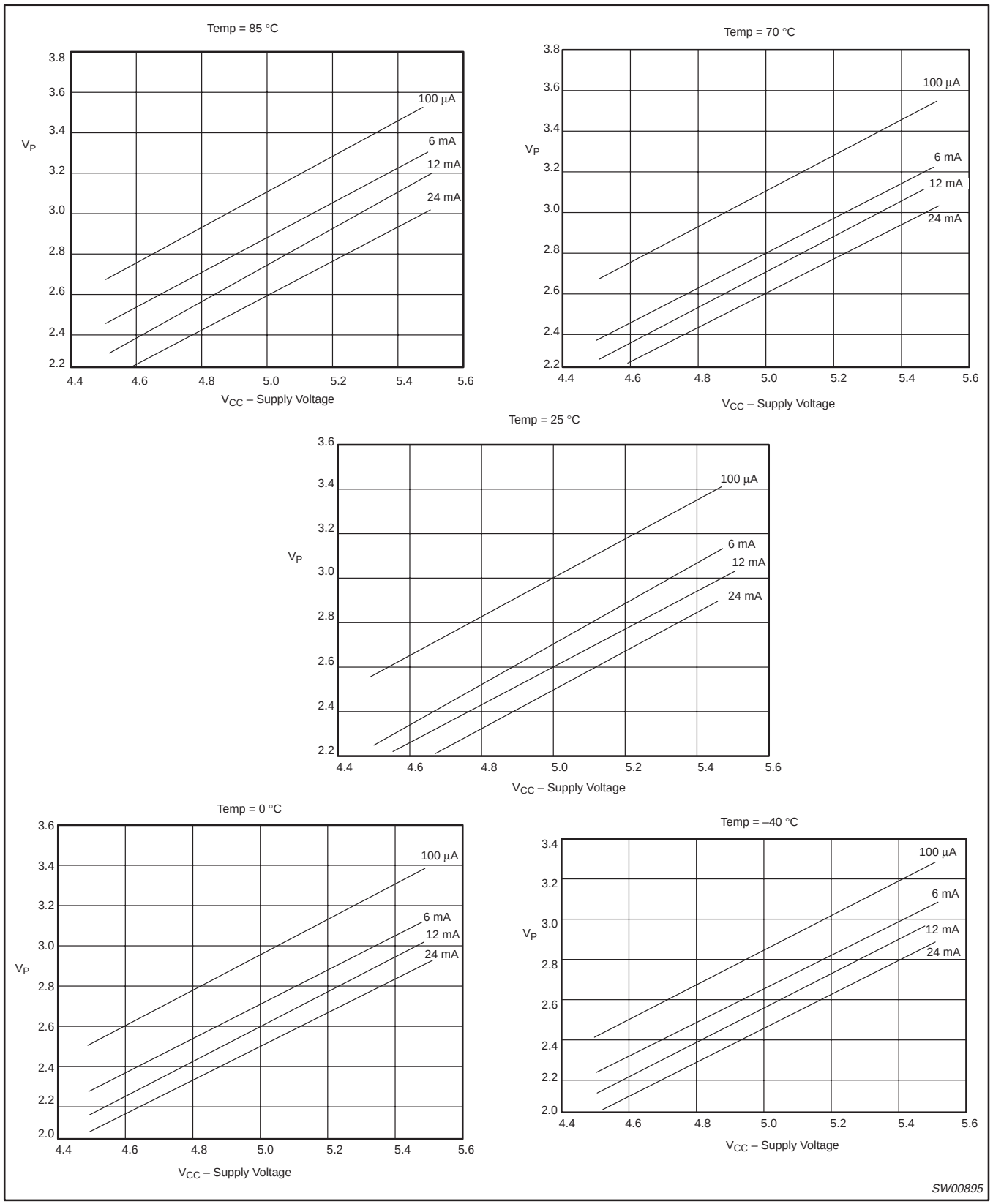
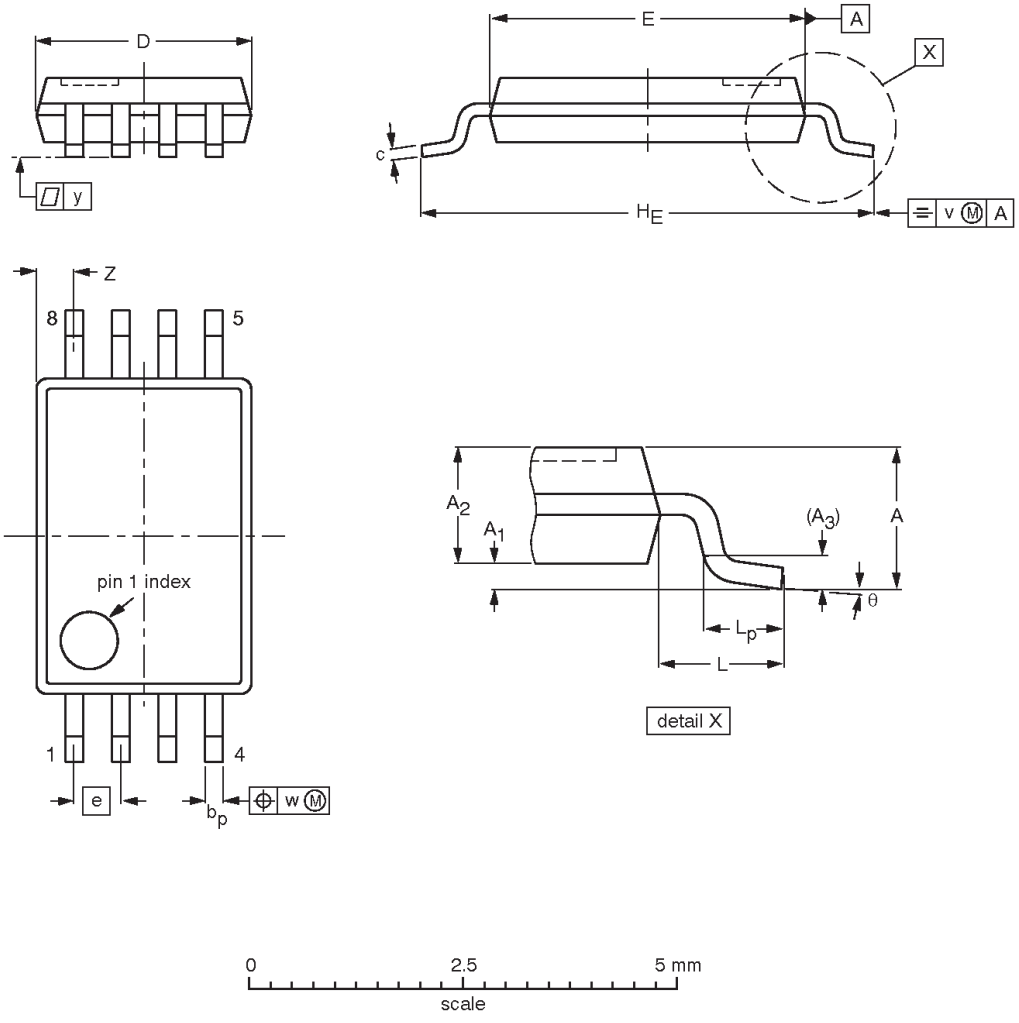


Figure 1. Pass voltage values ($V_{in} = V_{CC}$)

TSSOP8: plastic thin shrink small outline; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

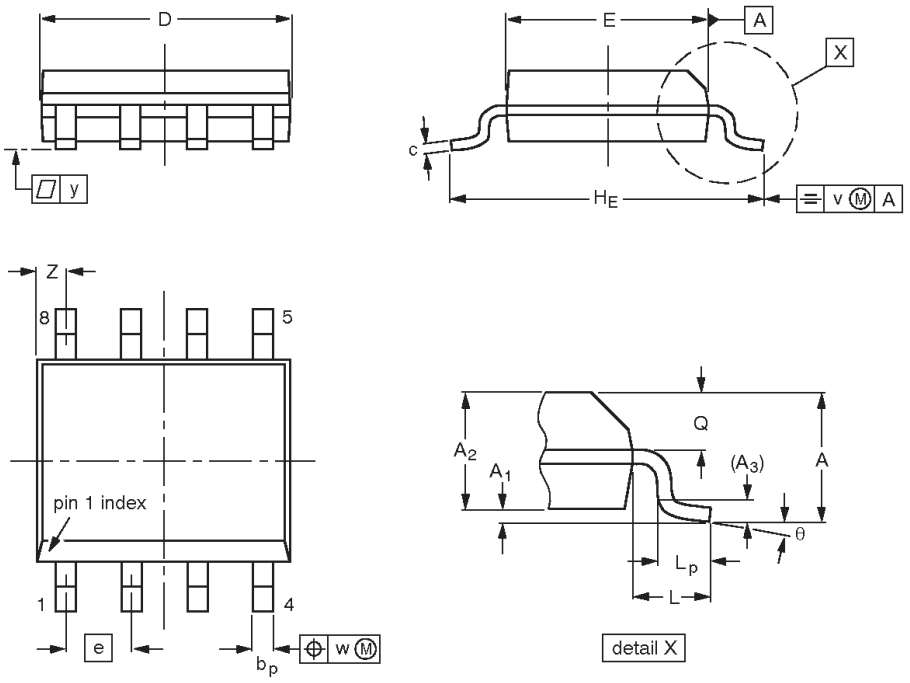
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.10 2.90	4.50 4.30	0.65	6.50 6.30	0.94	0.70 0.50	0.10	0.10	0.10	0.70 0.35	8° 0°

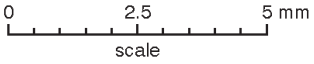
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT530-1		MO-153				~~99-12-27~~ 00-02-24

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

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2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

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Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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