

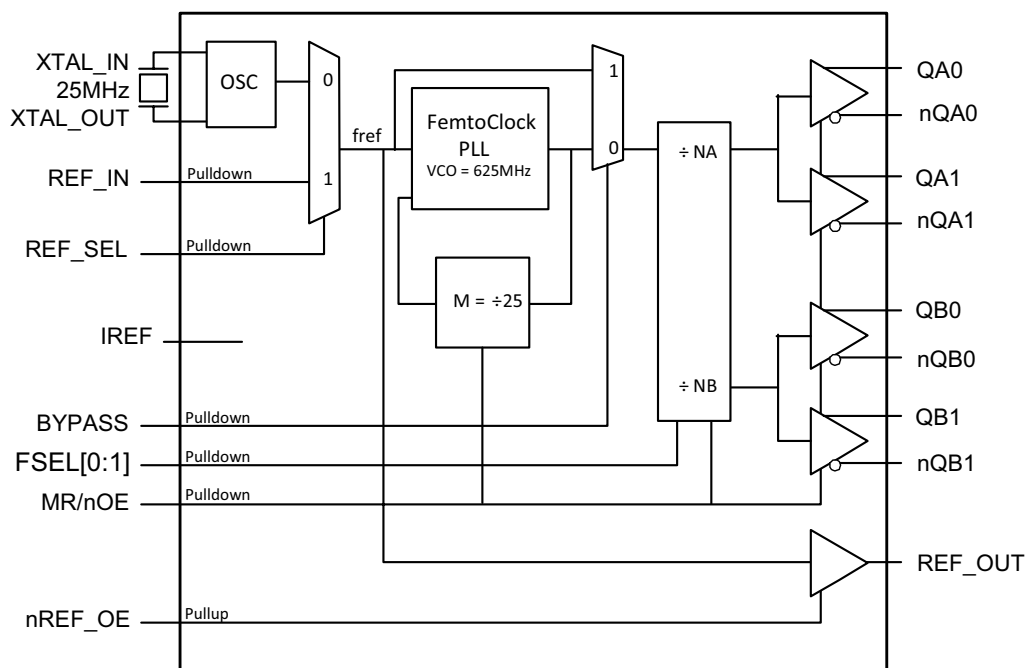
General Description

The ICS841664I is an optimized sRIO clock generator and a member of the family of high-performance clock solutions from IDT. The device uses a 25MHz parallel crystal to generate 125MHz and 156.25MHz clock signals, replacing solution requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter (<1ps RMS) suitable to clock components requiring precise and low-jitter sRIO clock signals. Designed for telecom, networking and industrial application, the ICS841664I can also drive the high-speed sRIO SerDes clock inputs of communication processors, DSPs, switches and bridges.

Features

- Four differential HCSL clock outputs: configurable for sRIO (125MHz or 156.25MHz) clock signals
One REF_OUT LVCMOS/LVTTL clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input or LVCMOS/LVTTL single-ended input
- Supports the following output frequencies: 125MHz or 156.25MHz
- VCO: 625MHz
- Supports PLL bypass and output enable functions
- RMS phase jitter, using a 25MHz crystal (1.875MHz - 20MHz): 0.45ps (typical) @ 125MHz
- Full 3.3V power supply mode
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment

| | | | |
|---------|----|----|----------|
| VDD | 1 | 28 | IREF |
| REF_OUT | 2 | 27 | FSEL0 |
| GND | 3 | 26 | FSEL1 |
| QA0 | 4 | 25 | QB0 |
| nQA0 | 5 | 24 | nQB0 |
| VDDOA | 6 | 23 | VDDOB |
| GND | 7 | 22 | GND |
| QA1 | 8 | 21 | QB1 |
| nQA1 | 9 | 20 | nQB1 |
| nREF_OE | 10 | 19 | MR/nOE |
| BYPASS | 11 | 18 | VDD |
| REF_IN | 12 | 17 | XTAL_IN |
| REF_SEL | 13 | 16 | XTAL_OUT |
| VDDA | 14 | 15 | GND |

ICS841664I
28-Lead TSSOP
6.1mm x 9.7mm x 0.925mm
package body
G Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------------|------------------------|--------|----------|--|
| 1, 18 | V _{DD} | Power | | Core supply pins. |
| 2 | REF_OUT | Output | | LVC MOS/LVTTL reference frequency clock output. |
| 3, 7, 15, 22 | GND | Power | | Power supply ground. |
| 4, 5, 8, 9 | QA0, nQA0 QA1, nQA1 | Output | | Differential Bank A output pairs. HCSL interface levels. |
| 6 | V _{DDOA} | Power | | Output supply pin for Bank A outputs. |
| 10 | nREF_OE | Input | Pullup | Active low REF_OUT enable/disable. See Table 3E. LVC MOS/LVTTL interface levels. |
| 11 | BYPASS | Input | Pulldown | Selects PLL/PLL bypass mode. See Table 3C. LVC MOS/LVTTL interface levels. |
| 12 | REF_IN | Input | Pulldown | LVC MOS/LVTTL reference clock input. |
| 13 | REF_SEL | Input | Pulldown | Reference select, Selects the input reference source. See Table 3B. LVC MOS/LVTTL interface levels |
| 14 | V _{DDA} | Power | | Analog supply pin. |
| 16, 17 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 19 | MR/nOE | Input | Pulldown | Active HIGH master reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance. When logic LOW, the internal dividers and the outputs are enabled. See Table 3D. LVC MOS/LVTTL interface levels. |
| 20, 21, 24, 25 | nQB1, QB1 nQB0, QB0 | Output | | Differential Bank B output pairs. HCSL interface levels. |
| 23 | V _{DDOB} | Power | | Output supply pin for Bank B outputs. |
| 26, 27 | FSEL1, FSEL0 | Input | Pulldown | Output frequency select pins. LVC MOS/LVTTL interface levels. |
| 28 | IREF | Output | | HCSL current reference resistor output. A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QX[0:1], nQX[0:1] clock outputs. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------------|--------------------------|--------------------------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 4 | | pF |
| C _{PD} | Power Dissipation Capacitance | V _{DD} = 3.465V | | 4 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{OUT} | Output Impedance | REF_OUT | V _{DD} = 3.465V | 20 | | Ω |

Function Tables

Table 3A. NA, NB FSELx Function Table ($f_{ref} = 25\text{MHz}$)

| Inputs | | | Outputs Frequency Settings | |
|--------|-------|----|----------------------------|-----------------------|
| FSEL1 | FSEL0 | M | QA[0:1], nQA[0:1] | QB[0:1], nQB[0:1] |
| 0 | 0 | 25 | VCO/5 (125MHz) | VCO/5 (125MHz) |
| 0 | 1 | 25 | VCO/5 (125MHz) | VCO/4 (156.25MHz) |
| 1 | 0 | 25 | VCO/5 (125MHz) | QB0:1 = L, nQB0:1 = H |
| 1 | 1 | 25 | VCO/4 (156.25MHz) | VCO/4 (156.25MHz) |

Table 3B. REF_SEL Function Table

| Input | |
|---------|-----------------|
| REF_SEL | Input Reference |
| 0 | XTAL |
| 1 | REF_IN |

Table 3C. BYPASS Function Table

| Input | |
|--------|---|
| BYPASS | PLL Configuration ^{NOTE 1} |
| 0 | PLL enabled |
| 1 | PLL bypassed (QA, QB = f_{ref}/N_x , $x = A$ or B) |

NOTE 1: Asynchronous control.

Table 3D. MR/nOE Function Table

| Input | |
|--------|--|
| MR/nOE | Function ^{NOTE 1} |
| 0 | Outputs enabled |
| 1 | Internal dividers reset, outputs disabled (High impedance) |

NOTE 1: Asynchronous control.

Table 3E. nREF_OE Function Table

| Input | |
|---------|-----------------------------------|
| nREF_OE | Function ^{NOTE 1} |
| 0 | REF_OUT enabled |
| 1 | REF_OUT disabled (high impedance) |

NOTE 1: Asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|--|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I XTAL_IN Other Inputs | 0V to V_{DD} -0.5V to $V_{DD} + 0.5V$ |
| Outputs, I_O Continuous Current REF_OUT Surge Current REF_OUT | $\pm 15mA$ $\pm 30mA$ |
| Package Thermal Impedance, θ_{JA} | 64.5°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------------------|-----------------------|--|-----------------|---------|---------|-------|
| V_{DD} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{DDA} | Analog Supply Voltage | | $V_{DD} - 0.20$ | 3.3 | 3.465 | V |
| V_{DDOA} , V_{DDOB} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | No Load | | | 80 | mA |
| I_{DDA} | Analog Supply Current | No Load | | | 20 | mA |
| I_{DDOA} , I_{DDOB} | Output Supply Current | No Load, $R_{REF} = 475\Omega \pm 1\%$ | | | 5 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------------------|---|--------------------------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL0, FSEL1 | $V_{DD} = V_{IN} = 3.465V$ | | 150 | μA |
| | | nREF_OE | $V_{DD} = V_{IN} = 3.465V$ | | 5 | μA |
| I_{IL} | Input Low Current | REF_IN, REF_SEL, BYPASS, MR/nOE, FSEL0, FSEL1 | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5 | | μA |
| | | nREF_OE | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | μA |
| V_{OH} | Output High Voltage; NOTE 1 | REF_OUT | $V_{DD} = 3.465V$ | 2.6 | | V |
| V_{OL} | Output Low Voltage; NOTE 1 | REF_OUT | $V_{DD} = 3.465V$ | | 0.5 | V |

NOTE 1: Outputs termination with 50Ω to $V_{DD}/2$. See Parameter Measurement Information Section, *Output Load Test Circuit diagram*.

Table 5. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

Table 6A. LVCMOS AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|----------------------------|-----------------|---------|---------|---------|-------|
| f_{OUT} | Output Frequency REF_OUT | | | 25 | | MHz |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 1.5 | | 2.2 | ns |
| odc | Output Duty Cycle | | 47 | | 53 | % |

Table 6B. HCSL AC Characteristics, $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------------|--|-------------------------|---|---------|---------|---------|-------|
| f_{OUT} | Output Frequency | | VCO/5 | | 125 | | MHz |
| | | | VCO/4 | | 156.25 | | MHz |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter (Random); NOTE 1 | | 125MHz, Integration Range: 1.875MHz - 20MHz | | 0.45 | 0.55 | ps |
| | | | 156.25MHz, Integration Range: 1.875MHz - 20MHz | | 0.41 | 0.54 | ps |
| $f_{jit}(cc)$ | Cycle-to-Cycle Jitter; NOTE 3 | | | | | 60 | ps |
| $t_{sk}(o)$ | Output Skew; NOTE 2, 3 | QAx, nQAx, QBx, nQBx | | | | 140 | ps |
| t_L | PLL Lock Time | | | | | 100 | ms |
| V_{HIGH} | Voltage High | | | 650 | 700 | 950 | mV |
| V_{LOW} | Voltage Low | | | -150 | | 150 | mV |
| V_{OVS} | Max. Voltage, Overshoot | | | | | 0.3 | V |
| V_{UDS} | Min. Voltage, Undershoot | | | -0.3 | | | V |
| V_{RB} | Ringback Voltage | | | | | 0.2 | V |
| V_{CROSS} | Absolute Crossing Voltage | | | 200 | | 550 | mV |
| ΔV_{CROSS} | Total Variation of V_{CROSS} over all edges | | | | | 160 | mV |
| t_R / t_F | Output Rise/Fall Time | QAx, nQAx, QBx, nQBx | measured between 0.175V to 0.525V | 100 | | 700 | ps |
| $\Delta t_R / \Delta t_F$ | Rise/Fall Time Variation | | | | | 125 | ps |
| odc | Output Duty Cycle | QAx, nQAx, QBx, nQBx | | 47 | | 53 | % |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

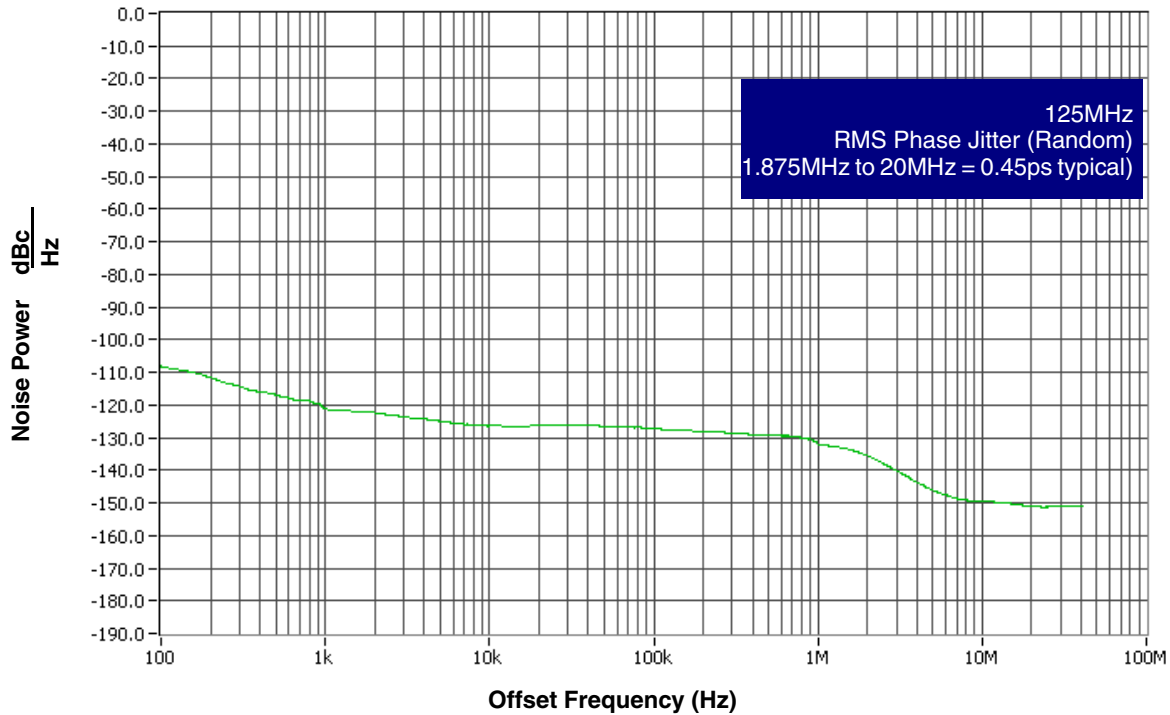
NOTE: All measurements are taken at 125MHz and 156.25MHz.

NOTE 1: Please refer to the Phase Noise Plot.

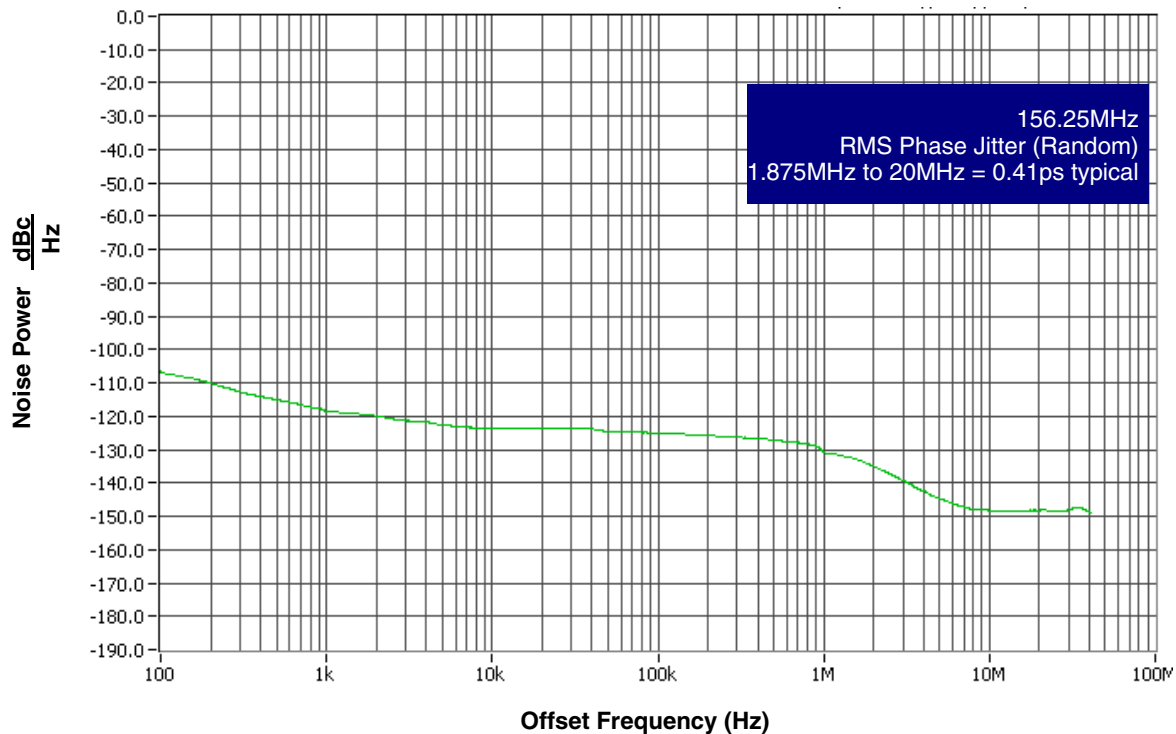
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

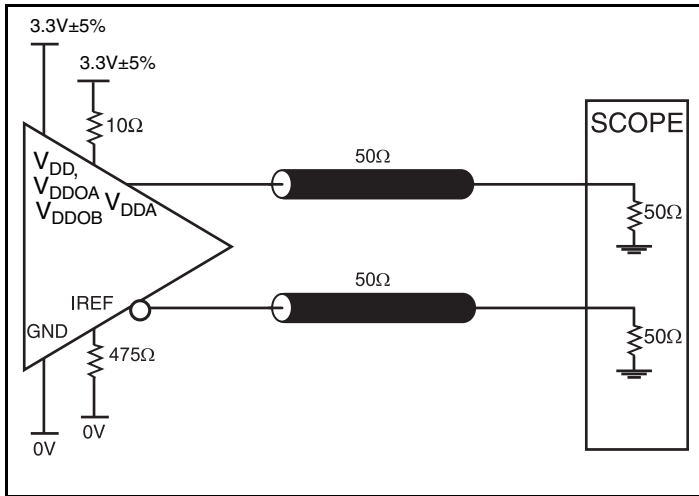
Typical Phase Noise at 125MHz At 3.3V



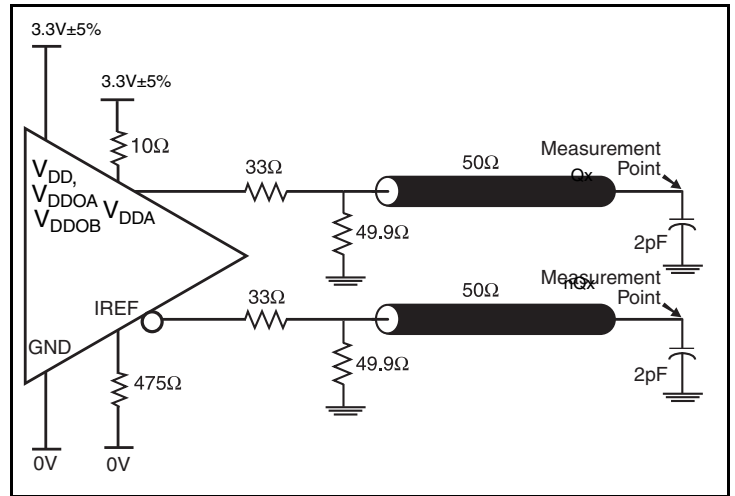
Typical Phase Noise at 156.25MHz At 3.3V



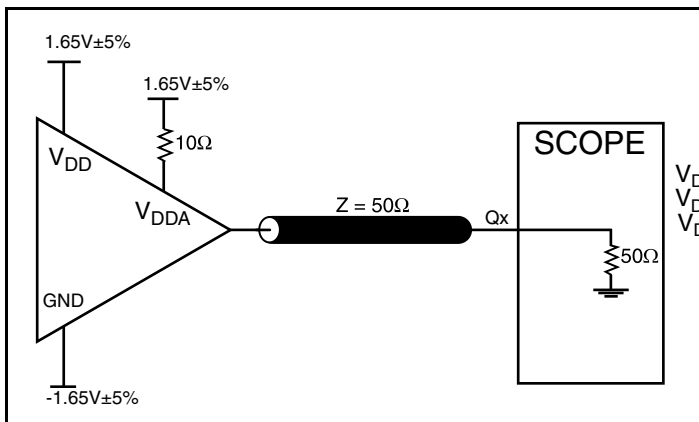
Parameter Measurement Information



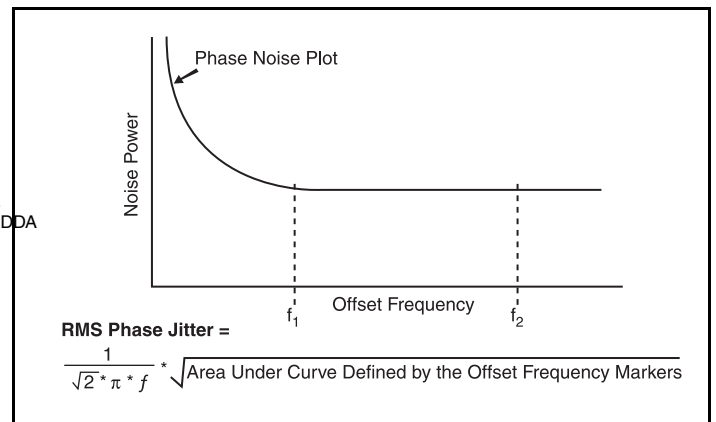
3.3V HCSL Output Load Test Circuit



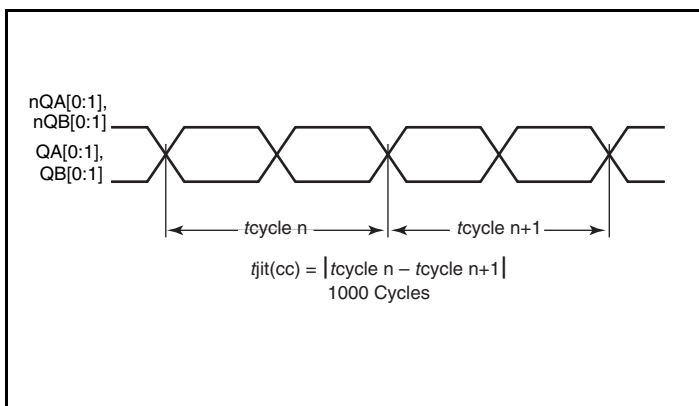
3.3V HCSL Output Load Test Circuit



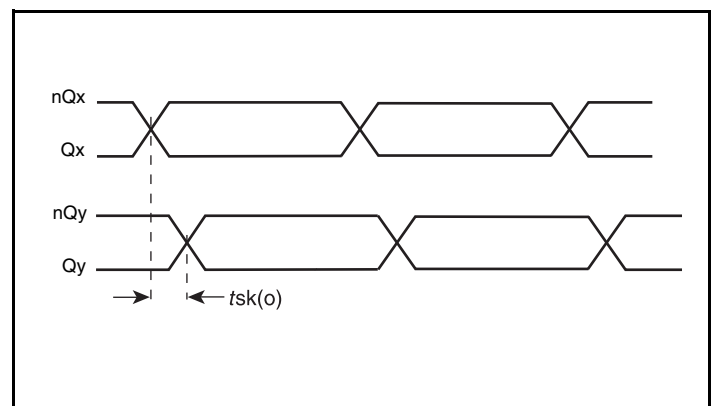
3.3V LVCMOS Output Load Test Circuit



RMS Phase Jitter

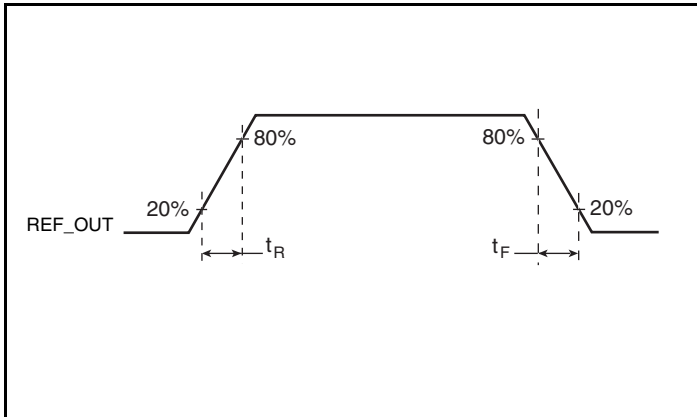


Cycle-to-Cycle Jitter

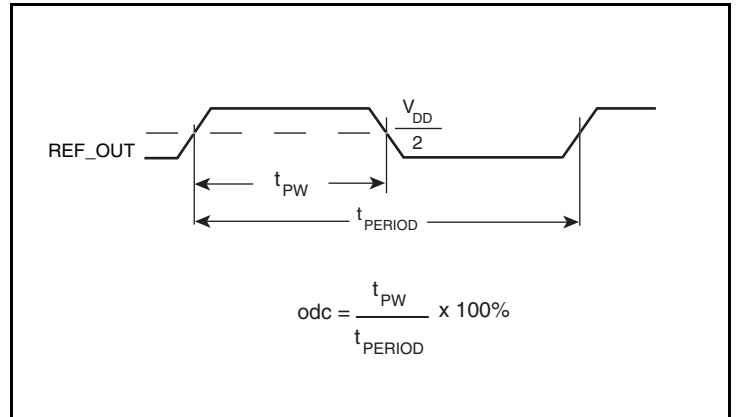


HCSL Output Skew

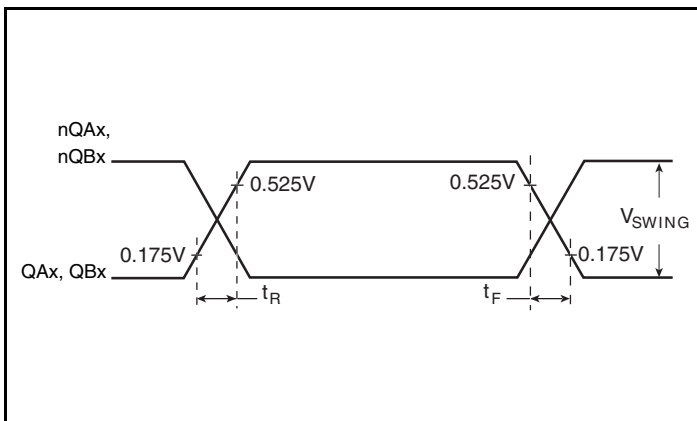
Parameter Measurement Information, continued



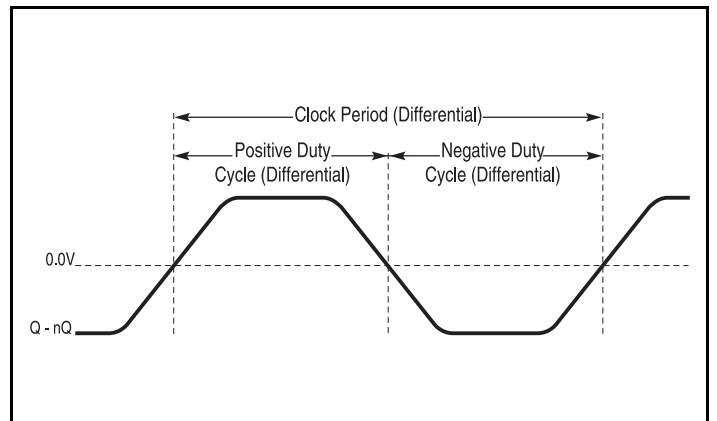
LVC MOS Output Rise/Fall Time



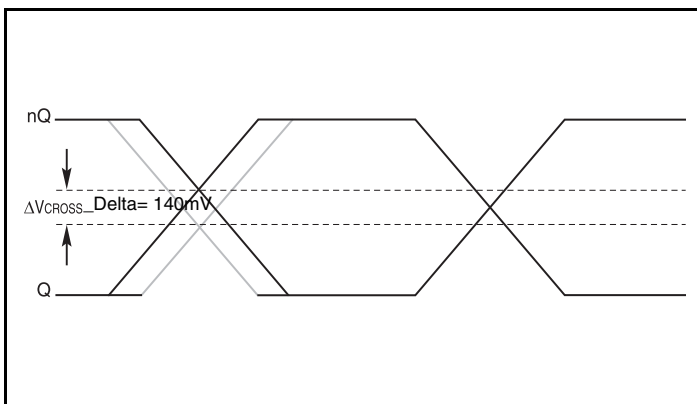
LVC MOS Output Duty Cycle/Pulse Width/Period



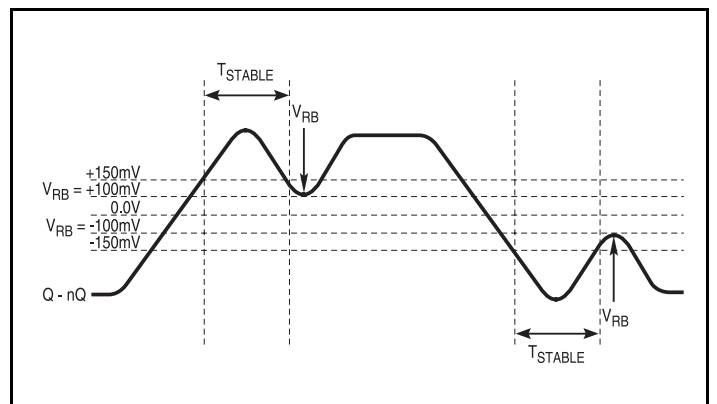
Differential Measurement Points For Rise/Fall Time



Differential Measurement Points For Duty Cycle/Period

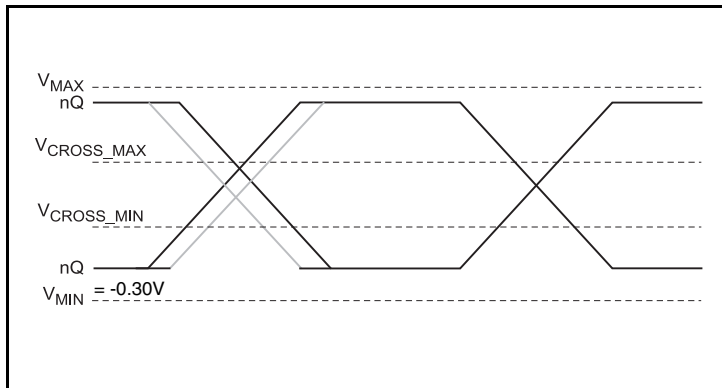


SE Measurement Points For Delta Cross Point



Differential Measurement Points For Ringback

Parameter Measurement Information, continued



SE Measurement Points For Absolute Cross Point/Swing

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1k\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1k\Omega$ resistor can be tied from the REF_CLK to ground.

LVC MOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A $1k\Omega$ resistor can be used.

Outputs:

HCSL Outputs

All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVC MOS Outputs

The unused LVC MOS output can be left floating. There should be no trace attached.

Schematic Layout

Figure 1 shows an example of ICS841664I application schematic. In this example, the device is operated at $V_{DD} = V_{DDA} = V_{DDOA} = V_{DDOB} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The load capacitance $C1 = 27pF$ and $C2 = 27pF$ are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require

adjusting $C1$ and $C2$. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS841664I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

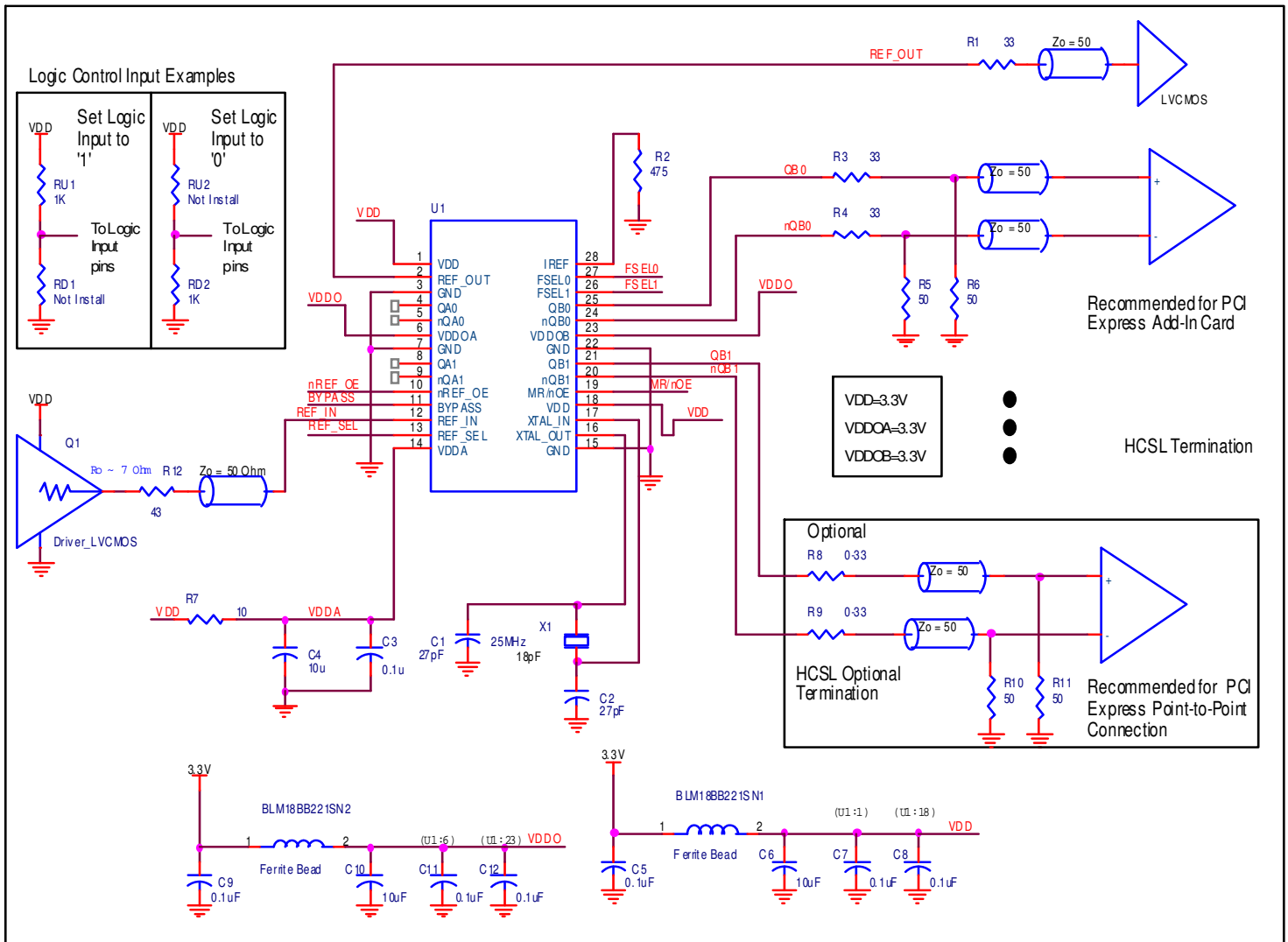


Figure 1. ICS841664I Schematic Example

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference

is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and changing R_2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

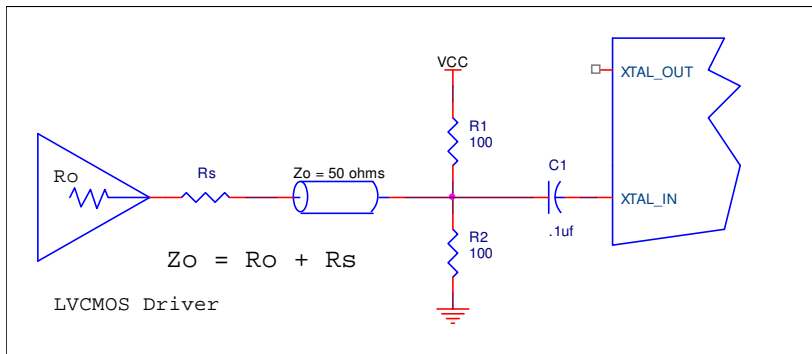


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

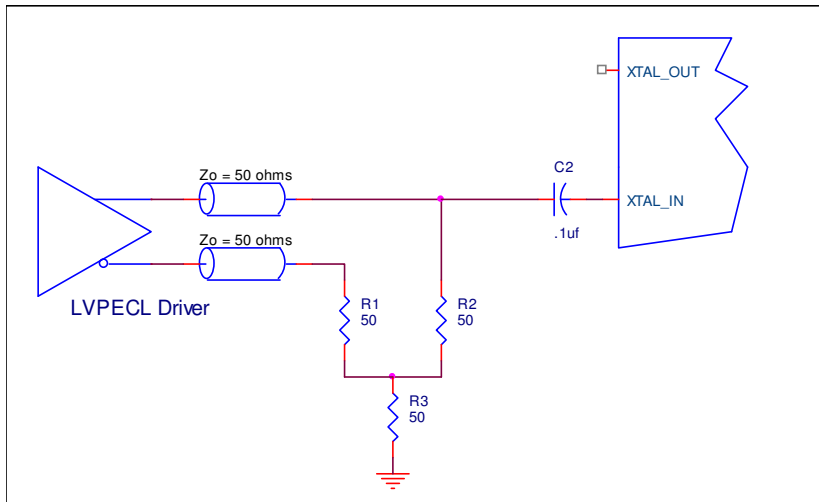


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

Applications Information, continued

Recommended Termination

Figure 3A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

All traces should be 50Ω impedance single-ended or 100Ω differential.

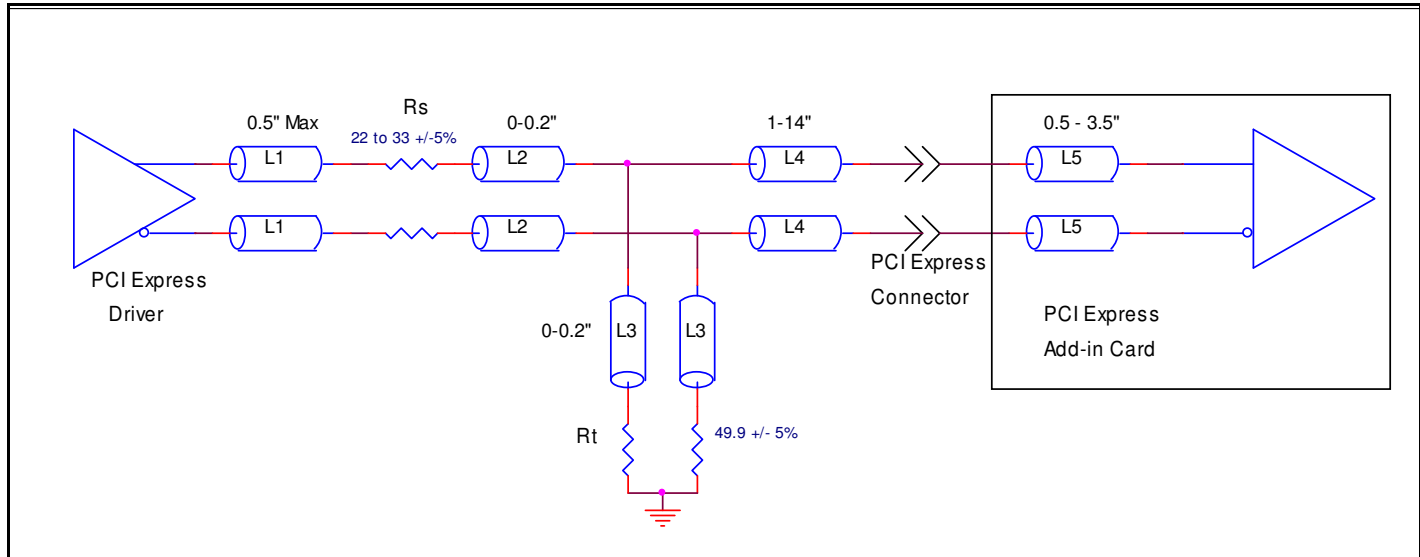


Figure 3A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 3B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (R_s) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

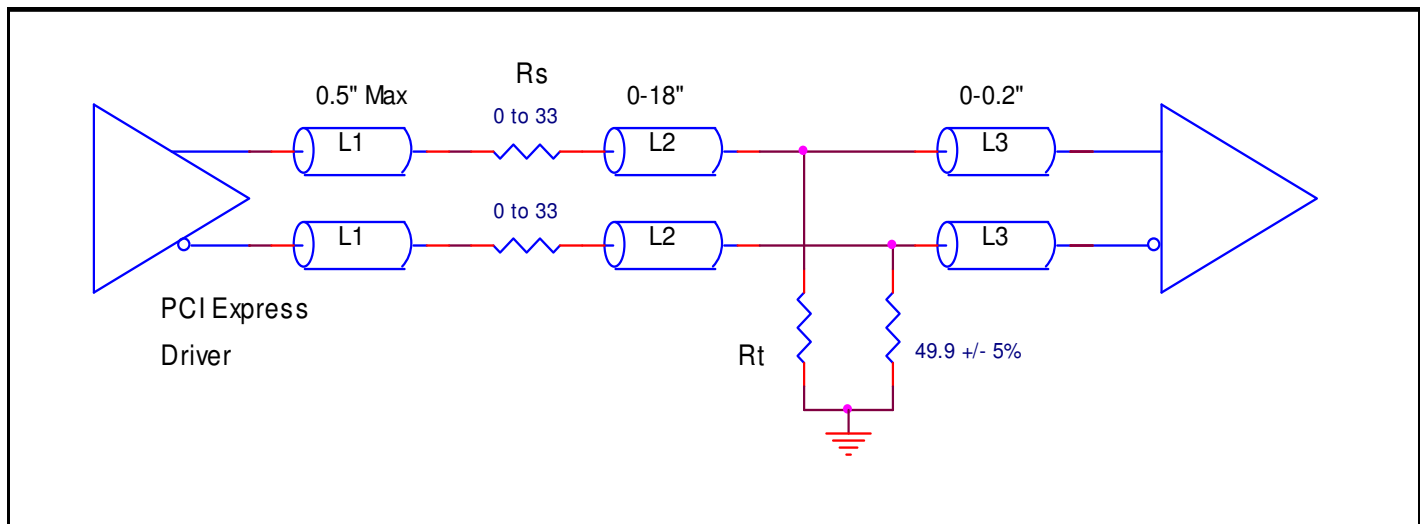


Figure 3B. Recommended Termination (where a point-to-point connection can be used)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS841664I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS841664I is the total power minus the analog power plus the power dissipated into the load. The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

Core and HCSL Output Power Dissipation

- Power (core)_{MAX} = $V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (80mA + 20mA) = \mathbf{346.5mW}$
- Power (outputs)_{MAX} = **44.5mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 44.5mW = \mathbf{178mW}$

LVC MOS Driver Power Dissipation

- Dynamic Power Dissipation at 25MHz
Power (25MHz) = $C_{PD} * \text{Frequency} * (V_{DD})^2 = 4pF * 25MHz * (3.465V)^2 = \mathbf{1.20mW \text{ per output}}$

Total Power Dissipation

- Total Power**
= Power (core) + Power (Outputs) + Total Power (25MHz)
= $346.5mW + 178mW + 1.2mW$
= **525.7mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 64.5°C/W per Table 7 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.526W * 64.3^\circ\text{C/W} = 118.9^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28 Lead TSSOP, Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.5°C/W | 60.4°C/W | 58.5°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 4*.

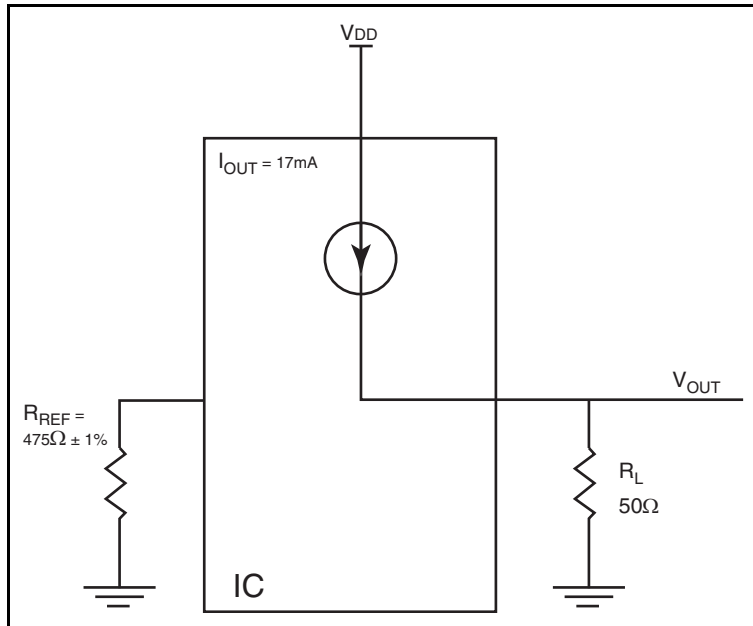


Figure 4. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX} .

$$\text{Power} = (V_{DD_MAX} - V_{OUT}) * I_{OUT}$$

$$\text{since } V_{OUT} = I_{OUT} * R_L$$

$$\text{Power} = (V_{DD_MAX} - I_{OUT} * R_L) * I_{OUT}$$

$$= (3.465V - 17mA * 50\Omega) * 17mA$$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 28 Lead TSSOP

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 64.5°C/W | 60.4°C/W | 58.5°C/W |

Transistor Count

The transistor count for ICS841664I is: 2954

Package Outline and Package Dimensions

Package Outline - G Suffix for 28 Lead TSSOP

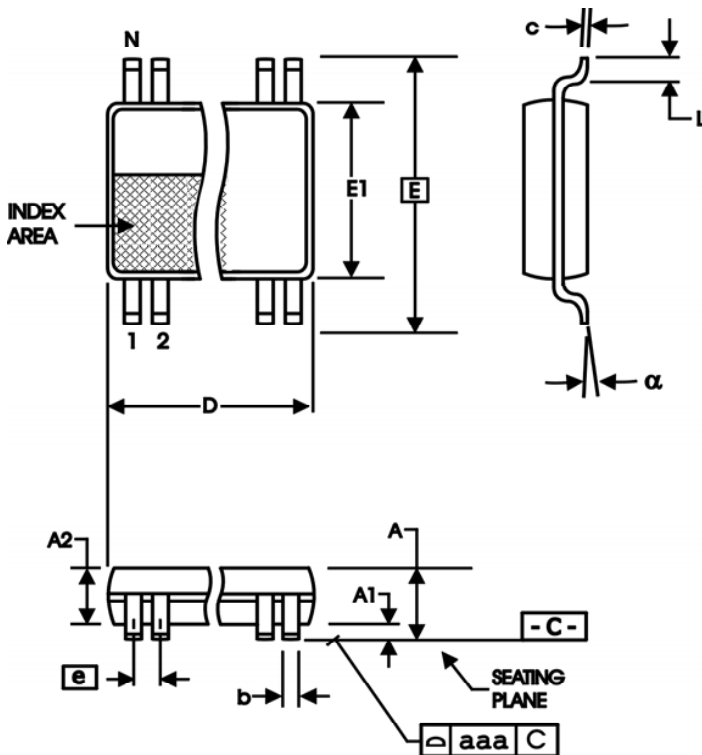


Table 9. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 28 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 9.60 | 9.80 |
| E | 8.10 Basic | |
| E1 | 6.00 | 6.20 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|--------------------------|----------------|---------------------------|---------------------------|--------------------|
| 841664AGILF | ICS841664AGI | 28 Lead "Lead-Free" TSSOP | Tube | -40°C to 85°C |
| 841664AGILFT | ICS841664AGI | 28 Lead "Lead-Free" TSSOP | Tape & Reel | -40°C to 85°C |

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-----------|---------|--|---------|
| A | T1 T10 | 2 18 | Pin Description Table - switched pin names for pins 20 through 25. Ordering Information Table - deleted Tape & Reel quantity. | 7/15/13 |
| | | | | |

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