

DESCRIPTION

This is a family of 262144-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

This device has $\overline{1}\text{CAS}$ and $2\overline{W}$ terminals. Refresh cycle is 1024 cycles every 16.4 ms.

FEATURES

Type name	$\overline{\text{RAS}}$ access time (max. ns)	$\overline{\text{CAS}}$ access time (max. ns)	Address access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mw)
M5M44170AXX-6,-6S	60	15	30	120	580
M5M44170AXX-7,-7S	70	20	35	140	500
M5M44170AXX-8,-8S	80	20	40	160	440
M5M44170AXX-10,-10S	100	25	50	190	375

XX=J,L,TP,RT

- 40 pin 400 mil SOJ
- 40 pin 475 mil ZIP
- 44 pin 400 mil TSOP
- Single $5\text{V} \pm 10\%$ supply
- Low stand-by power dissipation
- 5.5 mW (Max.). CMOS Input level
- 0.55 mW^* (Max.). CMOS Input level
- Low operating power dissipation
- M5M44170AXX-6,-6S. . . 770 mW (Max.)
- M5M44170AXX-7,-7S. . . 660 mW (Max.)
- M5M44170AXX-8,-8S. . . 578 mW (Max.)
- M5M44170AXX-10,-10S. . . 495 mW (Max.)
- Fast-page mode (256-bit random access), Read -modify-write, $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh capabilities.
- Self refresh capability
- Self refresh current..200us
- Extended refresh capability
- Extended refresh current..250us
- Early write mode and LW/UW and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A0 — A9)
- 1024 refresh cycles every 128 ms (A0 — A9)*

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

*:Applicable to self refresh version(M5M44170AJ,L,TP,RT-6S,-7S,-8S,-10S:option)only.

PIN CONFIGURATION (TOP VIEW)

VCC	1	40	VSS
DQ 1	2	39	DQ 16
DQ 2	3	38	DQ 15
DQ 3	4	37	DQ 14
DQ 4	5	36	DQ 13
VCC	6	35	VSS
DQ 5	7	34	DQ 12
DQ 6	8	33	DQ 11
DQ 7	9	32	DQ 10
DQ 8	10	31	DQ 9
NC.	11	30	NC.
$\overline{\text{LW}}$	12	29	$\overline{\text{NC}}$
$\overline{\text{UW}}$	13	28	$\overline{\text{CAS}}$
RAS	14	27	OE
A9	15	26	A8
A0	16	25	A7
A1	17	24	A6
A2	18	23	A5
A3	19	22	A4
VCC	20	21	VSS

(M5M44170AJ)

PIN CONFIGURATION (TOP VIEW)

VCC	1	44	VSS
DQ 1	2	43	DQ 16
DQ 2	3	42	DQ 15
DQ 3	4	41	DQ 14
DQ 4	5	40	DQ 13
VCC	6	39	VSS
DQ 5	7	38	DQ 12
DQ 6	8	37	DQ 11
DQ 7	9	36	DQ 10
DQ 8	10	35	DQ 9
NL.	11	34	NL.
NL.	12	33	NL.
$\overline{\text{NC}}$	13	32	$\overline{\text{NC}}$
$\overline{\text{LWE}}$	14	31	$\overline{\text{NC}}$
$\overline{\text{UWE}}$	15	30	$\overline{\text{CAS}}$
RAS	16	29	OE
A9	17	28	A8
A0	18	27	A7
A1	19	26	A6
A2	20	25	A5
A3	21	24	A4
VCC	22	23	VSS

(M5M44170ATP)

NL=NO LEAD

PIN CONFIGURATION (TOP VIEW)

VSS	1	44	VCC
DQ 16	2	43	DQ 1
DQ 15	3	42	DQ 2
DQ 14	4	41	DQ 3
DQ 13	5	40	DQ 4
VSS	6	39	VCC
DQ 12	7	38	DQ 5
DQ 11	8	37	DQ 6
DQ 10	9	36	DQ 7
DQ 9	10	35	DQ 8
NL.	11	34	NL.
NL.	12	33	NL.
NC.	13	32	NC.
NC.	14	31	LWE
CAS	15	30	UWE
OE	16	29	RAS
A8	17	28	A9
A7	18	27	A0
A6	19	26	A1
A5	20	25	A2
A4	21	24	A3
VSS	22	23	VCC

(M5M44170ART)

NL=NO LEAD

PIN CONFIGURATION (TOP VIEW)

DQ9	1	2	DQ 10
DQ 11	3	4	DQ 12
VSS	5	6	DQ 13
DQ 14	7	8	DQ 15
DQ 16	9	10	VSS
VCC	11	12	DQ 1
DQ2	13	14	DQ 3
DQ4	15	16	VCC
DQ5	17	18	DQ 6
DQ7	19	20	DQ 8
NC.	21	22	LW
UW	23	24	RAS
A9	25	26	A0
A1	27	28	A2
A3	29	30	VCC
VSS	31	32	A4
A5	33	34	A6
A7	35	36	A8
OE	37	38	CAS
NC.	39	40	NC.

(M5M44170AL)

FUNCTION

The M5M44170AJ, TP,RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input condition for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{LW}}$	$\overline{\text{UW}}$	$\overline{\text{OE}}$	DQ1 - DQ8	DQ9 - DQ16		
Read	ACT	ACT	NAC	NAC	ACT	DOUT	DOUT	YES	Fast page mode identical
Lower byte write	ACT	ACT	ACT	NAC	NAC	DIN	DNC	YES	
Upper byte write	ACT	ACT	NAC	ACT	NAC	DNC	DIN	YES	
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	DNC	OPN	OPN	YES	
Hidden refresh	ACT	ACT	NAC	NAC	ACT	DOUT	DOUT	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ (Extended*) refresh	ACT	ACT	DNC	DNC	DNC	OPN	OPN	YES	
Self refresh *	ACT	ACT	DNC	DNC	DNC	OPN	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN	NO	

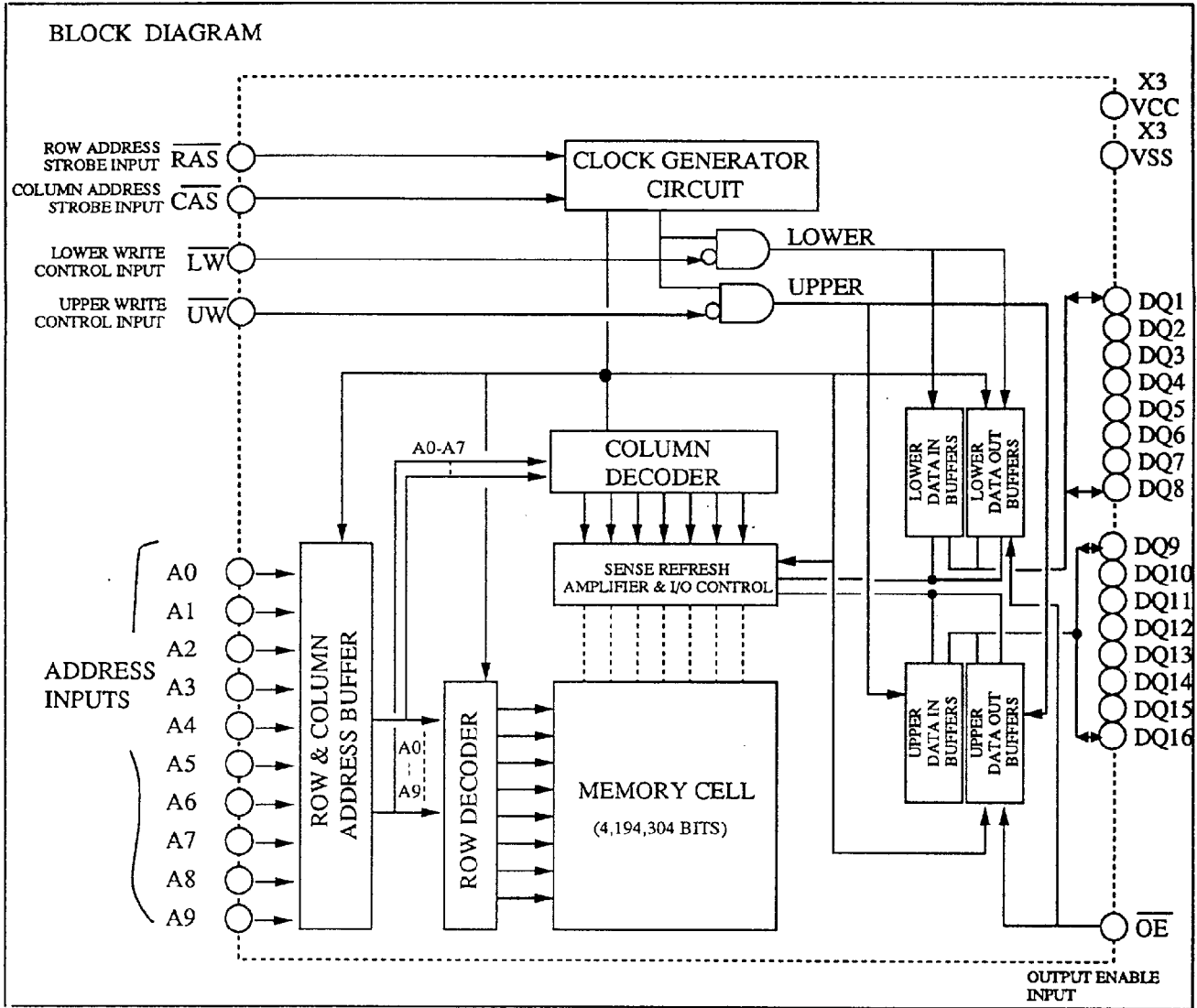
Note ACT:active, NAC:nonactive, DNC:don't care, OPN:open



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	-1~7	V
V _i	Input voltage		-1~7	V
V _o	Output voltage		-1~7	V
I _o	Output current		50	mA
P _d	Power dissipation	T _a = 25 °C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	4.5	5	5.5	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.5	V
V _{IL}	Low-level input voltage	DQ1 ~ DQ16	-1.0	0.8	V
		Others	-2.0	0.8	V

Note 1: All voltage values are with respect to V_{ss}.

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70 °C, V_{cc} = 5V ± 10%, V_{ss} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V ≤ V _{out} ≤ 5.5V	-10		10	μA
I _i	Input current	0 ≤ V _{IH} ≤ 6.5V, Other inputs pins = 0V	-10		10	μA
I _{CC1}	Average supply current from V _{cc} operating (Note 3, 4, 5)	M5M44170A-6,-6S	RAS, CAS cycling t _{RC} = t _{WC} = min. output open		140	mA
		M5M44170A-7,-7S			120	
		M5M44170A-8,-8S			105	
		M5M44170A-10,-10S			90	
I _{CC2}	Supply current from V _{cc} , stand-by (Note 6)	RAS = CAS = V _{IH} , output open			2	mA
		RAS = CAS ≥ V _{CC} -0.5 output open			1	
					0.1*	
I _{CC3}	Average supply current from V _{cc} refreshing (Note 3, 5)	M5M44170A-6,-6S	RAS cycling CAS = V _{IH} , t _{RC} = min. output open		140	mA
		M5M44170A-7,-7S			120	
		M5M44170A-8,-8S			105	
		M5M44170A-10,-10S			90	
I _{CC4}	Average supply current from V _{cc} Fast-Page-Mode (Note 3, 4, 5)	M5M44170A-6,-6S	RAS = V _{IL} CAS cycling t _{PC} = min., output open		140	mA
		M5M44170A-7,-7S			120	
		M5M44170A-8,-8S			105	
		M5M44170A-10,-10S			90	
I _{CC6}	Average supply current from V _{cc} CAS before RAS refresh mode (Note 3, 5)	M5M44170A-6,-6S	CAS before RAS refresh cycling, t _{RC} = min. output open		120	mA
		M5M44170A-7,-7S			105	
		M5M44170A-8,-8S			90	
		M5M44170A-10,-10S			80	

ELECTRICAL CHARACTERISTICS (continued) ($T_a = 0 \sim 70\text{ }^{\circ}\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ICC 8 *	Average supply current from VCC Extended refresh mode (Note 6)	RAS cycling $\overline{\text{CAS}} \leq 0.2\text{V}$ or $\overline{\text{CAS}}$ before RAS refresh cycling $\overline{\text{OE}} \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$ $\overline{\text{WE}} \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$ $A_0 \sim A_9 \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$ DQ = open $t_{RC} = 125\text{ }\mu\text{s}$ $t_{RAS} = t_{RAS\text{ min}} - 1\text{ }\mu\text{s}$			250	μA
ICC 9 *	Average supply current from VCC Self refresh mode (Note 6)	$\overline{\text{RAS}} = \overline{\text{CAS}} \leq 0.2\text{V}$ $\overline{\text{OE}} \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$ $\overline{\text{WE}} \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$ $A_0 \sim A_9 \leq 0.2\text{V}$ or $\geq V_{cc} - 0.2\text{V}$			200	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{cc1(AV)}$, $I_{cc3(AV)}$ and $I_{cc4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: $I_{cc1(AV)}$ and $I_{cc4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$ and $\overline{\text{CAS}} = \text{VIH}$.

CAPACITANCE ($T_a = 0 \sim 70\text{ }^{\circ}\text{C}$, $V_{cc} = 5\text{V} \pm 10\%$, $V_{ss} = 0\text{V}$, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
C I (A)	Input capacitance, address inputs	M5M44170AJ,TP,RT	$V_I = V_{SS}$ $f = 1\text{ MHz}$ $V_i = 2.5\text{ mV rms}$			5	pF
		M5M44170AL				7	pF
C I (CLK)	Input capacitance, clock inputs	M5M44170AJ,TP,RT				7	pF
		M5M44170AL				9	pF
C I/O	Input/Output capacitance, data ports	M5M44170AJ,TP,RT				7	pF
		M5M44170AL				9	pF



SWITCHING CHARACTERISTICS (Ta = 0 ~ 70 °C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 5, 12, 13)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCAC	Access time from CAS (Note 7, 8)		15		20		20		25	ns
tRAC	Access time from RAS (Note 7, 9)		60		70		80		100	ns
tAA	Column Address access time (Note 7, 10)		30		35		40		50	ns
tCPA	Access time from CAS precharge (Note 7, 11)		35		40		45		55	ns
tOEA	Access time from OE (Note 7)		15		20		20		25	ns
tCLZ	Output low impedance from CAS low (Note 7)	5		5		5		5		ns
tOFF	Output disable time after CAS high (Note 12)	0	15	0	20	0	20	0	25	ns
tOEZ	Output disable time after OE high (Note 12)	0	15	0	20	0	20	0	25	ns

Note 6: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -Only refresh).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to 2TTL loads and 100pF.

8: Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

9: Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.

10: Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ and $t_{\text{ASC}} \leq t_{\text{ASC}}(\text{max})$.

11: Assumes that $t_{\text{CP}} \leq t_{\text{CP}}(\text{max})$ and $t_{\text{ASC}} \geq t_{\text{ASC}}(\text{max})$.

12: $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ defines the time at which the output achieves the high impedance state ($I_{\text{out}} \leq |\pm 10 \mu\text{A}|$) and is not reference to $\text{VOH}(\text{min})$ or $\text{VOL}(\text{max})$.

TARGET SPEC.

Preliminary

M5M44170AJ,TP,RT-6,-6S,-7,-7S,-8,-8S,-10,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(Ta = 0 ~ 70 °C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 12, 13)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4		16.4	ms
tREF	Refresh cycle time*		128		128		128		128	ms
tRP	RAS high pulse width	50		60		70		80		ns
tRCD	Delay time, RAS low to CAS low (Note 15)	20	45	20	50	20	60	25	75	ns
tCRP	Delay time, CAS high to RAS low	10		10		10		10		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		0		ns
tCPN	CAS high pulse width	10		10		10		10		ns
tRAD	Column address delay time from RAS low (Note 16)	15	30	15	35	15	40	20	50	ns
tASR	Row address setup time before RAS low	0		0		0		0		ns
tASC	Column address setup time before CAS low (Note 17)	0	10	0	10	0	15	0	20	ns
tRAH	Row address hold time after RAS low	10		10		10		15		ns
tCAH	Column address hold time after CAS low	15		15		15		20		ns
tDZC	Delay time, data to CAS low (Note 18)	0		0		0		0		ns
tDZO	Delay time, data to OE low (Note 18)	0		0		0		0		ns
tCDD	Delay time, CAS high to data (Note 19)	15		20		20		25		ns
tODD	Delay time, OE high to data (Note 19)	15		20		20		25		ns
tT	Transition time (Note 20)	1	50	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT = 5ns.

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC.

If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

tRCD(min) is specified as tRCD(min) = tRAH(min) + 2tT + tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.

17: tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.

18: Either tDZC or tDZO must be satisfied.

19: Either tCDD or tODD must be satisfied.

20: tT is measured between VIH(min) and VIL(max).



rev. B

Read and Refresh Cycles

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	120		140		160		190		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	60	10000	70	10000	80	10000	100	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	15	10000	20	10000	20	10000	25	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	60		70		80		100		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	15		20		20		25		ns
tRCS	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		0		ns
tRCH	Read hold time after $\overline{\text{CAS}}$ high (Note 21)	0		0		0		0		ns
tRRH	Read hold time after $\overline{\text{RAS}}$ high (Note 21)	10		10		10		10		ns
tRAL	Column address to $\overline{\text{RAS}}$ hold time	30		35		40		50		ns
tOCH	$\overline{\text{CAS}}$ hold time after $\overline{\text{OE}}$ low	15		20		20		25		ns
tORH	$\overline{\text{RAS}}$ hold time after $\overline{\text{OE}}$ low	15		20		20		25		ns

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	120		140		160		190		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	60	10000	70	10000	80	10000	100	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	15	10000	20	10000	20	10000	25	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	60		70		80		100		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	15		20		20		25		ns
tWCS	Write setup time before $\overline{\text{CAS}}$ low (Note 23)	0		0		0		0		ns
tWCH	Write hold time after $\overline{\text{CAS}}$ low	10		15		15		20		ns
tCWL	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		25		ns
tRWL	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		25		ns
tWP	Write pulse width	10		15		15		20		ns
tDS	Data setup time before $\overline{\text{CAS}}$ low or W low	0		0		0		0		ns
tDH	Data hold time after CAS low or W low	10		15		15		20		ns
tOEh	OE hold time after W low	15		20		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWC	Read Write/read modify write cycle time (Note 22)	160		185		205		245		ns
tRAS	$\overline{\text{RAS}}$ low pulse width	95	10000	115	10000	125	10000	155	10000	ns
tCAS	$\overline{\text{CAS}}$ low pulse width	50	10000	65	10000	65	10000	80	10000	ns
tCSH	$\overline{\text{CAS}}$ hold time after $\overline{\text{RAS}}$ low	95		115		125		155		ns
tRSH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ low	50		65		65		80		ns
tRCS	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		0		ns
tCWD	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note 23)	35		40		40		50		ns
tRWD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{W}}$ low (Note 23)	80		90		100		125		ns
tAWD	Delay time, address to $\overline{\text{W}}$ low (Note 23)	50		55		60		75		ns
tCWL	$\overline{\text{CAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		25		ns
tRWL	$\overline{\text{RAS}}$ hold time after $\overline{\text{W}}$ low	15		20		20		25		ns
tWP	Write pulse width	10		15		15		20		ns
tDS	Data setup time before $\overline{\text{W}}$ low	0		0		0		0		ns
tDH	Data hold time after $\overline{\text{W}}$ low	10		15		15		20		ns
tOEh	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	15		15		20		25		ns

Note 22: tRWC is specified as $tRWC(\min) = tRAC(\max) + tODD(\min) + tRWL(\min) + tRP(\min) + 4tT$.

23: tWCS, tCWD, tRWD and tAWD and tCPWD are specified as reference points only. If $tWCS \geq tWCS(\min)$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $tCWD \geq tCWD(\min)$, $tRWD \geq tRWD(\min)$, $tAWD \geq tAWD(\min)$, and $tCPWD \geq tCPWD(\min)$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		50		60		ns
tPRWC	Fast page mode read write/read modify write cycle time	75		95		100		115		ns
tRAS	$\overline{\text{RAS}}$ low pulse width for read write cycle (Note 25)	100	100000	115	100000	135	100000	160	100000	ns
tCP	$\overline{\text{CAS}}$ high pulse width (Note 26)	10	15	10	15	10	20	10	25	ns
tCPRH	$\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$ precharge	35		40		45		55		ns
tCPWD	Delay time, $\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ low (Note 23)	35		40		45		55		ns



Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: tRAS(min) is specified as two cycles of $\overline{\text{CAS}}$ input are performed.

26: tCP(max) is specified as a reference point only.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle ,Extended Refresh* (Note 27)

Symbol	Parameter	Limits								Unit
		M5M44170A-6,-6S		M5M44170A-7,-7S		M5M44170A-8,-8S		M5M44170A-10,-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCSR	$\overline{\text{CAS}}$ setup time before RAS low	10		10		10		10		ns
tCHR	$\overline{\text{CAS}}$ hold time after RAS low	10		15		15		20		ns
tCAS	$\overline{\text{CAS}}$ low pulse width	25		30		30		35		ns

Note 27: Eight or more $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles instead of eight $\overline{\text{RAS}}$ cycles are necessary for proper operation of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle* (Note 28)

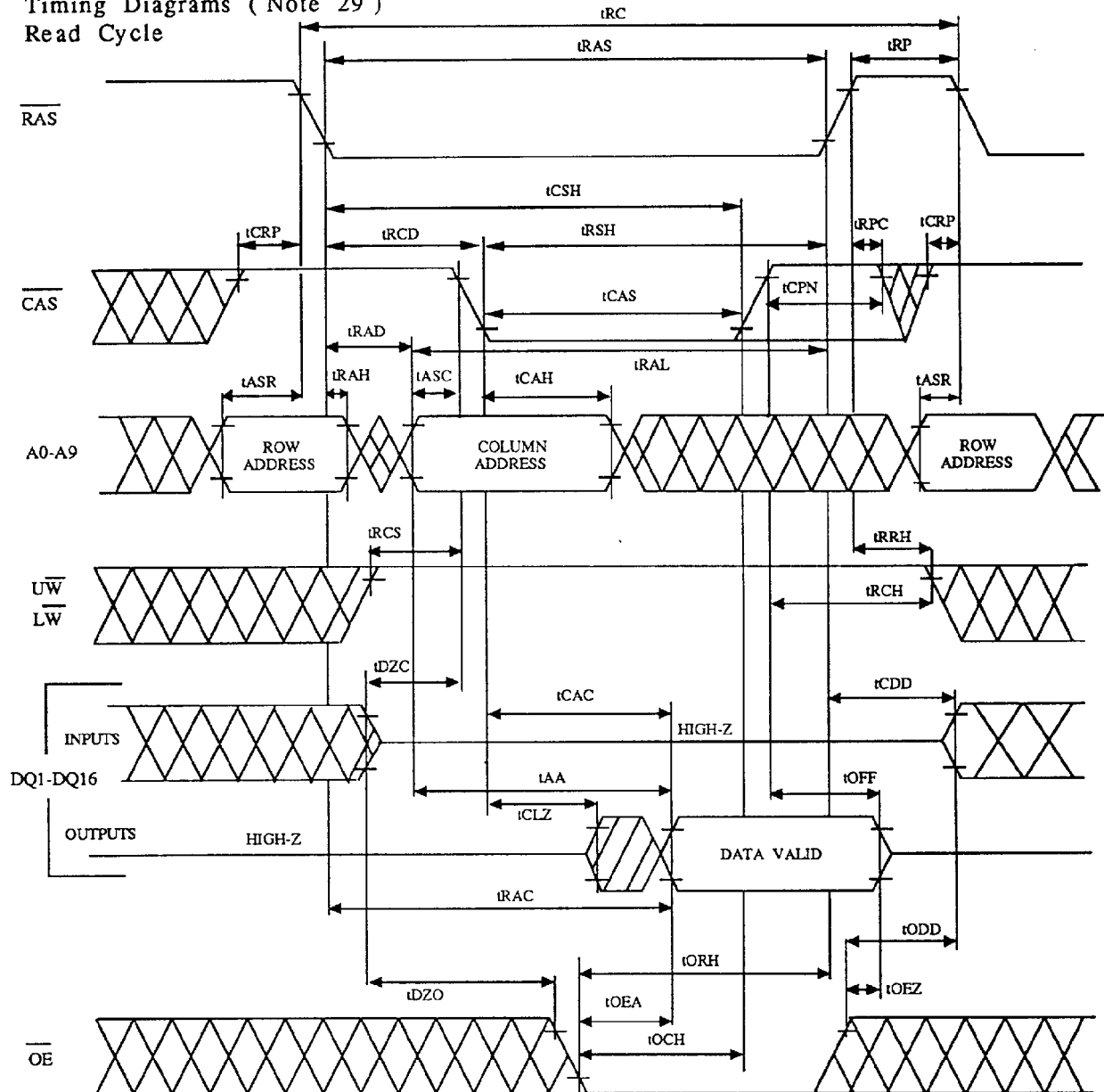
Symbol	Parameter	Limits								Unit
		M5M44170A-6S		M5M44170A-7S		M5M44170A-8S		M5M44170A-10S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh $\overline{\text{RAS}}$ low pulse width	100		100		100		100		μS
tRPS	CBR self refresh $\overline{\text{RAS}}$ high precharge time	120		140		160		190		ns
tCHS	CBR self refresh $\overline{\text{CAS}}$ hold time	-50		-50		-50		-50		ns



FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

Timing Diagrams (Note 29)

Read Cycle

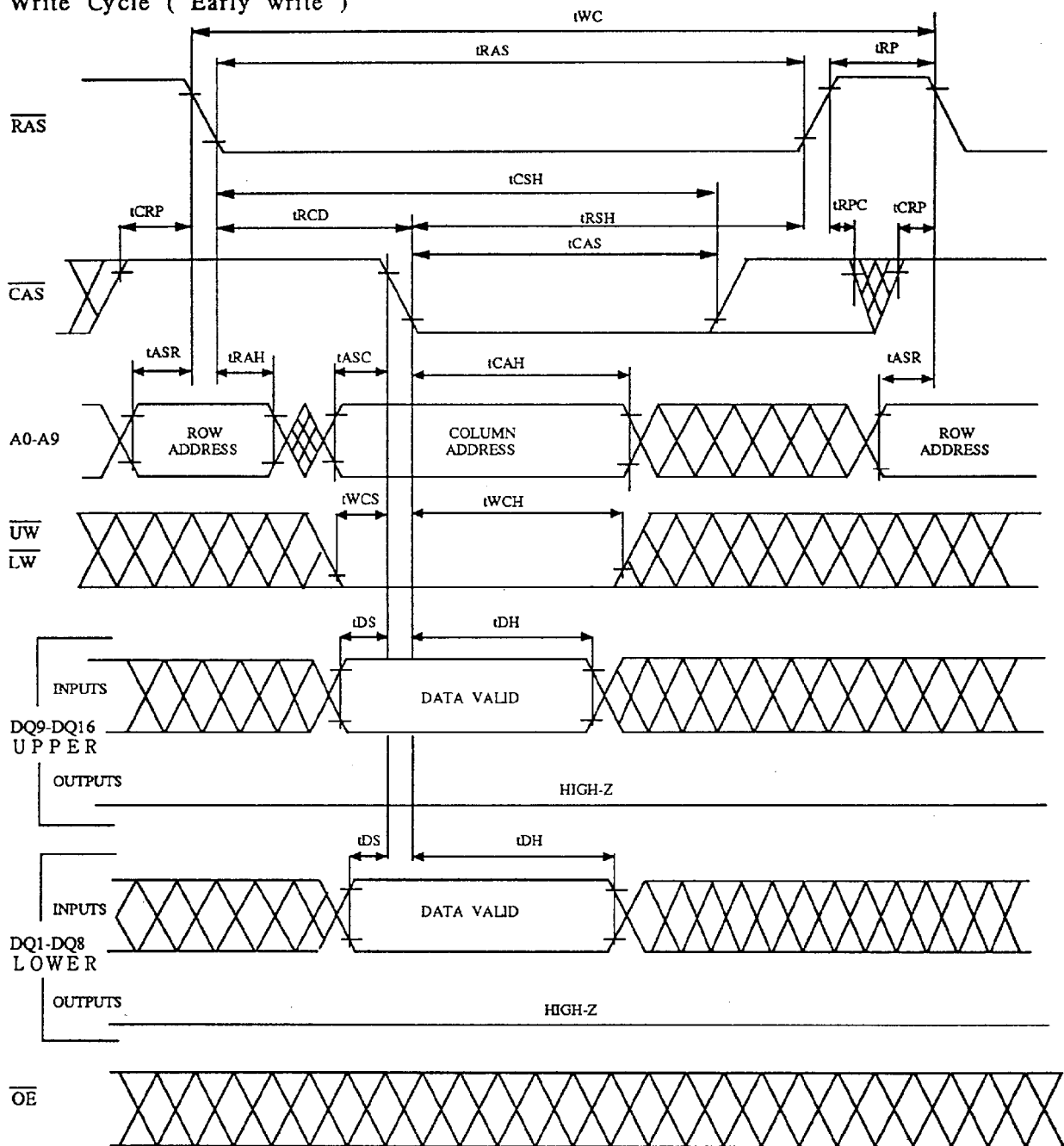


Note 29  Indicates the don't care input.
 $V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

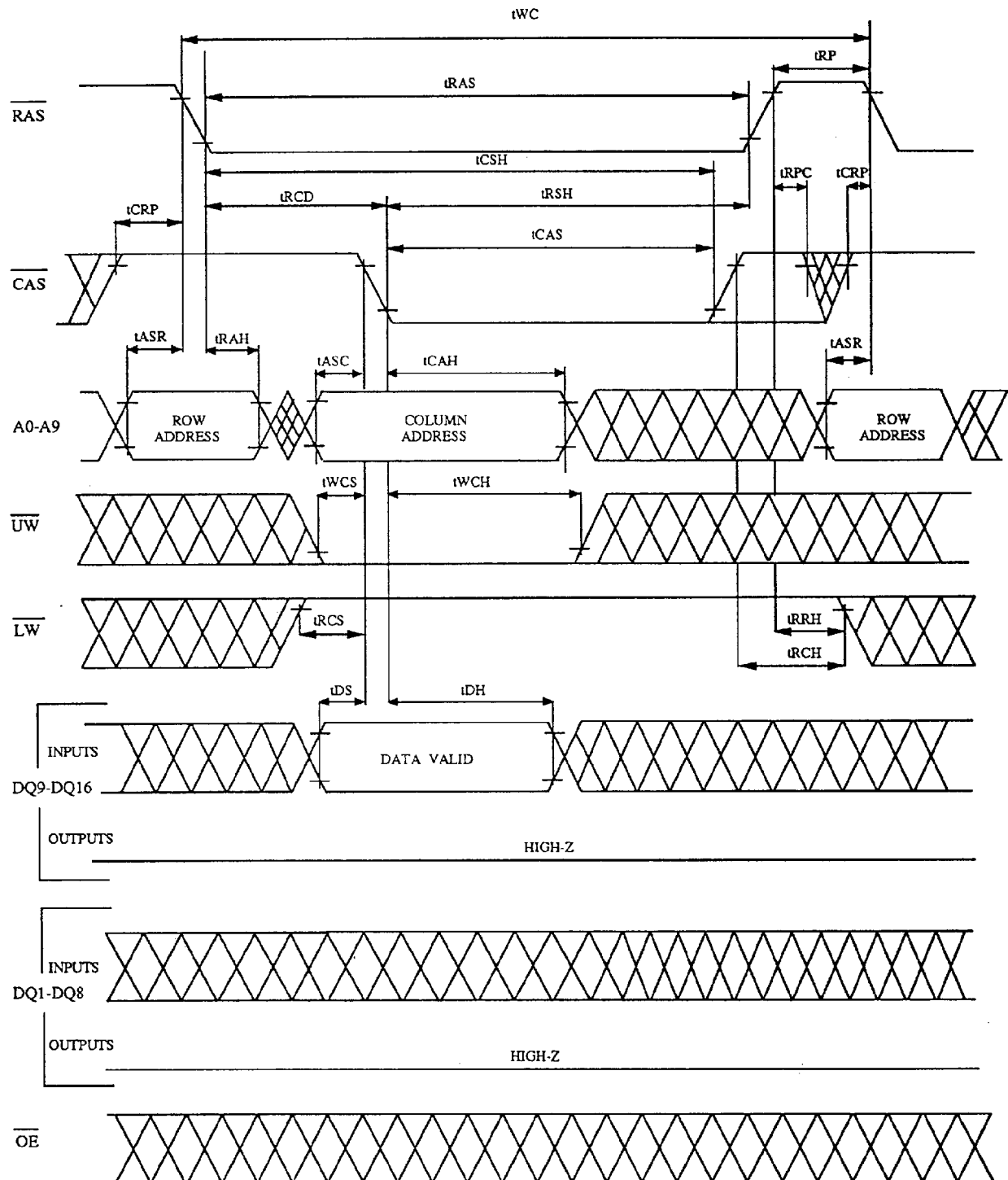
Indicates the invalid output.

Indicates the skew of the two inputs.

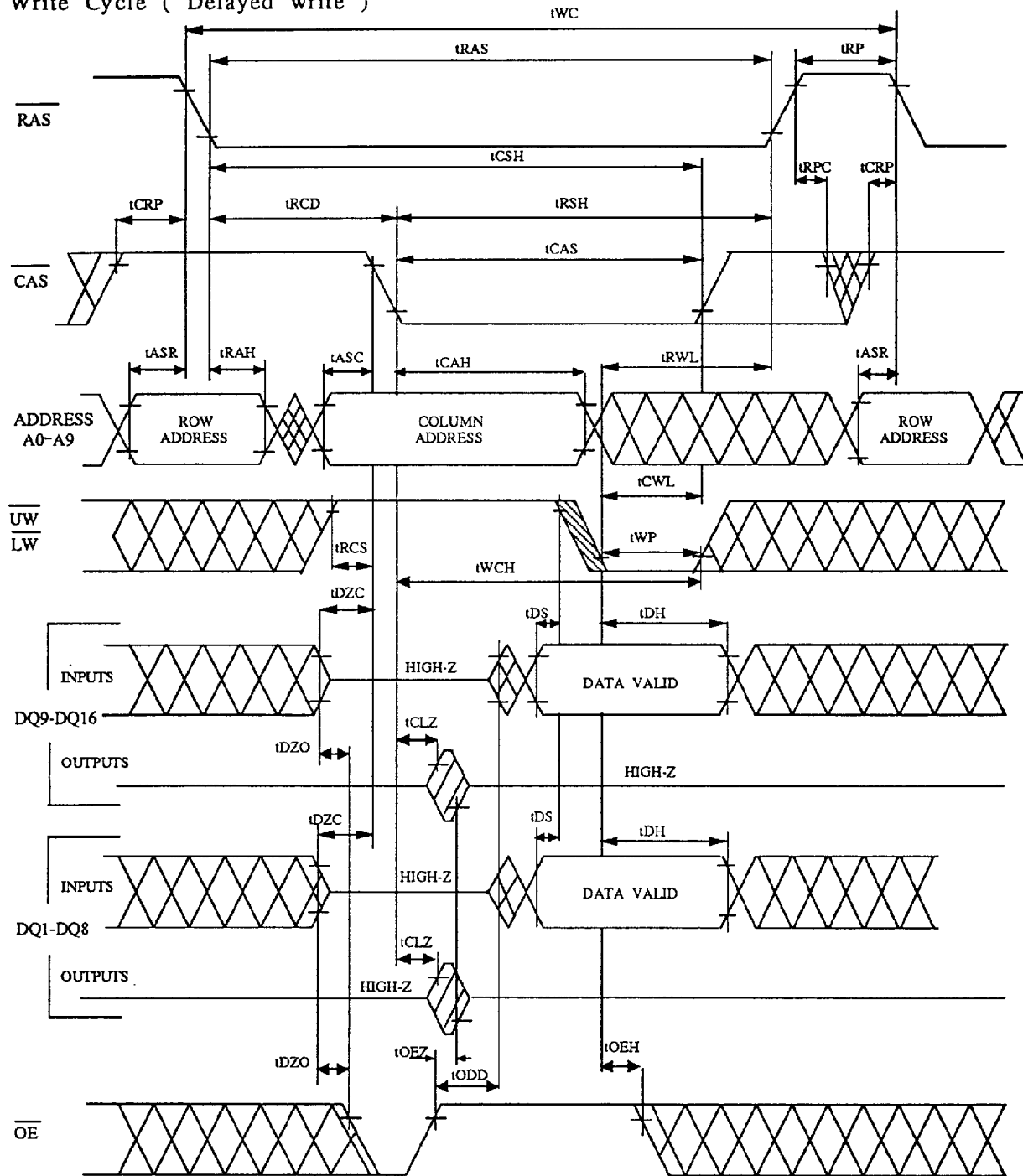
Write Cycle (Early write)



Upper/(Lower) Byte Write Cycle (Early write)



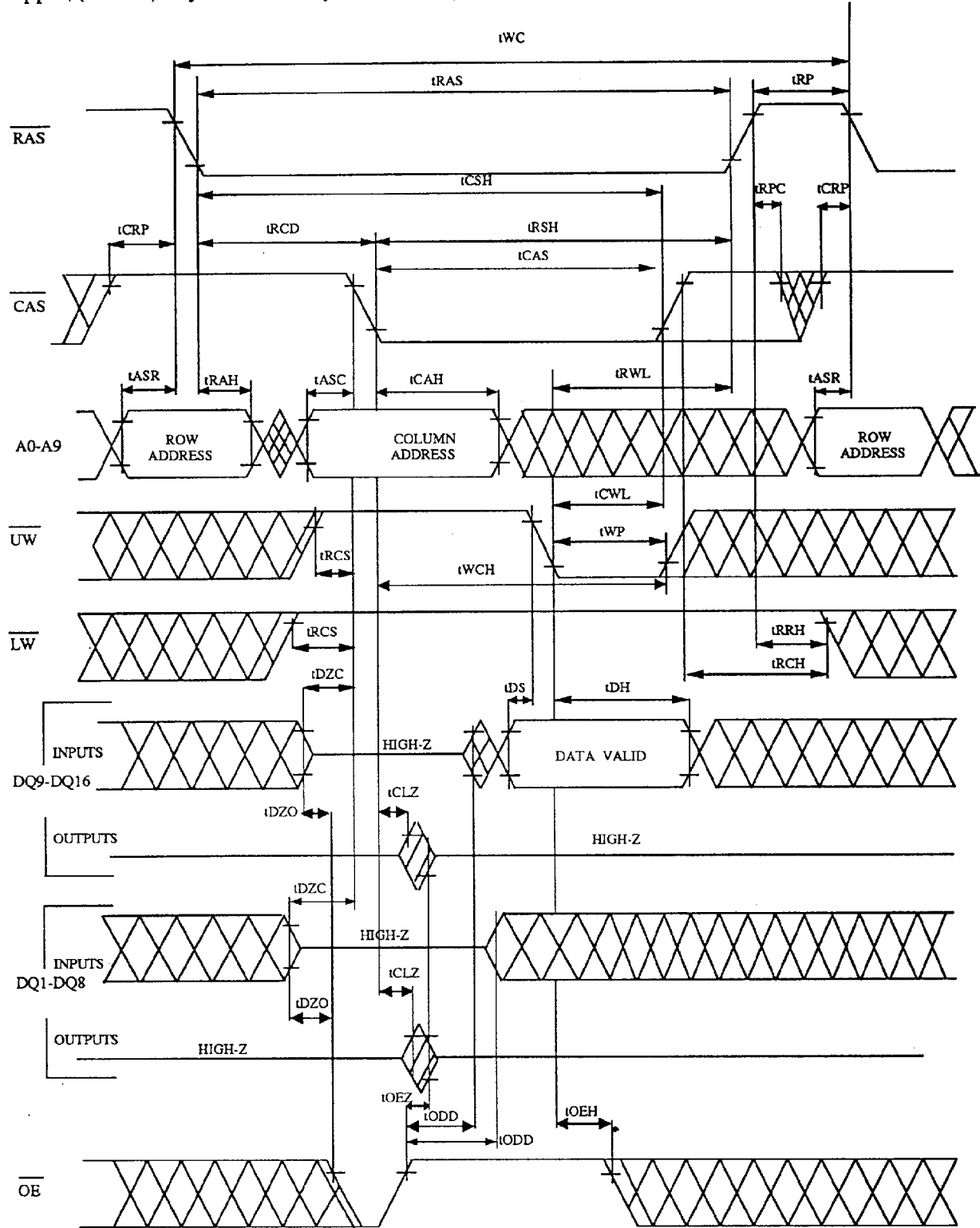
Write Cycle (Delayed write)



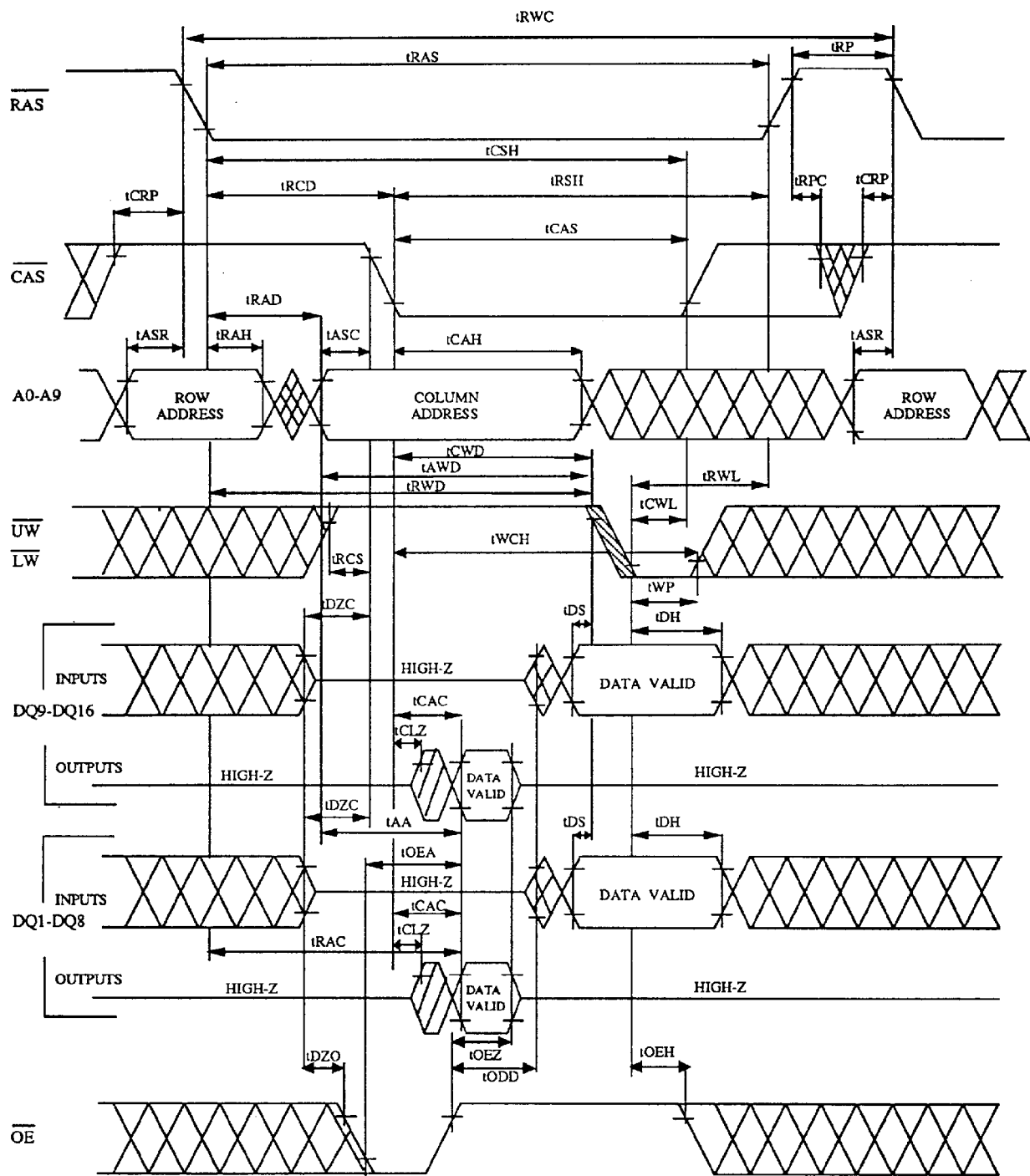
Preliminary

MITSUBISHI LSIs
M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S
FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

Upper/(Lower) Byte Write Cycle (Delayed write)



Read-Write, Read-Modify-Write Cycle



Preliminary

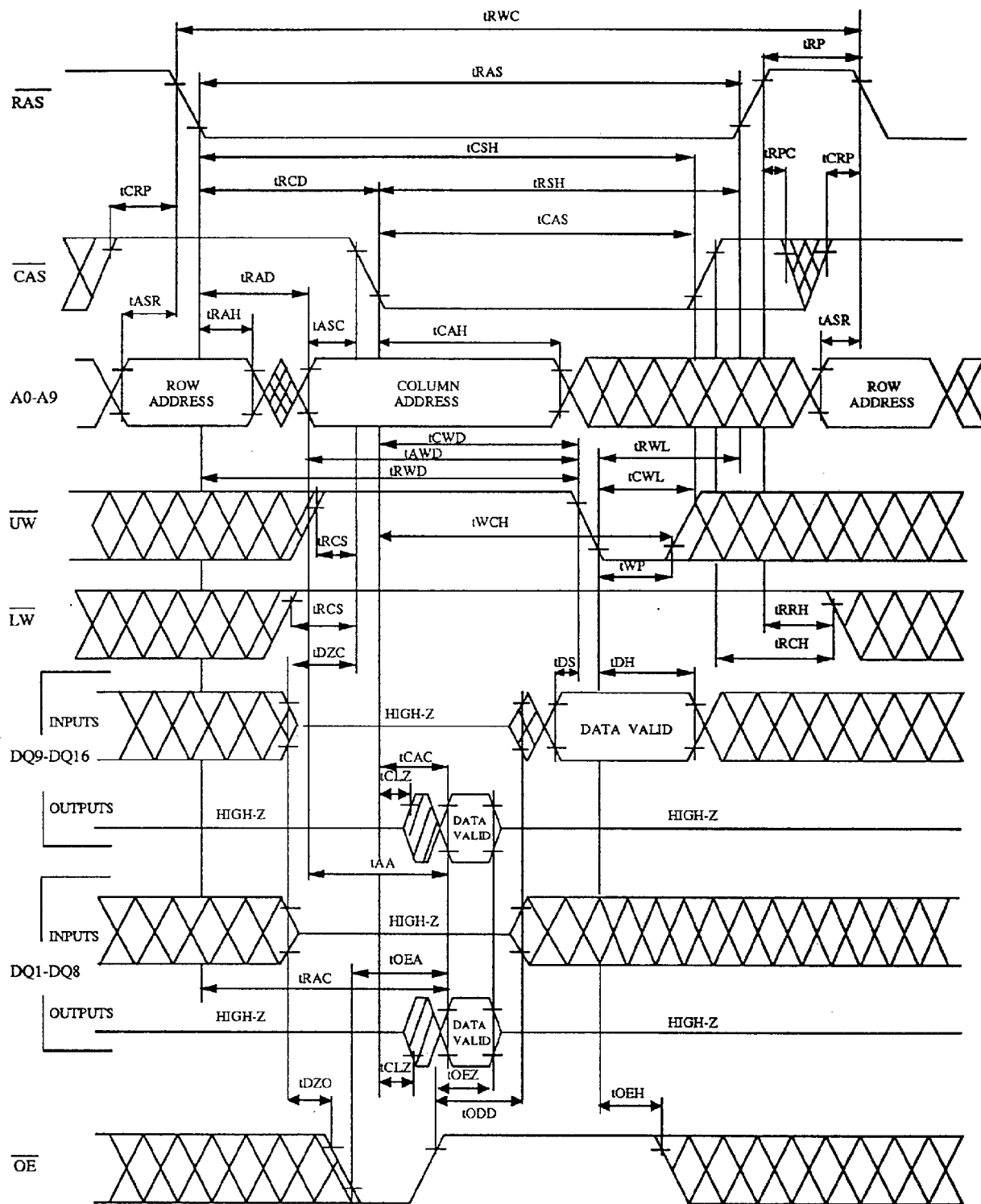
MITSUBISHI LSI

M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

MITSUBISHI (MEMORY/ASIC)

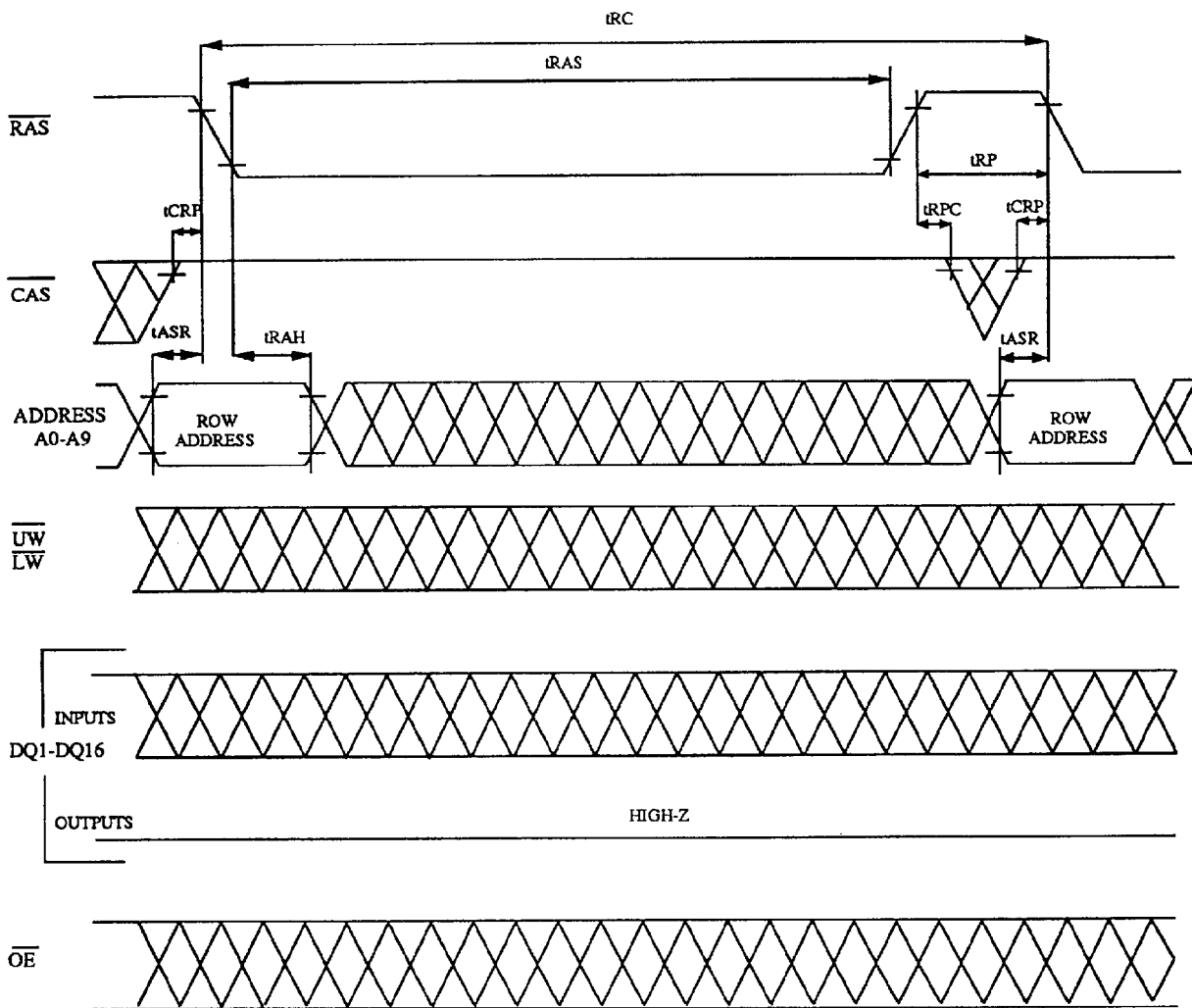
Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



Preliminary

MITSUBISHI LSIs
M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S
FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

$\overline{\text{RAS}}$ -only Refresh Cycle



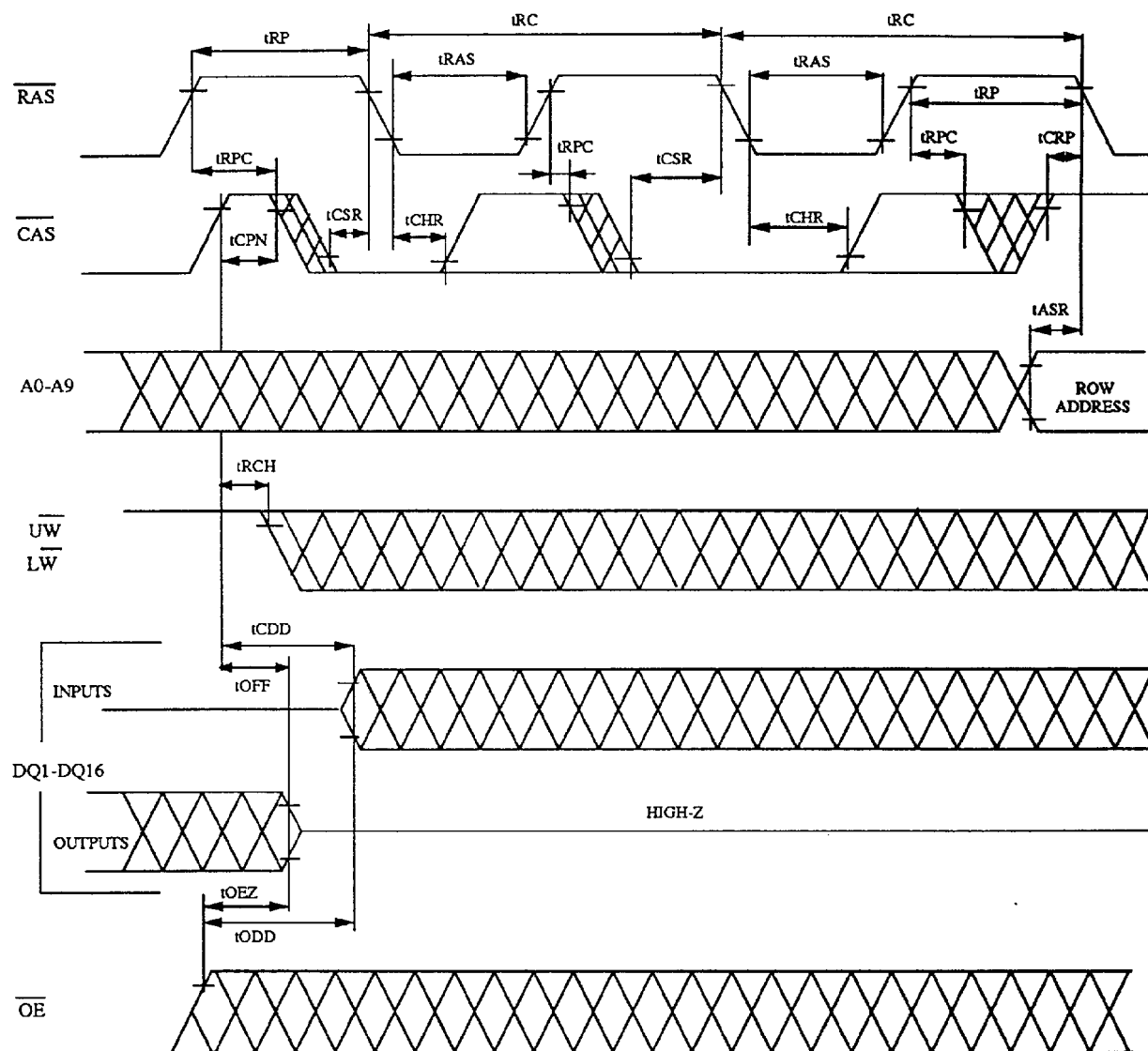
MITSUBISHI
ELECTRIC

Rev.B

Preliminary

MITSUBISHI LSI's
M5M44170AJ,TP,RT-6,-6S,-7,-7S,-8,-8S,-10,-10S
FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

CAS before RAS Refresh Cycle ,Extended Refresh Cycle *



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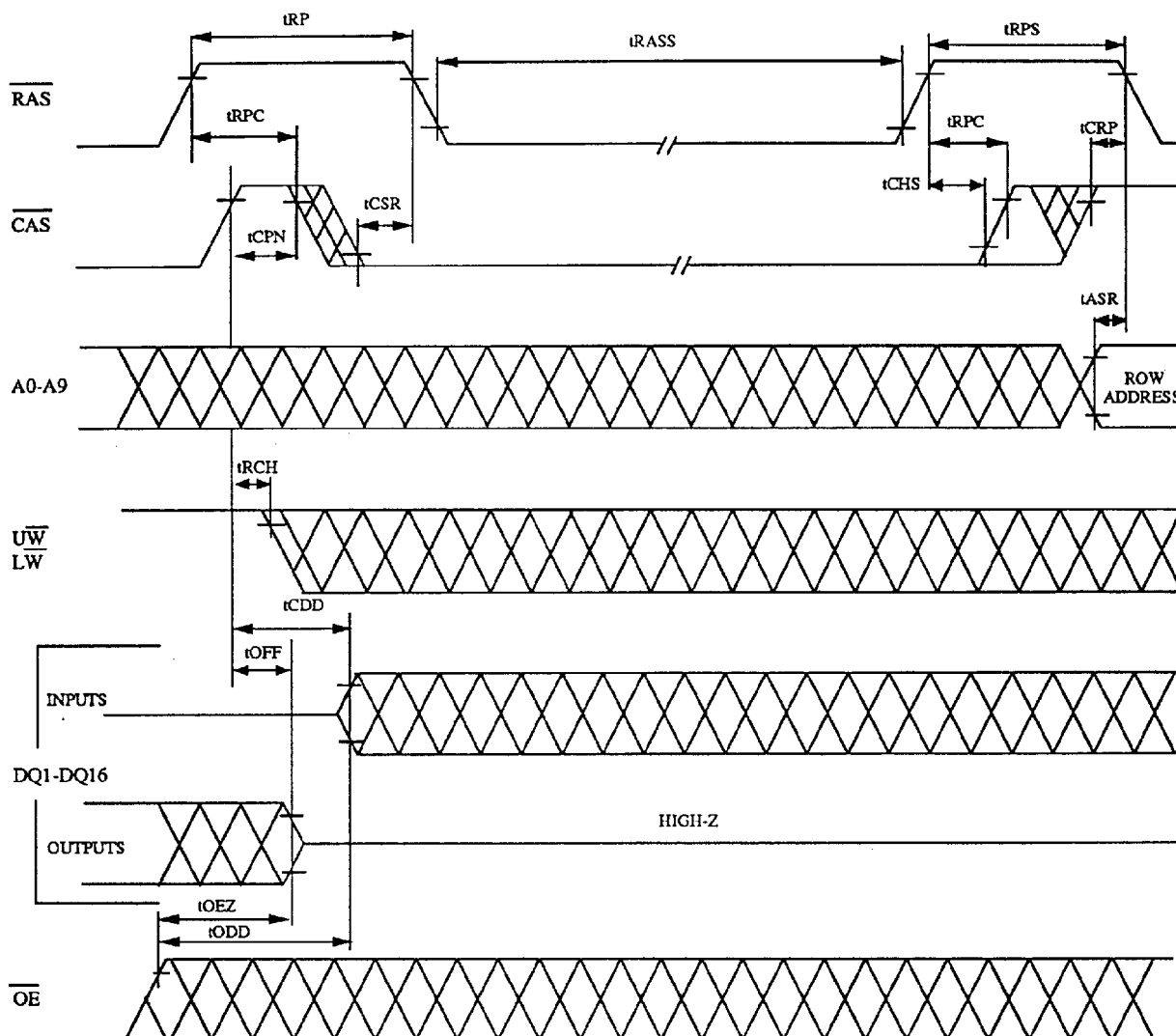
rev. B

Preliminary

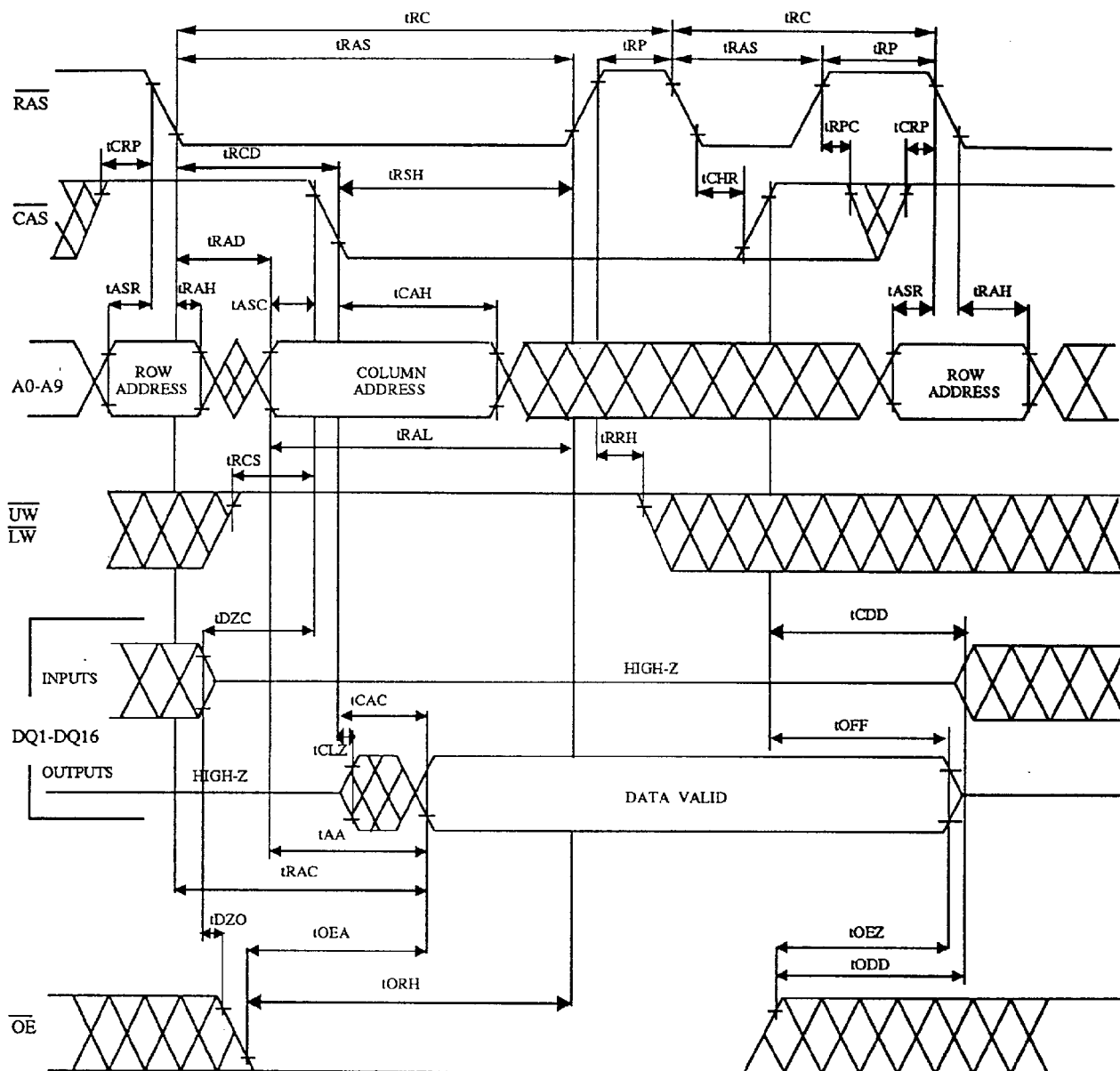
M5M44170AJ,TP,RT-6S,-7S,-8S,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

Self Refresh Cycle * (Note 28)



Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

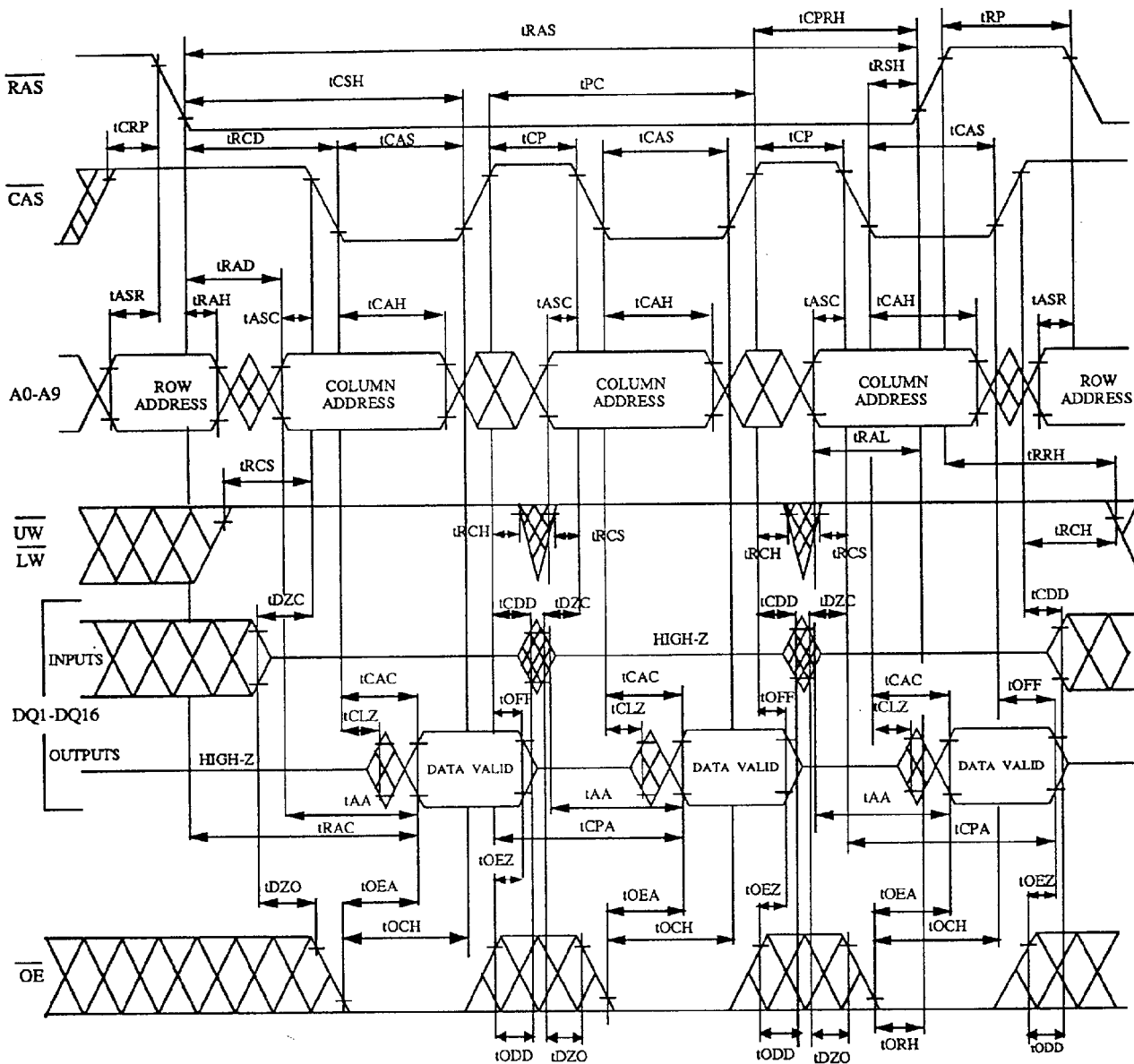
Preliminary

MITSUBISHI LSIs

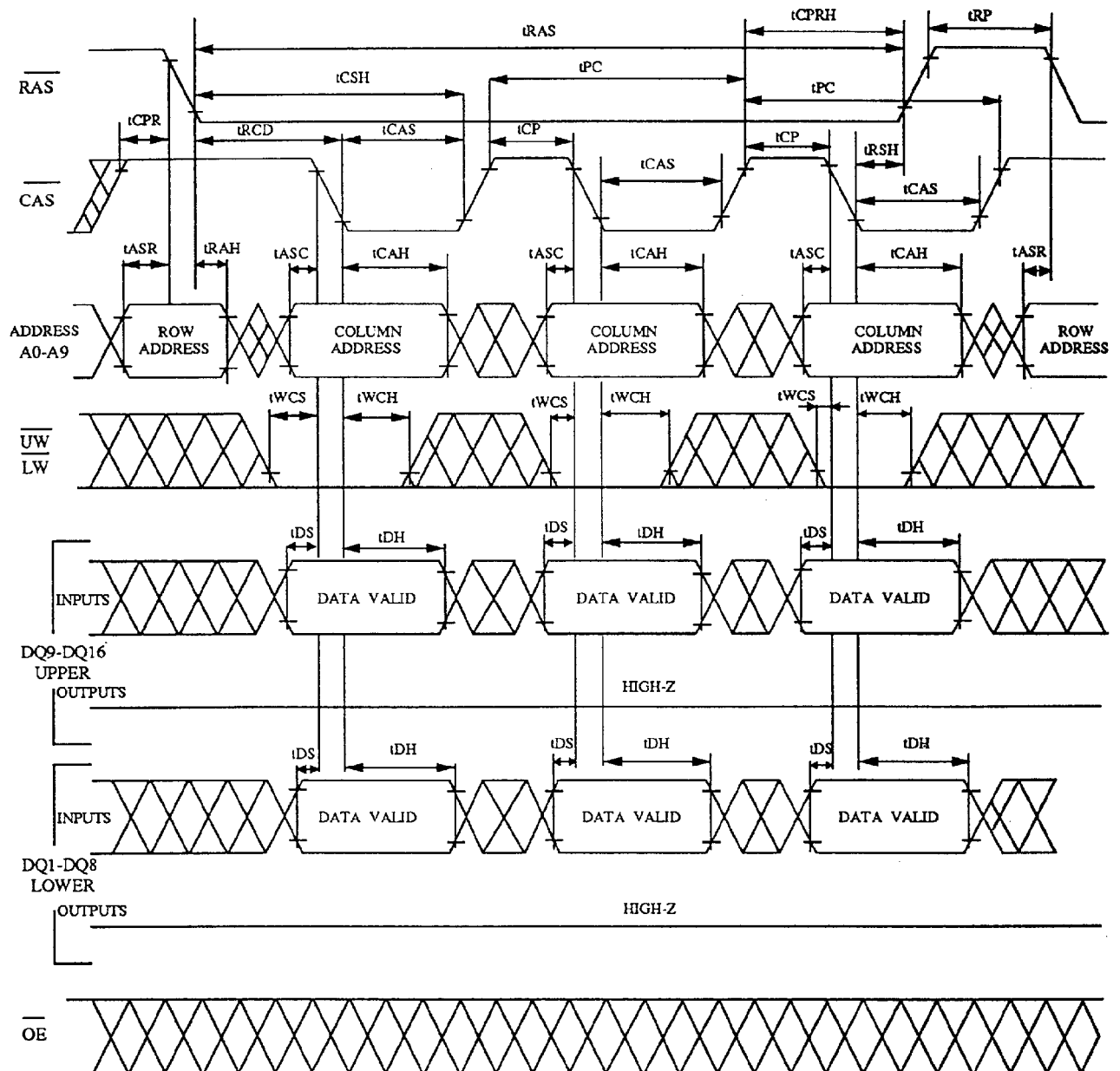
M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Read Cycle



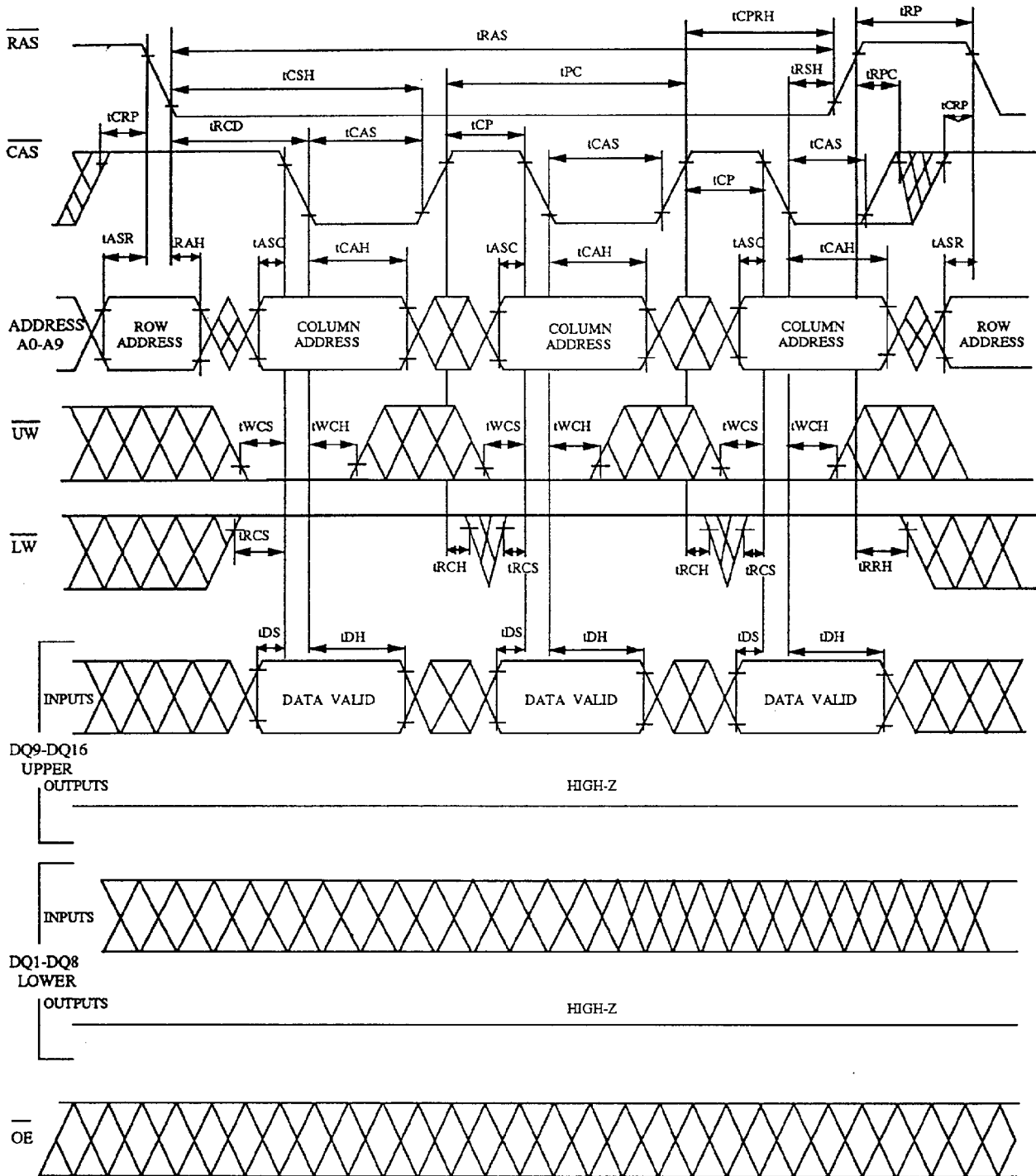
Fast Page Mode Write Cycle (Early Write)



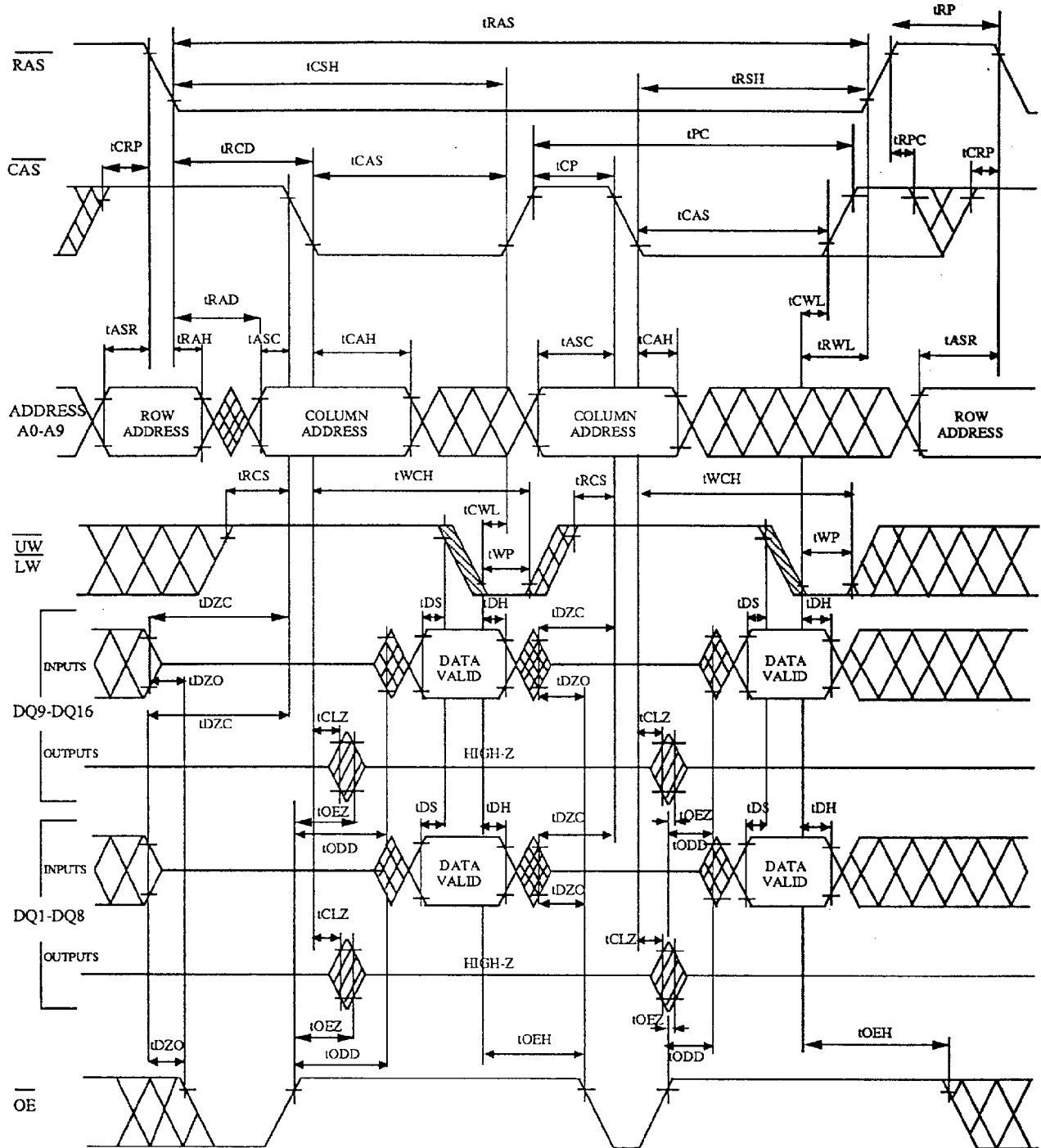
Preliminary

MITSUBISHI LSI's
M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S
FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

Fast Page Mode Upper/(Lower) Byte Write Cycle (Early Write)



Fast Page Mode Write Cycle (Delayed Write)

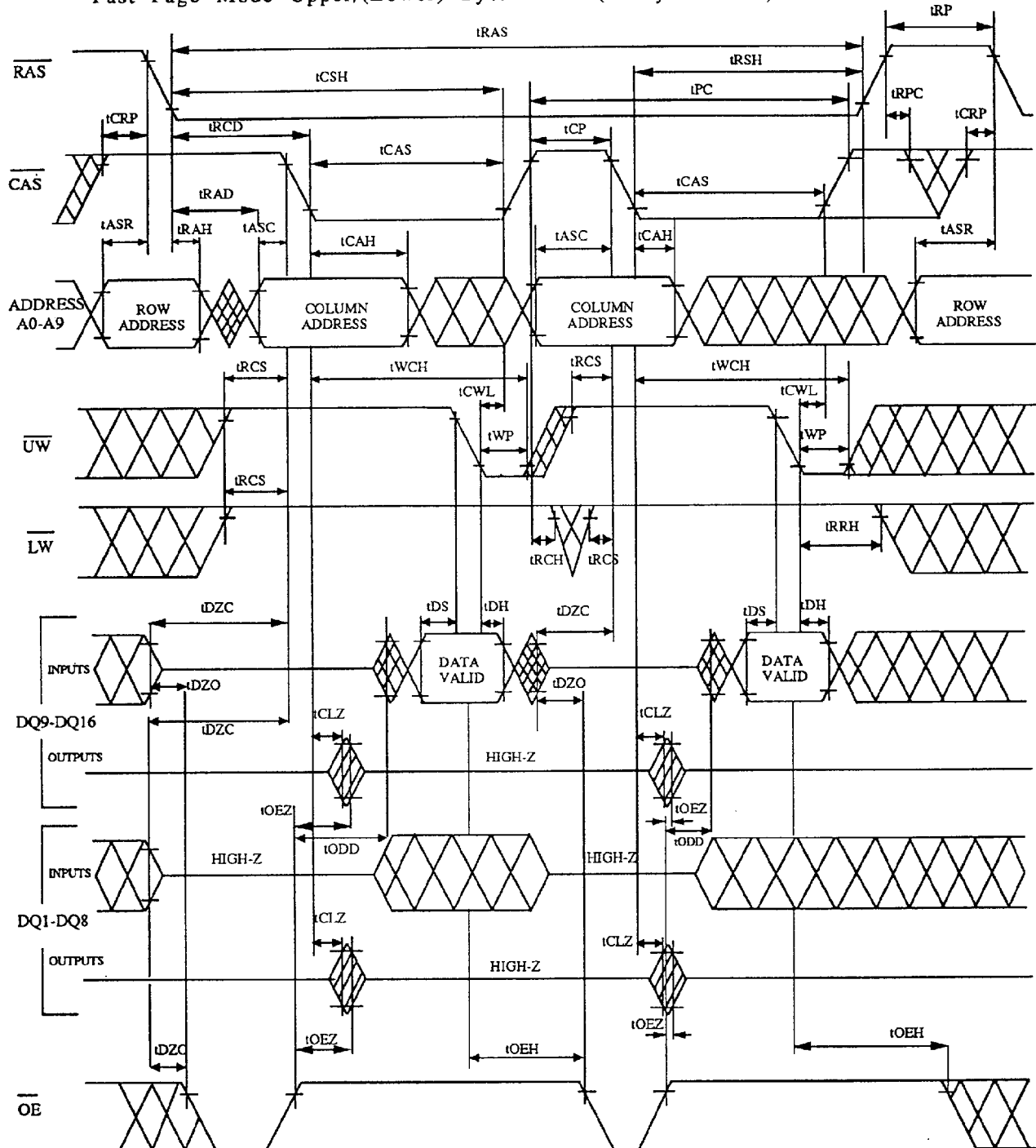


MITSUBISHI LSIs
6,-7,-8,-10,-6S,-7S,-8S,-10S

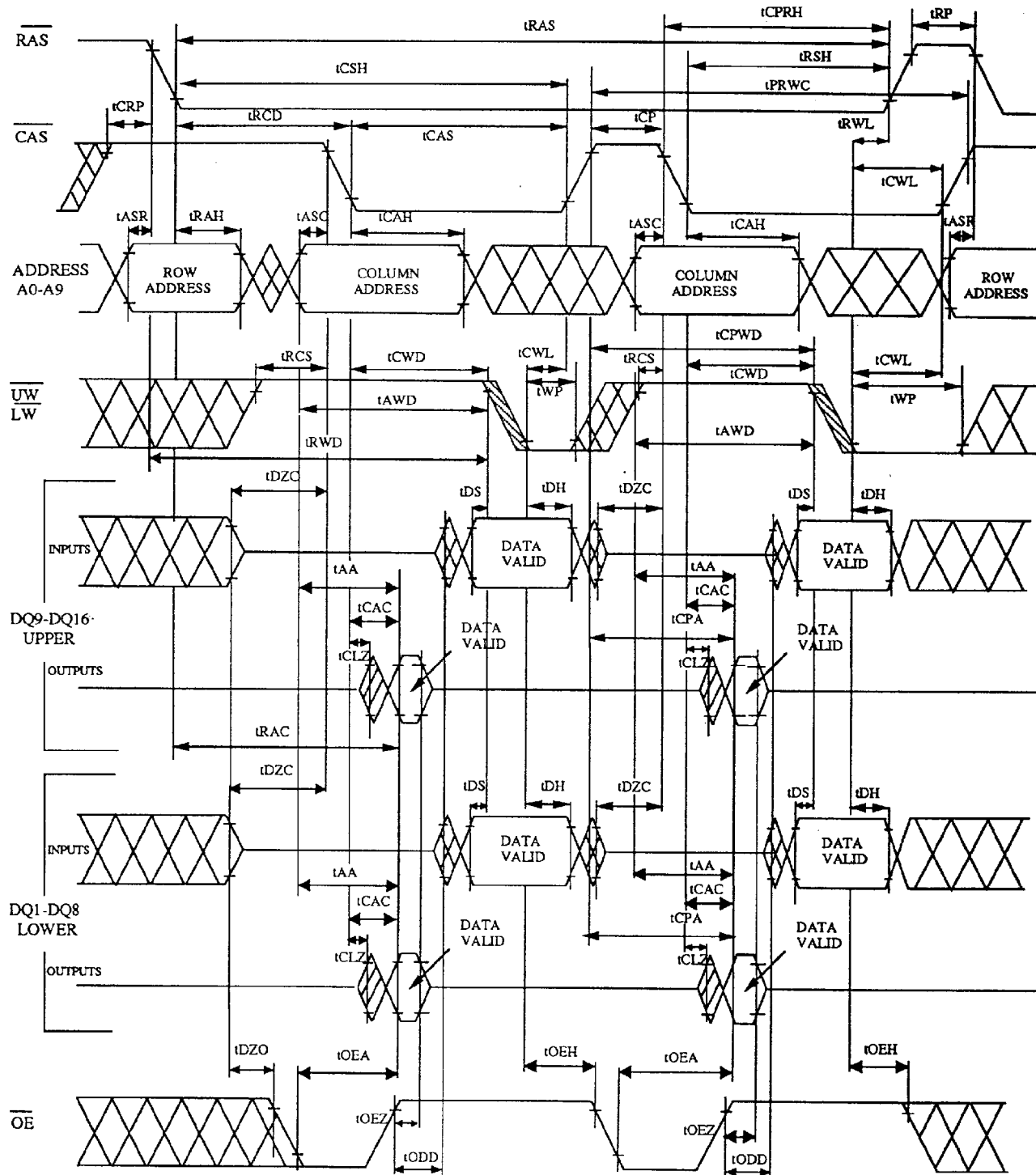
M5M44170AJ,L,TP,RT-6,-7,-8,-10,-6S,-7S,-8S,-10S

FAST PAGE MODE 4,194,304-BIT(262,144-WORD BY 16-BIT) DYNAMIC RAM

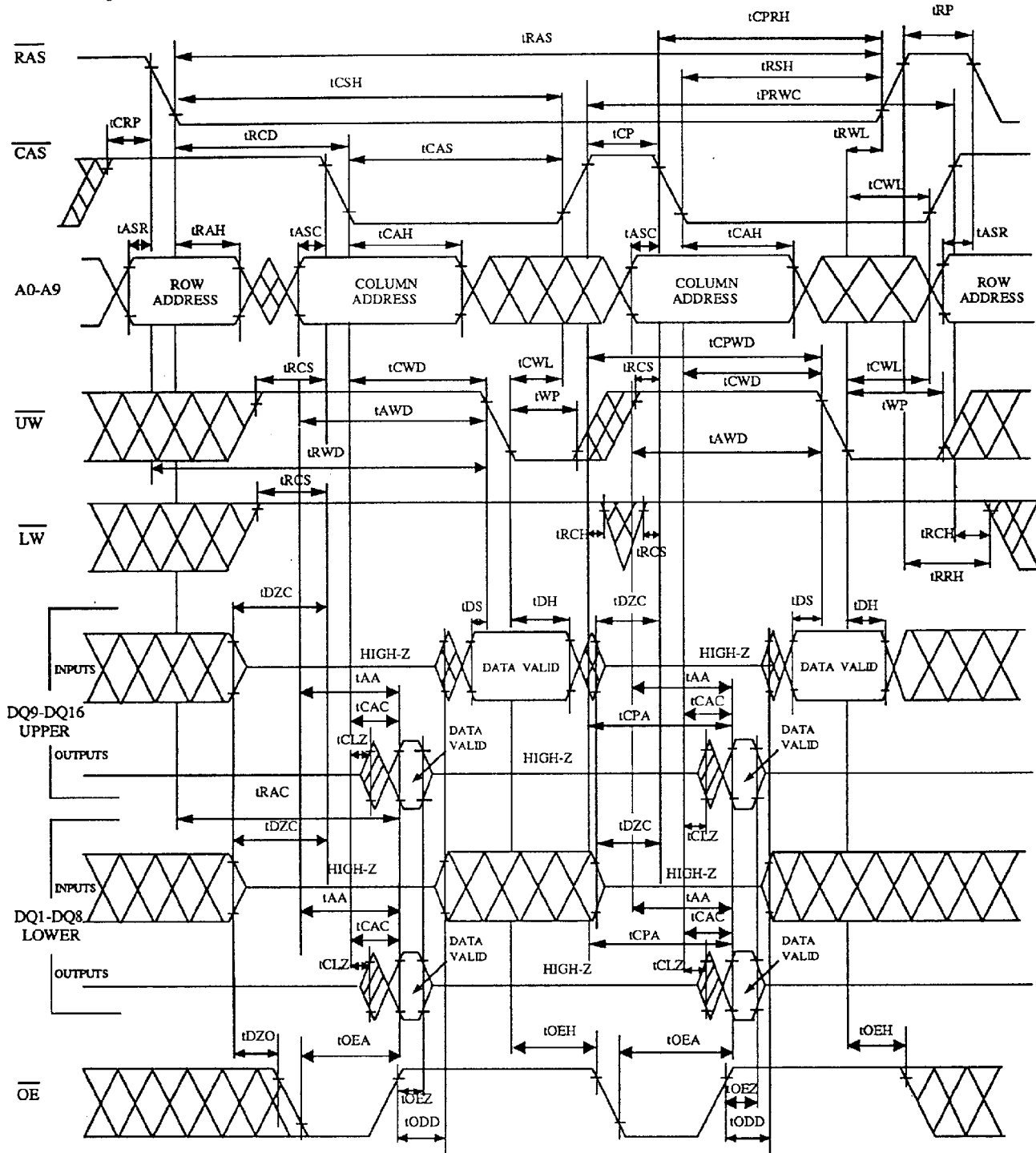
Fast Page Mode Upper/(Lower) Byte Write (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Fast Page Mode Read-Upper/(Lower) Write, Read-Modify-Upper/(Lower) Write Cycle



Note 2 8 Self refresh sequence

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Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{\text{RAS}}$ signal during self refresh period.

1. In case of $t_{\text{RASS}} < 300 \text{ ms}$

1.1 Distributed refresh during Read / Write operation

(A) Timing Diagrams

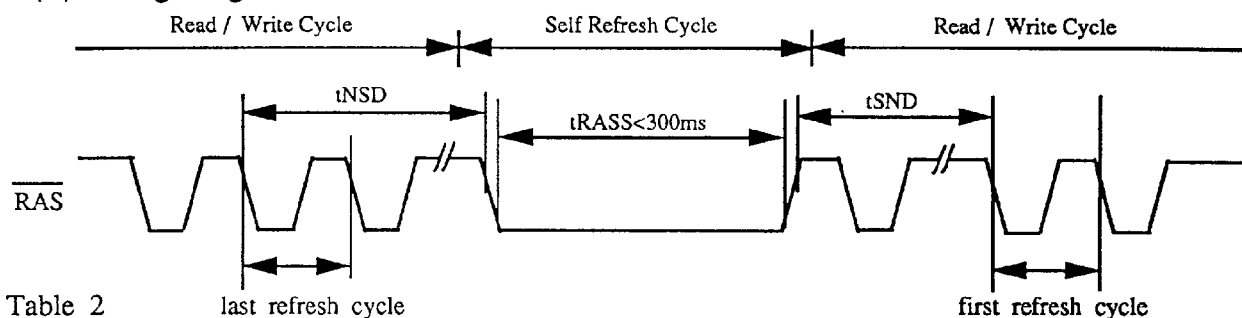


Table 2

Read / Write Cycle	Read / Write $\rightarrow$ Self Refresh	Self Refresh $\rightarrow$ Read / Write
CBR distributed refresh	$t_{\text{NSD}} + t_{\text{SND}} \leq 16.4 \text{ ms}$	
$\overline{\text{RAS}}$ only distributed refresh	$t_{\text{NSD}} \leq 16 \mu \text{ s}$	$t_{\text{SND}} \leq 16 \mu \text{ s}$

(B) Definition of distributed refresh

Definition of CBR distributed refresh (Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max) CBR cycles within 128 ms.

Definition of $\overline{\text{RAS}}$ only distributed refresh

All combination of nine row address signals ($A_0 - A_9$) are selected during 1024 constant period (16 μs max) $\overline{\text{RAS}}$ only refresh cycles within 16.4 ms.

Note : Hidden refresh may be used instead of CBR refresh, $\overline{\text{RAS}}/\overline{\text{CAS}}$ refresh may be used instead of $\overline{\text{RAS}}$ only refresh.

1.1.1. CBR distributed Refresh

● Switching from read / write operation to self refresh operation.

The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read / write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2)

● Switching from self refresh operation to read / write operation.

The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read / write operation period should be set within t_{SND} (shown in table 2)

1.1.2. $\overline{\text{RAS}}$ only distributed refresh

● Switching from read / write operation to self refresh operation.

The time interval t_{NSD} from the falling edge of $\overline{\text{RAS}}$ signal in the last $\overline{\text{RAS}}$ only refresh cycle during read / write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within $16 \mu \text{ s}$.

● Switching from self refresh operation to read / write operation.

The time interval t_{SND} from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read / write operation period should be set within $16 \mu \text{ s}$.

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1.2 Burst refresh during Read / Write operation

(A) Timing diagram

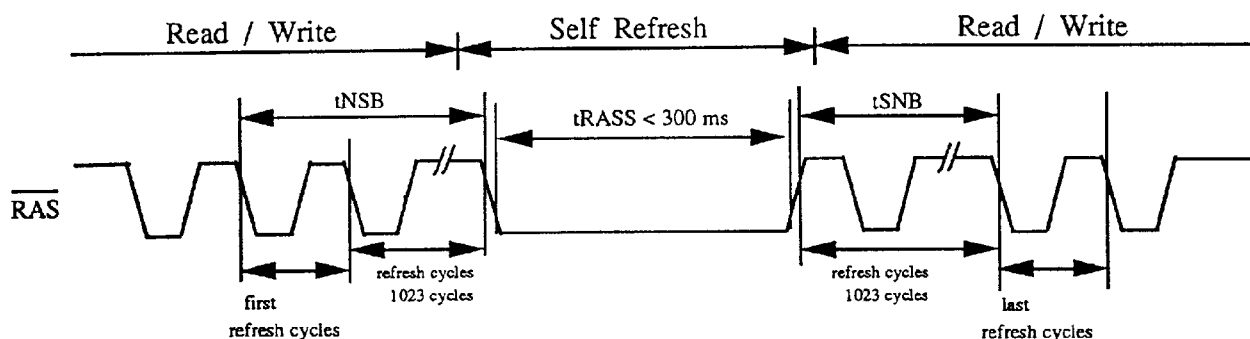


Table 3

Read / Write Cycle	Read / Write → Self Refresh	Self Refresh → Read / Write
CBR burst refresh	$t_{NSB} \leq 16.4 \text{ ms}$	$t_{SNB} \leq 16.4 \text{ ms}$
$\overline{\text{RAS}}$ only burst refresh	$t_{NSB} + t_{SNB} \leq 16.4 \text{ ms}$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4 ms.

Definition of $\overline{\text{RAS}}$ only burst refresh

All combination of ten row address signals (A0 - A9) are selected during 1024 continuous $\overline{\text{RAS}}$ only refresh cycles within 16.4 ms.

1.2.1 . CBR distributed Refresh

- Switching from read / write operation to self refresh operation.
The time interval t_{NSB} from the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read / write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 16.4 ms .
- Switching from self refresh operation to read / write operation.
The time interval t_{SNB} from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read / write operation period should be set within 16.4 ms.

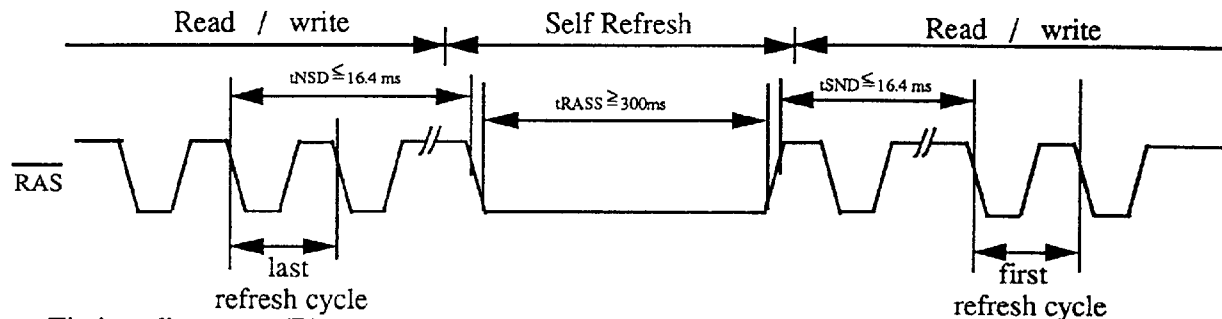
1.2.2 . $\overline{\text{RAS}}$ only distributed refresh

- Switching from read / write operation to self refresh operation.
The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the first $\overline{\text{RAS}}$ only refresh cycle during read / write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3)
- Switching from self refresh operation to read / write operation.
The time interval from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the last $\overline{\text{RAS}}$ only refresh cycle during read / write operation period should be set within t_{SNB} (shown in table 3)



2. In case of $t_{RASS} \geq 300 \text{ ms}$

Timing diagram - (A)



Timing diagram - (B)

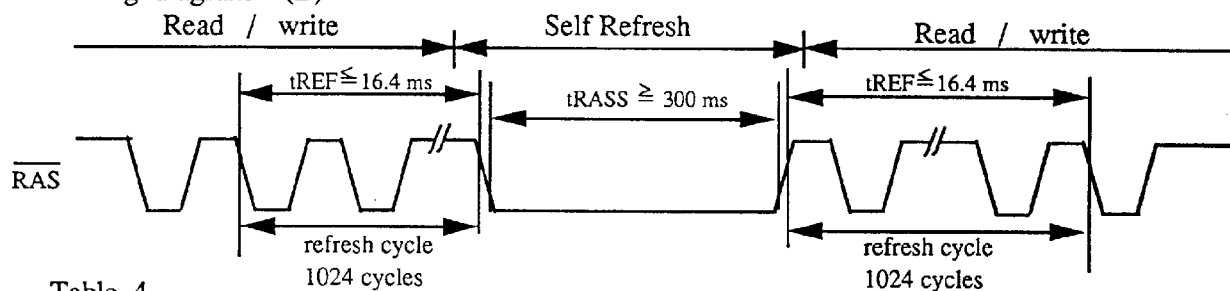


Table 4

Read / Write Cycle	Read / Write $\rightarrow$ Self Refresh	Self Refresh $\rightarrow$ Read / Write
CBR distributed refresh	Timing Diagram - A	Timing Diagram - A
$\overline{\text{RAS}}$ only distributed CBR burst refresh $\overline{\text{RAS}}$ only burst refresh	Timing Diagram - B	Timing Diagram - B

(B) Definition of refresh

The same as 1.1 - (B) and 1.2 - (B).

2.1.1 CBR distributed refresh

- Switching from read / write operation to self refresh operation .
The time interval t_{NSD} from the falling edge of $\overline{\text{RAS}}$ signal in the last CBR refresh cycle during read / write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 16.4 ms .
- Switching from self refresh operation to read / write operation .
The time interval t_{SND} from the rising edge of $\overline{\text{RAS}}$ signal at the end of self refresh operation to the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read / write operation period should be set within 16.4 ms .

2.1.2 $\overline{\text{RAS}}$ only distributed , CBR burst , $\overline{\text{RAS}}$ only burst refresh

- Before and after the self refresh , 1024 refresh cycles should be executed within 16.4 ms for each refresh operation .

