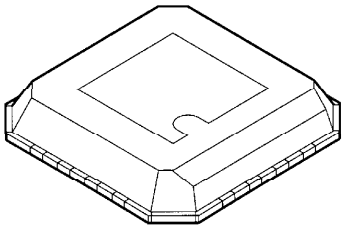
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB31251FL

1.4 GHz DUAL-PLL FREQUENCY SYNTHESIZER

This PLL frequency synthesizer is designed for use in digital mobile radio communications. It contains two channels of PLL circuits which can be controlled independently of each other.



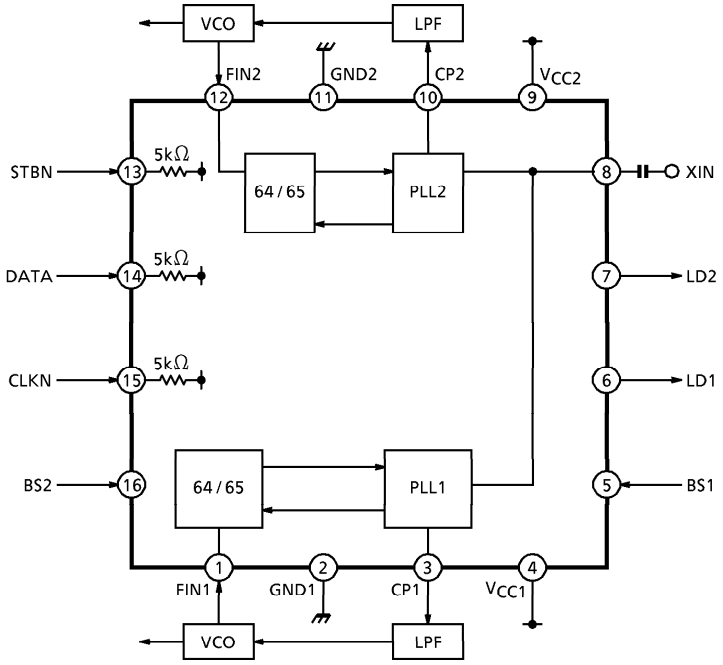
QON16-P-0404-0.65

Weight : 0.04 g (Typ.)

Abbreviated marked on product : B05

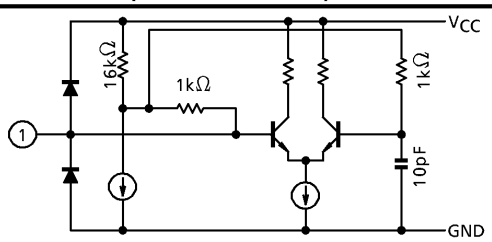
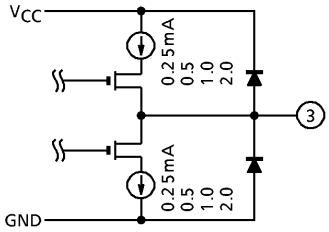
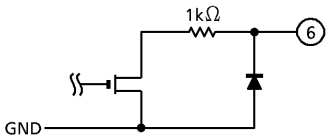
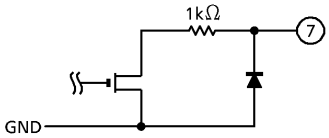
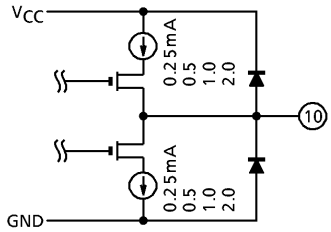
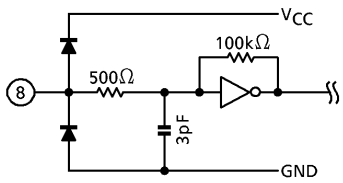
FEATURES

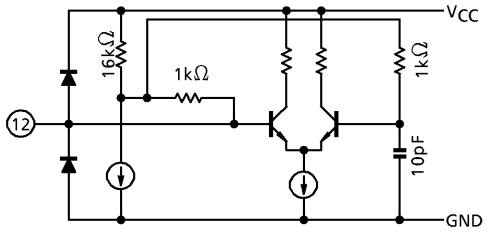
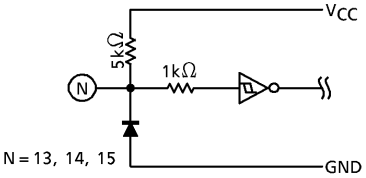
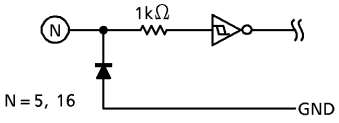
- Operating frequency PLL1 : 500 to 1400 MHz
  PLL2 : 500 to 1400 MHz
- Current consumption
  When operating in full : 6.0 mA (Typ.)
  PLL1 : 3.0 mA (Typ.)
  PLL2 : 3.0 mA (Typ.)
- Operating voltage range : 2.4 to 3.6 V
- Independent power-down (battery-saving) mode is possible
- Compact package : 16-pin QON (0.65 mm pitch)



Handle with care to prevent devices from deterioration by static electricity.

PIN FUNCTION (The values of resistor and capacitor are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT (PIN PERIPHERY)
1	FIN1	Prescaler input for PLL1. Use a VCO-oscillated frequency for this input.	
2	GND1	Ground.	—
3	CP1	PLL1 charge pump output. This is a constant-current output type.	
4	V_{CC1}	Power supply.	—
6	LD1	PLL1 lock detection output. This output is an NMOS open-drain type. Locked state : Open Unlocked state : Low Power-down state : Open	
7	LD2	PLL2 lock detection output. This output is an NMOS open-drain type. Locked state : Open Unlocked state : Low Power-down state : Open	
9	V_{CC2}	Power supply.	—
10	CP2	PLL2 charge pump output. This is a constant-current output type.	
8	XIN	Oscillator input.	
11	GND2	Ground.	—

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT (PIN PERIPHERY)
12	FIN2	Prescaler input for PLL2. Use a VCO-oscillated frequency for this input.	
13	STBN	Strobe input. (Pull-up resistor included, 5kΩ)	
14	DATA	Data input. (Pull-up resistor included, 5kΩ)	
15	CLKN	Clock input. (Pull-up resistor included, 5kΩ)	
5	BS1	Battery save for PLL1	
16	BS2	Battery save for PLL2	

DESCRIPTION

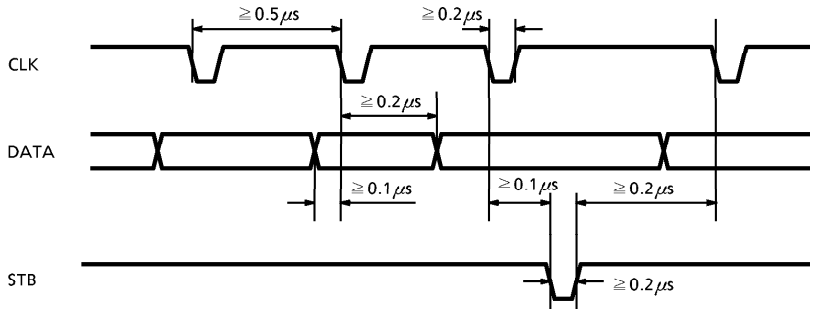
(1) Serial Data Input

The operation of this IC is controlled by a serial data program. Use the clock (CLK), data (DATA), and strobe (STB) pins to input the serial data.

(2) Method for Entering Serial Data

- The data is forwarded into the IC's internal shift register sequentially beginning with the LSB in synchronism with rising edges of the clock pulse. When all bits of data are forwarded, drive the strobe pin high. The data is latched in the appropriate place according to each content of control by a rising edge of this strobe signal. Control is initiated simultaneously when the data is stored in this place.
- The clock, data, and strobe pins each contain a Schmitt trigger circuit to eliminate noise-induced erroneous operation.
- At power-on, be sure to transmit option control before sending divide-by-n data.

(3) Serial Data Input Timing



(4) Group Code

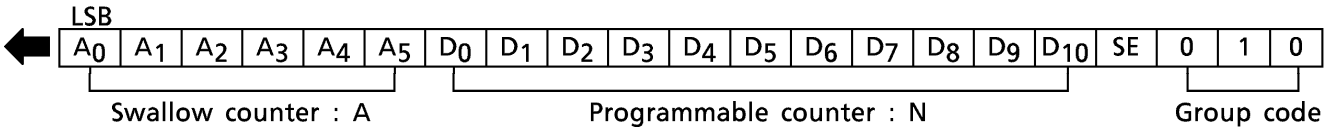
- The serially input data is grouped by the last 3 bits code.

Bit Before Preceding One	Previous Bit	Last Bit	Content of Control
0	1	0	Divide-by number for PLL1 programmable divider
0	0	1	Divide-by number for PLL2 programmable divider
0	1	1	Divide-by number for PLL1 reference divider
1	1	1	Divide-by number for PLL2 reference divider
0	0	0	Option control

(5) PLL1 Divide-by Data (21 bits)

- PLL1 is comprised of a 6-bit swallow counter (programmable counter), a 11-bit programmable counter, and a 2-modulus (1/64 and 1/65) prescaler.
- By sending data to the swallow and programmable counters, any desired divide-by number can be set in the range of 4,032 to 131,071.

PLL1



Divide-by number = 64N + A

$A = A_0 + A_1 \times 2^1 \ \ldots\ldots\ + A_5 \times 2^5$ A : Value of counter A (remainder)

$N = D_0 + D_1 \times 2^1 + \ \ldots\ldots\ + D_{10} \times 2^{10}$ N : Value of counter N (quotient)

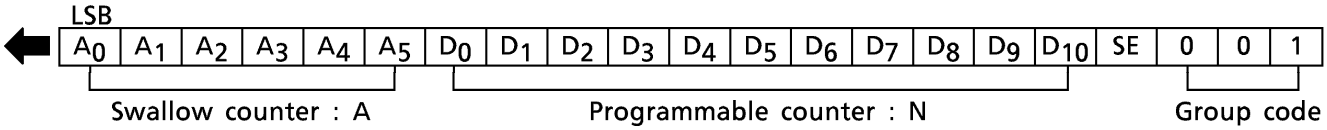
$4032 \leqq$ divide-by number $\leqq 131071$

SE	Frame structure
0	4 frames
1	5 frames

(6) PLL2 Divide-by Data (21 bits)

- PLL2 consists of a 6-bit swallow counter (programmable counter), a 11-bit programmable counter, and a 2-modulus (1/64 and 1/65) prescaler.
- By sending data to the swallow and programmable counters, any desired divide-by number can be set in the range of 4032 to 131071.

PLL2



Divide-by number = 64N + A

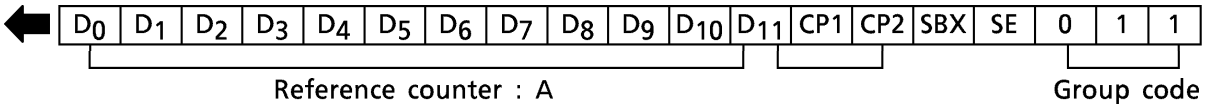
$A = A_0 + A_1 \times 2^1 \ \ldots\ldots\ + A_5 \times 2^5$ A : Value of counter A (remainder)

$N = D_0 + D_1 \times 2^1 + \ \ldots\ldots\ + D_{10} \times 2^{10}$ N : Value of counter N (quotient)

$4032 \leqq$ divide-by number $\leqq 131071$

SE	Frame structure
0	4 frames
1	5 frames

(7) PLL1 Reference Divider (19 bits)



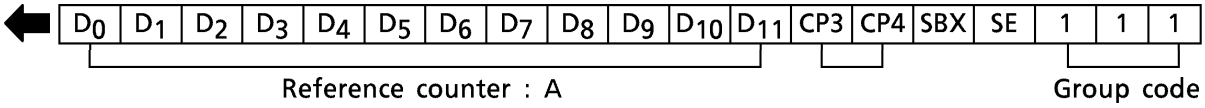
$D = D_0 + D_1 \times 2^1 \ \ldots\ldots\ + D_9 \times 2^9 + D_{10} \times 2^{10} + D_{11} \times 2^{11}$

$4 \leqq$ divide-by number $\leqq 4095$

SE	Frame structure
0	4 frames
1	5 frames

CP1	CP2	CP1 Output Current
0	0	0.25mA
0	1	0.5mA
1	0	1.0mA
1	1	2.0mA

(8) PLL2 Reference Divider (19 bits)



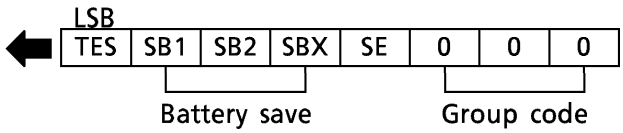
$D = D_0 + D_1 \times 2^1 + \ \ldots . \ D_9 \times 2^9 + D_{10} \times 2^{10} + D_{11} \times 2^{11}$

$4 \leqq$ divide-by number $\leqq 4095$

SE	Frame structure
0	4 frames
1	5 frames

CP3	CP4	CP2 Output Current
0	0	0.25mA
0	1	0.5mA
1	0	1.0mA
1	1	2.0mA

(9) Option Control



- Power-down mode

The PLL1, PLL2, and XIN can be switched between the power-down mode and operating state by using external battery save pins-BS1 and BS2-and the SB1, SB2, and SBX bits. This power-down mode is controlled in connection with the SB1 and SB2 bits as shown in the table below.

External Pin		Serial Data				Operating State		
BS1	BS2	SB1	SB2	SBX	SE	PLL1	PLL2	XIN
L	L	*	*	0	*	OFF	OFF	OFF
L	L	*	*	1	*	OFF	OFF	ON
L	H	*	*	*	*	OFF	ON	ON
H	L	*	*	*	*	ON	OFF	ON
H	H	*	*	*	0	ON	ON	ON
H	H	0	0	0	1	OFF	OFF	OFF
H	H	0	0	1	1	OFF	OFF	ON
H	H	0	1	*	1	OFF	ON	ON
H	H	1	0	*	1	ON	OFF	ON
H	H	1	1	*	1	ON	ON	ON

ON = Operating state ; OFF = Power-down state (Not operating), * = Don't Care

- Lock detection

When a phase error (in terms of time) falls within one TCXO count, the lock detection output timer is started. After 7 counts of phase comparison, the timer outputs a "locked" signal (high). When a phase error (in terms of time) becomes greater than one TCXO count, the timer outputs an "unlocked" signal (low).

Locked state = High ; Unlocked state = Low ; Power-down state = High.

MAXIMUM RATING (Ta = 25°C)

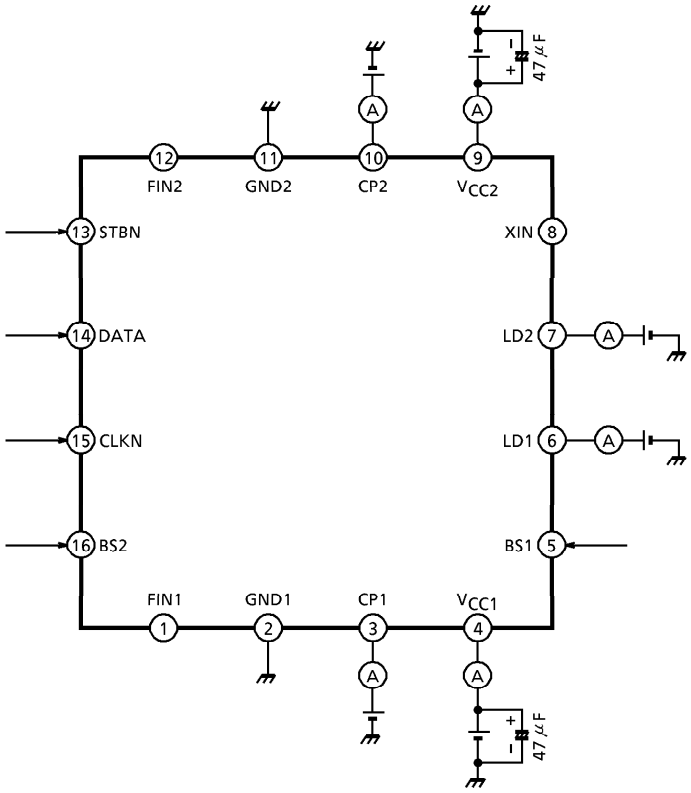
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	4	V
Power Dissipation	P_D	240	mW
Input Pin Voltage	V_{IN}	−0.5~4	V
LD Pin Sink Current	ILD-SINK	3	mA
Operating Temperature Range	V_{opr}	−40~85	°C
Storage Temperature Range	V_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 3.0V, Ta = 25°C)

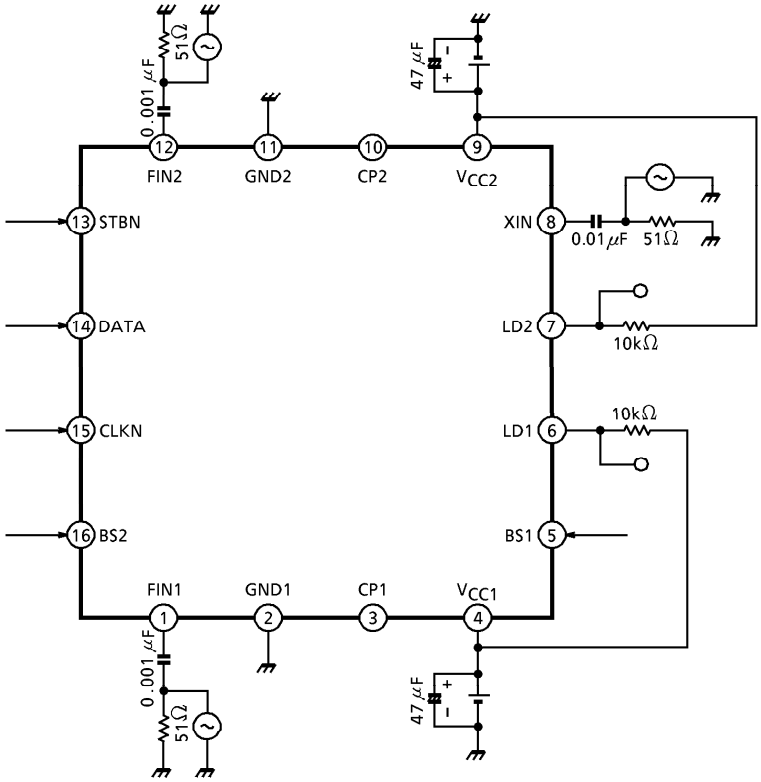
CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Operating Supply Voltage	V_{CC}	1		2.4	3.0	3.6	V
Current Consumption During No Signal 1~4	Icco1	1	During full operation	—	6.0	7.5	mA
	Icco2	1	BS1 = H, BS2 = L	—	3.0	4.0	mA
	Icco3	1	BS1 = L, BS2 = H	—	3.0	4.0	mA
	Icco4	1	BS1 = L, BS2 = L, SBX = 1	—	0.3	0.6	mA
Current Consumption During BS	Iccoq	1	BS1 = L, BS2 = L, SBX = 0	—	0	10	μA
Operating Frequency (PLL1)	F_{IN1}	2	V_{FIN1} = 92dBμV	500	—	1400	MHz
Operating Frequency (PLL2)	F_{IN2}	2	V_{FIN2} = 92dBμV	500	—	1400	MHz
FIN1 Input Level	V_{FIN1}	2	F_{IN1} = 500~1400MHz	92	—	107	dBμV
FIN2 Input Level	V_{FIN2}	2	F_{IN2} = 500~1400MHz	92	—	107	dBμV
Reference Operating Frequency	F_{XIN}	2	V_{XIN} = 97dBμV	5	—	20	MHz
Reference Input Voltage	V_{XIN}	2	F_{XIN} = 5~20MHz	97	—	110	dBμV
Clock Input Frequency	—	—		1	500	2000	kHz
Pull-up Resistance (Serial Data)	R_{SD}	—	CLKN, DATA, STBN	4.25	5	5.75	kΩ

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Charge Pump Output Current (PLL1)	ICP1	1	CP1 = 0, CP2 = 0	0.21	0.25	0.29	mA
			CP1 = 0, CP2 = 1	0.42	0.5	0.58	mA
			CP1 = 1, CP2 = 0	0.85	1.0	1.15	mA
			CP1 = 1, CP2 = 1	1.7	2.0	2.3	mA
Charge Pump Output Current (PLL2)	ICP2	1	CP3 = 0, CP4 = 0	0.21	0.25	0.29	mA
			CP3 = 0, CP4 = 1	0.42	0.5	0.58	mA
			CP3 = 1, CP4 = 0	0.85	1.0	1.15	mA
			CP3 = 1, CP4 = 1	1.7	2.0	2.3	mA
Charge Pump Output Off-Leakage	ICP (OFF)	1	$V_{CP} = 1 / 2\ V_{CC}$	−0.1	0	0.1	nA
High Level Input Voltage	V_{IH}	—	BS1, BS2, CLK, DATA, STB	$0.8 \times V_{CC}$	—	4.0	V
Low Level Input Voltage	V_{IL}	—	BS1, BS2, CLK, DATA, STB	GND	—	$0.2 \times V_{CC}$	V
LD Pin Off-Leakage	ILD	1	$V_{LD} = 3.6V$	−1	0	1	μA
LD Pin On-Resistance	RLD (ON)	1	$V_{LD} = 0.4V$	—	1	1.5	kΩ

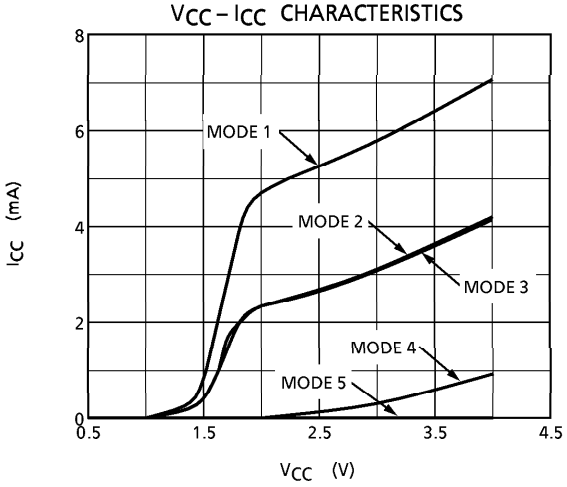
TEST CIRCUIT 1



TEST CIRCUIT 2

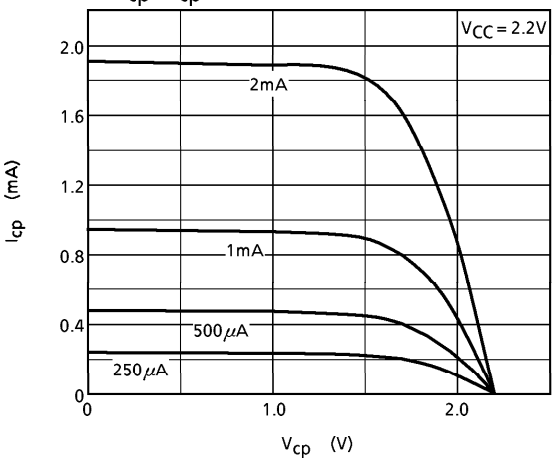


V_{CC} – I_{CC} CHARACTERISTICS

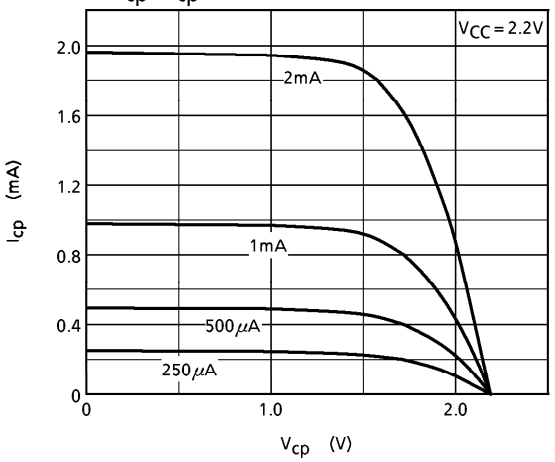


	PLL1	PLL2	Xin
MODE 1	ON	ON	ON
MODE 2	OFF	ON	ON
MODE 3	ON	OFF	ON
MODE 4	OFF	OFF	ON
MODE 5	OFF	OFF	OFF

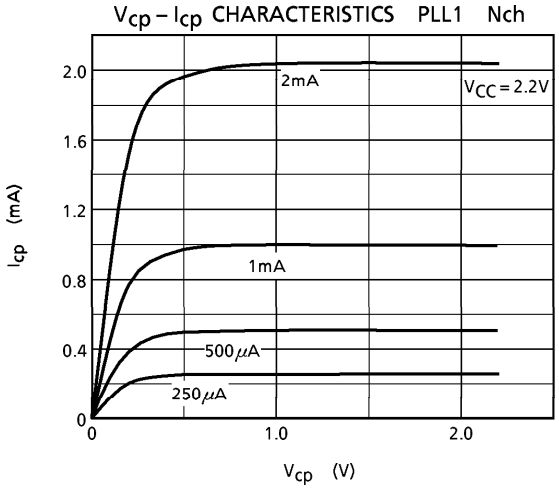
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Pch



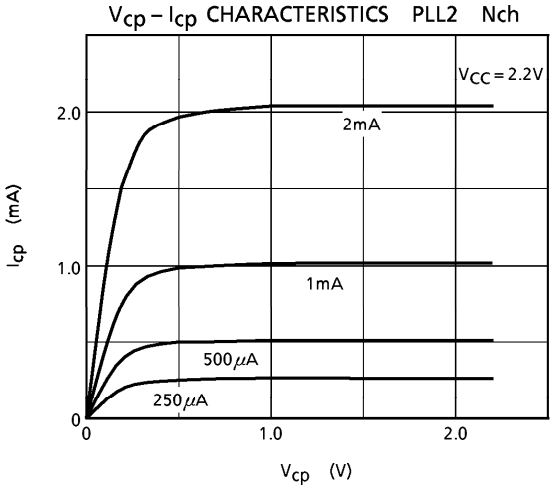
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Pch



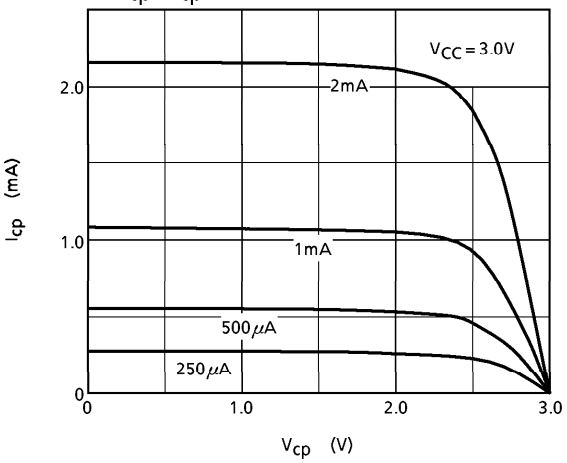
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Nch



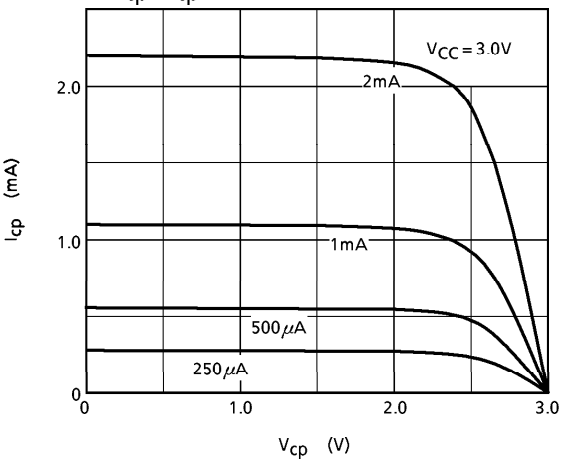
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Nch



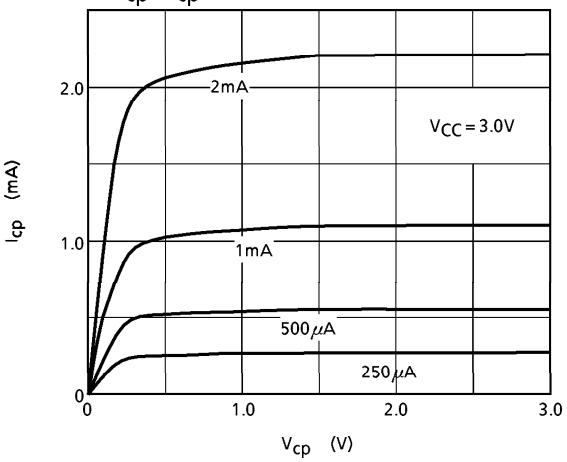
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Pch



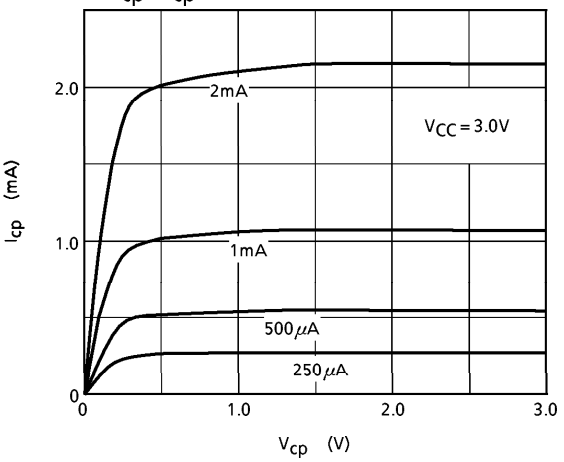
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Pch



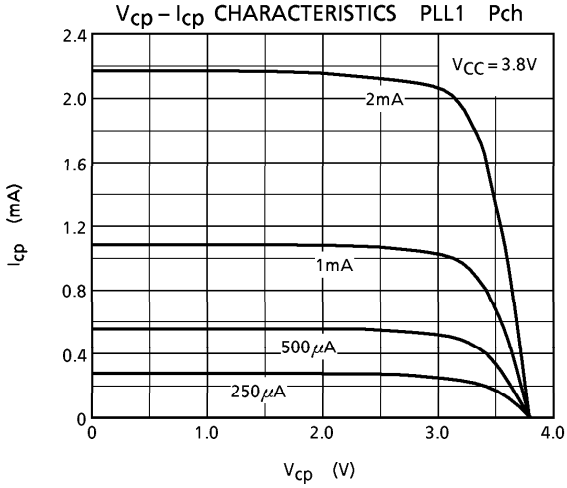
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Nch



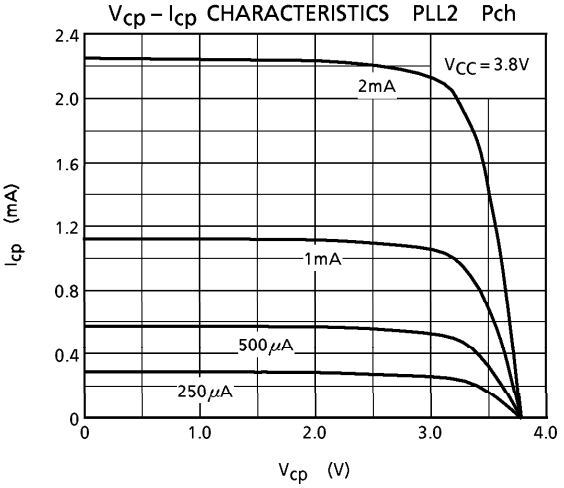
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Nch



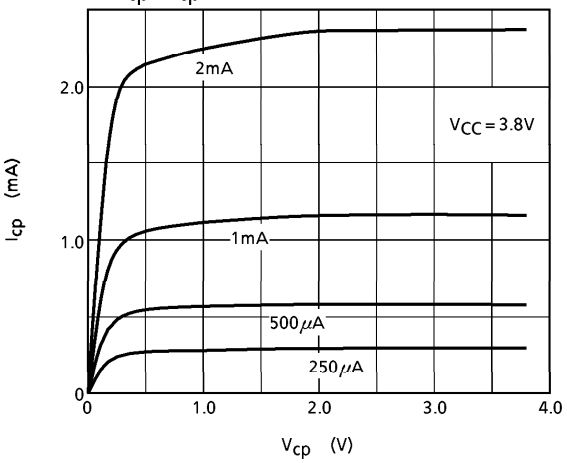
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Pch



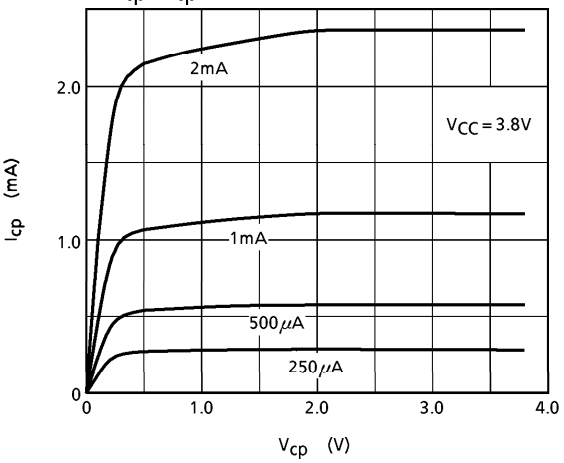
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Pch



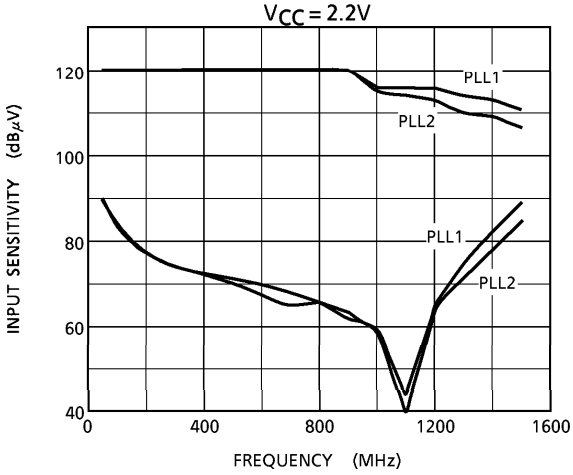
V_{cp} – I_{cp} CHARACTERISTICS PLL1 Nch



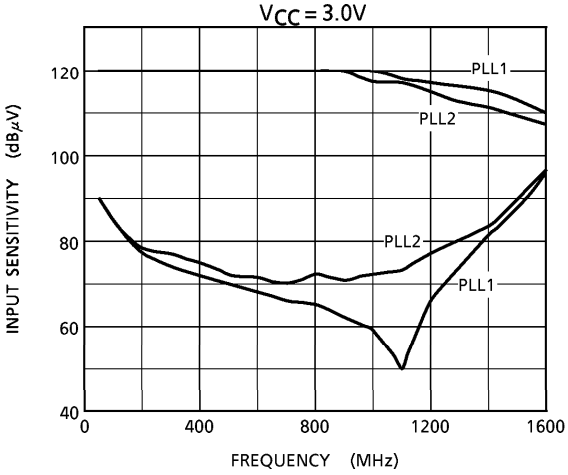
V_{cp} – I_{cp} CHARACTERISTICS PLL2 Nch



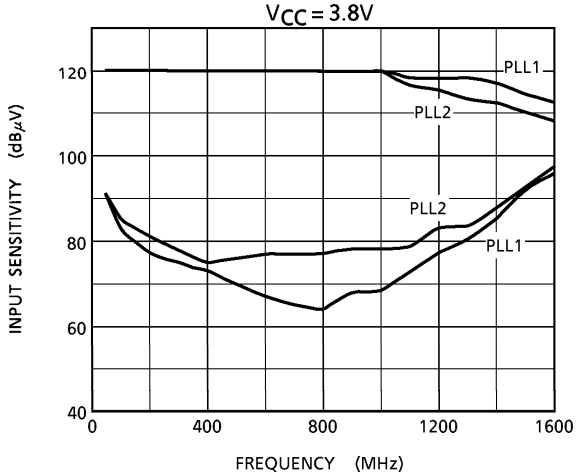
INPUT SENSITIVITIY CHARACTERISTICS
V_{CC} = 2.2V



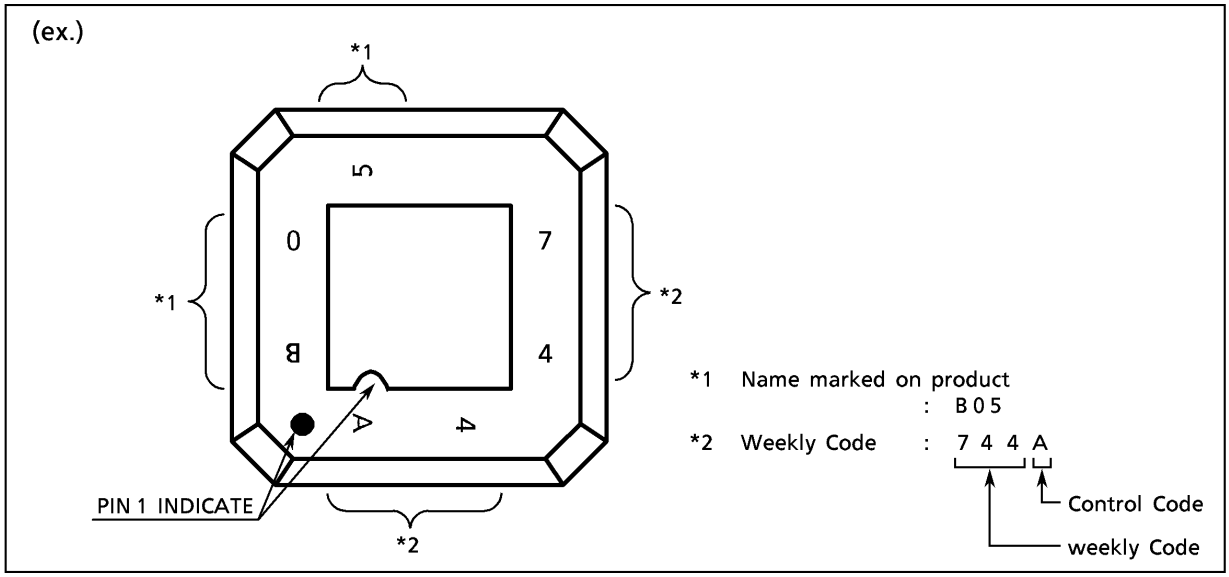
INPUT SENSITIVITIY CHARACTERISTICS
V_{CC} = 3.0V



INPUT SENSITIVITIY CHARACTERISTICS
V_{CC} = 3.8V



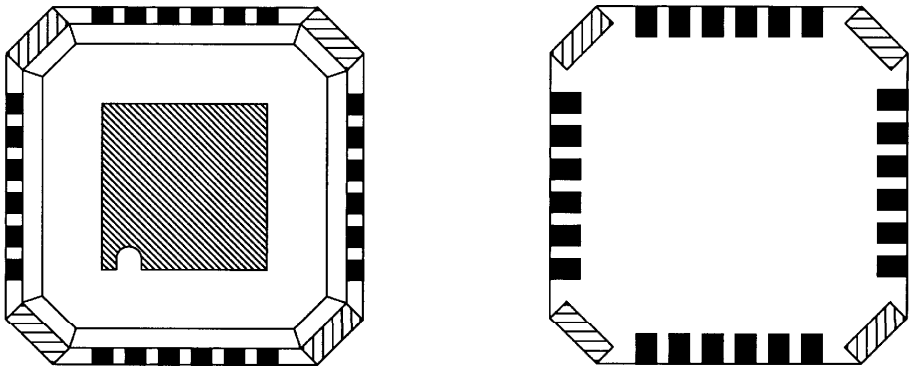
Type marked on product



Usage Precautions for Quad Outline Nonlead (QON)

A drawing is the conceptual figure of QON and is not an exact reduced scale drawing. The form of the island area and the lead count is not exact.

(TOP) (Bottom)



Before using QON, note the following items.

Notes

(1) Do not solder on the island areas (shaded in bottom view) in the four corners of the package for the purpose of strengthening mechanically.

(2) Electrically insulate externally (*1) the areas exposed on the surface of the package (shaded in top view) and the island areas in the four corners of the package (shaded in both top and bottom view)

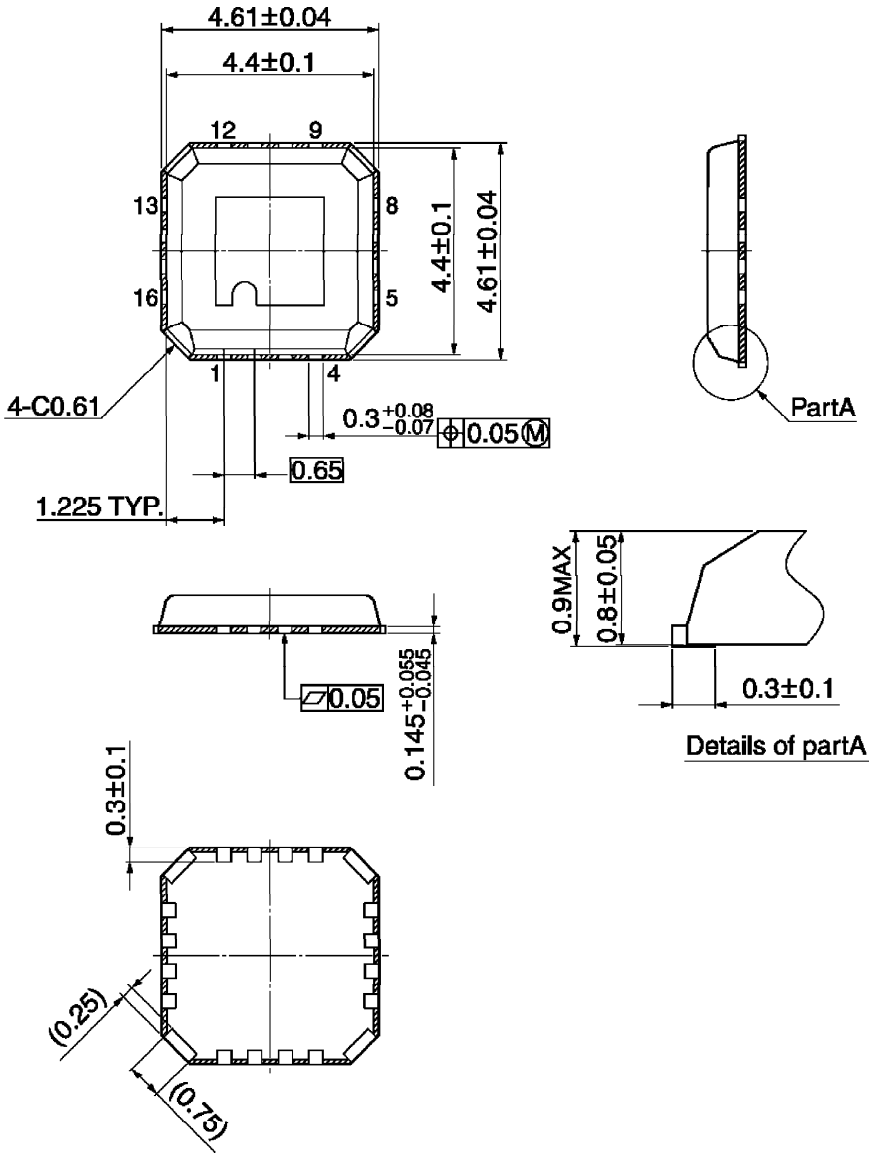
(3) When mounting or solder-mounting be careful not to apply static electricity or electrical overstress to the IC (protect the device from electrical leakage or charging).

(4) When using the IC in a set, design the set so that the structure does not allow any voltage to be directly applied to the island areas.

*1 : Make sure that on the substrate layout, soldering for through holes does not touch the island areas (shaded in bottom view).

PACKAGE DIMENSIONS

QON16-P-0404-0.65 Unit : mm



Note 1) The solder plating portion in four corners of tne package shall not be treated as an external terminal.

Note 2) Don`t carry out soldering to four corners of the package.

Note 3) ▨ area : Resin surface

Weight : 0.04 g (Typ.)

RESTRICTIONS ON PRODUCT USE

000707EDA

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