4-Channel, Simultaneous Sampling, High Speed, 12-Bit ADC

AD7864

FEATURES

High speed (1.65 µs) 12-bit ADC
4 simultaneously sampled inputs
4 track-and-hold amplifiers
0.35 µs track-and-hold acquisition time
1.65 µs conversion time per channel
HW/SW select of channel sequence for conversion
Single-supply operation
Selection of input ranges
±10 V, ±5 V for AD7864-1
±2.5 V for AD7864-3 0 V to 2.5 V, 0 V to 5 V for AD7864-2
High speed parallel interface that allows
Interfacing to 3 V processors
Low power, 90 mW typical
Power saving mode, 20 µW typical
Overvoltage protection on analog inputs

APPLICATIONS

AC motor control
Uninterrupted power supplies
Data acquisition systems
Communications

GENERAL DESCRIPTION

The AD7864 is a high speed, low power, 4-channel, simultaneous sampling 12-bit analog-to-digital converter (ADC) that operates from a single 5 V supply. The part contains a 1.65 µs successive approximation ADC, four track-and-hold amplifiers, a 2.5 V reference, an on-chip clock oscillator, signal conditioning circuitry, and a high speed parallel interface. The input signals on four channels sample simultaneously preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of ±10 V, ±5 V (AD7864-1), 0 V to +2.5 V, 0 V to +5 V (AD7864-2), and ±2.5 V (AD7864-3).

Any subset of the four channels can be converted to maximize the throughput rate on the selected sequence. Select the channels to convert via hardware (channel select input pins) or software (programming the channel select register).

A single conversion start signal ($\overline{\text{CONVST}}$) simultaneously places all the track-and-holds into hold and initiates a conversion sequence for the selected channels. The $\overline{\text{EOC}}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence.

FUNCTIONAL BLOCK DIAGRAM

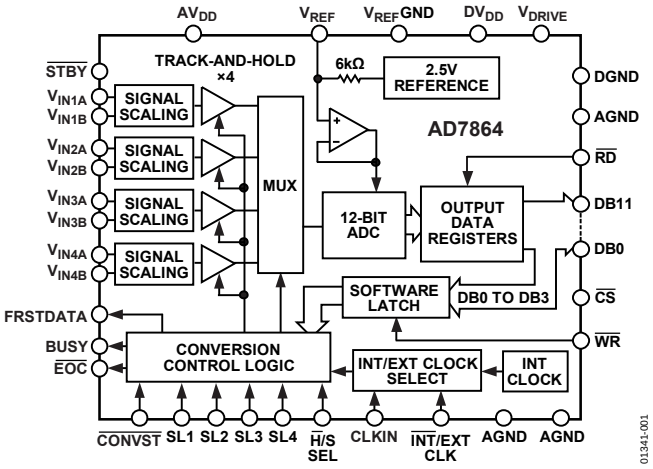

Figure 1.

Data is read from the part by a 12-bit parallel data bus using the standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals. Maximum throughput for a single channel is 500 kSPS. For all four channels, the maximum throughput is 130 kSPS for the read-during-conversion sequence operation. The throughput rate for the read-after-conversion sequence operation depends on the read cycle time of the processor. See the Timing and Control section. The AD7864 is available in a small (0.3 square inch area) 44-lead MQFP.

PRODUCT HIGHLIGHTS

1. Four track-and-hold amplifiers and a fast (1.65 µs) ADC for simultaneous sampling and conversion of any subset of the four channels.
2. A single 5 V supply consuming only 90 mW typical, makes it ideal for low power and portable applications. See the Standby Mode Operation section.
3. High speed parallel interface for easy connection to microprocessors, microcontrollers, and digital signal processors.
4. Available in three versions with different analog input ranges. The AD7864-1 offers the standard industrial input ranges of ±10 V and ±5 V; the AD7864-3 offers the common signal processing input range of ±2.5 V; the AD7864-2 can be used in unipolar, 0 V to 2.5 V and 0 V to 5 V, applications.
5. Features very tight aperture delay matching between the four input sample-and-hold amplifiers.

Rev. D

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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- AD7864: 4-Channel, Simultaneous Sampling, High Speed, 12-Bit ADC Data Sheet

TOOLS AND SIMULATIONS

- AD7864 IBIS Model

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7864 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7864 EngineerZone Discussions.

SAMPLE AND BUY

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TECHNICAL SUPPORT

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SPECIFICATIONS

V_{DD} = 5 V ± 5%, AGND = DGND = 0 V, V_{REF} = internal, clock = internal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Version[1]	B Version	Unit	Test Conditions/Comments
SAMPLE AND HOLD				
−3 dB Full Power Bandwidth	3	3	MHz typ	
Aperture Delay	20	20	ns max	
Aperture Jitter	50	50	ps max	
Aperture Delay Matching	4	4	ns max	
DYNAMIC PERFORMANCE[2]				f_{IN} = 100.0 kHz, f_S = 500 kSPS
Signal-to-(Noise + Distortion) Ratio[3]				
@ 25°C	70	72	dB min	
T_{MIN} to T_{MAX}	70	70	dB min	
Total Harmonic Distortion[3]	−80	−80	dB max	
Peak Harmonic or Spurious Noise[3]	−80	−80	dB max	
Intermodulation Distortion[3]				fa = 49 kHz, fb = 50 kHz
Second-Order Terms	−80	−80	dB typ	
Third-Order Terms	−80	−80	dB typ	
Channel-to-Channel Isolation[3]	−80	−80	dB max	f_{IN} = 50 kHz sine wave
DC ACCURACY				Any channel
Resolution	12	12	Bits	
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±0.9	±0.9	LSB max	No missing codes
AD7864-1				
Positive Gain Error[3]	±3	±3	LSB max	
Positive Gain Error Match[3]	+3	±3	LSB max	
Negative Gain Error[3]	±3	±3	LSB max	
Negative Gain Error Match[3]	+3	±3	LSB max	
Bipolar Zero Error	±4	±3	LSB max	
Bipolar Zero Error Match	+2	±2	LSB max	
AD7864-3				
Positive Gain Error[3]	±3		LSB max	
Positive Gain Error Match[3]	2		LSB max	
Negative Gain Error[3]	±3		LSB max	
Negative Gain Error Match[3]	2		LSB max	
Bipolar Zero Error	±3		LSB max	
Bipolar Zero Error Match	2		LSB max	
AD7864-2				
Positive Gain Error[3]	±3		LSB max	
Positive Gain Error Match[3]	3		LSB max	
Unipolar Offset Error	±3		LSB max	
Unipolar Offset Error Match	2		LSB max	
ANALOG INPUTS				
AD7864-1				
Input Voltage Range	±5, ±10	±5, ±10	V	
Input Resistance	9, 18	9, 18	kΩ min	
AD7864-3				
Input Voltage Range	±2.5	±2.5	V	
Input Resistance	4.5	4.5	kΩ min	

Parameter	A Version[1]	B Version	Unit	Test Conditions/Comments
AD7864-2				
Input Voltage Range	0 to 2.5, 0 to 5	0 to 2.5, 0 to 5	V	
Input Current (0 V to 2.5 V Option)	±100	±100	nA max	
Input Resistance (0 V to 5 V Option)	9	9	kΩ min	
REFERENCE INPUT/OUTPUT				
V_{REF} In Input Voltage Range	2.375/2.625	2.375/2.625	V_{MIN}/V_{MAX}	2.5 V ± 5%
V_{REF} In Input Capacitance[4]	10	10	pF max	
V_{REF} Out Output Voltage	2.5	2.5	V nom	
V_{REF} Out Error @ 25°C	±10	±10	mV max	
V_{REF} Out Error T_{MIN} to T_{MAX}	±20	±20	mV max	
V_{REF} Out Temperature Coefficient	25	25	ppm/°C typ	
V_{REF} Out Output Impedance	6	6	kΩ typ	See the Reference section
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	µA max	
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	4.0	4.0	V min	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11 to DB0				
High Impedance				
Leakage Current	±10	±10	µA max	
Capacitance[4]	10	10	pF max	
Output Coding				
AD7864-1, AD7864-3	Twos complement			
AD7864-2	Straight (natural) binary			
CONVERSION RATE				
Conversion Time	1.65	1.65	µs max	For one channel
Track-And-Hold Acquisition Time[2, 3]	0.35	0.35	µs max	
Throughput Time	130	130	kSPS max	For all four channels
POWER REQUIREMENTS				
V_{DD}	5	5	V nom	±5% for specified performance
I_{DD}				5 µA typical, logic inputs = 0 V or V_{DD}
Normal Mode	24	24	mA max	
Standby Mode	20	20	µA max	Typically 4 µA
Power Dissipation				
Normal Mode	120	120	mW max	Typically 90 mW
Standby Mode	100	100	µW max	Typically 20 µW

[1] Temperature ranges are as follows: A, B versions: –40°C to +85°C. The A version is fully specified up to 105°C with a maximum sample rate of 450 kSPS and I_{DD} maximum (normal mode) of 26 mA.
[2] Performance is measured through the full channel (SHA and ADC).
[3] See the Terminology section.
[4] Sample tested at initial release to ensure compliance.

TIMING CHARACTERISTICS

V_{DRIVE} = 5 V± 5%, AGND = DGND = 0 V, V_{REF} = internal, clock = internal; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.[1, 2]

Table 2.

Parameter	A, B Versions	Unit	Test Conditions/Comments
t_{CONV}	1.65	µs max	Conversion time, internal clock
	13	Clock cycles	Conversion time, external clock
	2.6	µs max	CLKIN = 5 MHz
t_{ACQ}	0.34	µs max	Acquisition time
t_{BUSY}	No. of channels × (t_{CONV} + t_9) − t_9	µs max	Selected number of channels multiplied by (t_{CONV} + $\overline{EOC}$ pulse width)—$\overline{EOC}$ pulse width
$t_{WAKE-UP}$ —External V_{REF}	2	µs max	$\overline{STBY}$ rising edge to $\overline{CONVST}$ rising edge
$t_{WAKE-UP}$ —Internal V_{REF}[3]	6	ms max	$\overline{STBY}$ rising edge to $\overline{CONVST}$ rising edge
t_1	35	ns min	$\overline{CONVST}$ pulse width
t_2	70	ns max	$\overline{CONVST}$ rising edge to BUSY rising edge
READ OPERATION			
t_3	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_4	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_5	35	ns min	Read pulse width, V_{DRIVE} = 5 V
	40	ns min	Read pulse width, V_{DRIVE} = 3 V
t_6[4]	35	ns max	Data access time after falling edge of $\overline{RD}$, V_{DRIVE} = 5 V
	40	ns max	Data access time after falling edge of $\overline{RD}$, V_{DRIVE} = 3 V
t_7[5]	5	ns min	Bus relinquish time after rising edge of $\overline{RD}$
	30	ns max	
t_8	10	ns min	Time between consecutive reads
t_9	75	ns min	$\overline{EOC}$ pulse width
	180	ns max	
t_{10}	70	ns max	$\overline{RD}$ rising edge to FRSTDATA edge (rising or falling)
t_{11}	15	ns max	$\overline{EOC}$ falling edge to FRSTDATA falling delay
t_{12}	0	ns min	$\overline{EOC}$ to $\overline{RD}$ delay
WRITE OPERATION			
t_{13}	20	ns min	$\overline{WR}$ pulse width
t_{14}	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_{15}	0	ns min	$\overline{WR}$ to $\overline{CS}$ hold time
t_{16}	5	ns min	Input data setup time of rising edge of $\overline{WR}$
t_{17}	5	ns min	Input data hold time

[1] Sample tested at initial release to ensure compliance. All input signals are measured with tr = tf = 1 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2] See Figure 9, Figure 10,and Figure 11.
[3] Refer to the Standby Mode Operation section. The maximum specification of 6 ms is valid when using a 0.1 µF decoupling capacitor on the V_{REF} pin.
[4] Measured with the load circuit of Figure 2 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[5] These times are derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part, and as such, are independent of external bus loading capacitances.

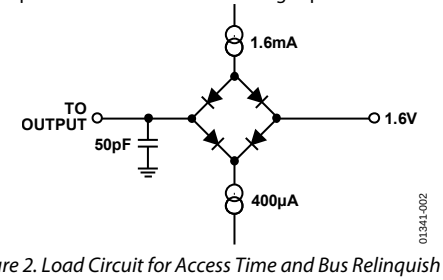


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
Analog Input Voltage to AGND	
AD7864-1 (±10 V Input Range)	±20 V
AD7864-1 (±5 V Input Range)	−7 V to +20 V
AD7864-3	−7 V to +20 V
AD7864-2	−1 V to +20 V
Reference Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
V_{DRIVE} to AGND	−0.3 V to AV_{DD} + 0.3 V
V_{DRIVE} to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Commercial (A and B Versions)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MQFP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

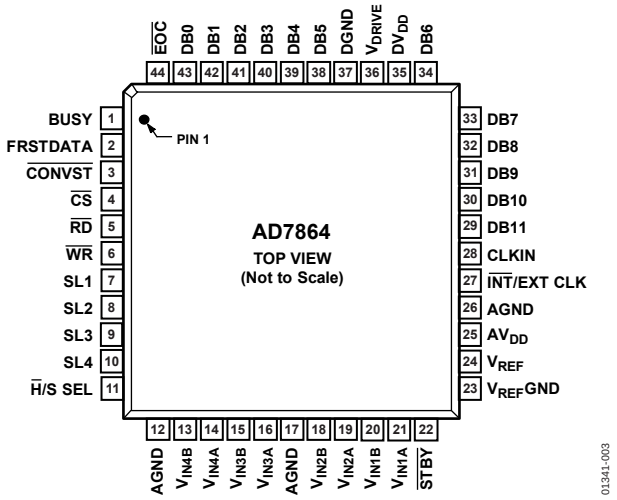


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BUSY	Busy Output. The busy output is triggered high by the rising edge of $\overline{\text{CONVST}}$ and remains high until conversion is completed on all selected channels.
2	FRSTDATA	First Data Output. FRSTDATA is a logic output which, when high, indicates that the output data register pointer is addressing Register 1—see the Accessing the Output Data Registers section.
3	$\overline{\text{CONVST}}$	Convert Start Input. Logic input. A low-to-high transition on this input puts all track-and-holds into their hold mode and starts conversion on the selected channels. In addition, the state of the channel sequence selection is also latched on the rising edge of $\overline{\text{CONVST}}$.
4	$\overline{\text{CS}}$	Chip Select Input. Active low logic input. The device is selected when this input is active.
5	$\overline{\text{RD}}$	Read Input. Active low logic input that is used in conjunction with $\overline{\text{CS}}$ low to enable the data outputs. Ensure the $\overline{\text{WR}}$ pin is at logic high while performing a read operation.
6	$\overline{\text{WR}}$	Write Input. A rising edge on the $\overline{\text{WR}}$ input, with $\overline{\text{CS}}$ low and $\overline{\text{RD}}$ high, latches the logic state on DB0 to DB3 into the channel select register.
7 to 10	SL1 to SL4	Hardware Channel Select. Conversion sequence selection can also be made via the SL1 to SL4 pins if $\overline{\text{H}}$/S SEL is Logic 0. The selection is latched on the rising edge of $\overline{\text{CONVST}}$. See the Selecting a Conversion Sequence section.
11	$\overline{\text{H}}$/S SEL	Hardware/Software Select Input. When this pin is at Logic 0, the AD7864 conversion sequence selection is controlled via the SL1 to SL4 input pins. When this pin is at Logic 1, the sequence is controlled via the channel select register. See the Selecting a Conversion Sequence section.
12	AGND	Analog Ground. General analog ground. Connect this AGND pin to the AGND plane of the system.
13 to 16	V_{IN4x}, V_{IN3x}	Analog Inputs. See the Analog Input section.
17	AGND	Analog Ground. Analog ground reference for the attenuator circuitry. Connect this AGND pin to the AGND plane of the system.
18 to 21	V_{IN2x}, V_{IN1x}	Analog Inputs. See the Analog Input section.
22	$\overline{\text{STBY}}$	Standby Mode Input. TTL-compatible input that is used to put the device into the power save or standby mode. The $\overline{\text{STBY}}$ input is high for normal operation and low for standby operation.
23	V_{REF}GND	Reference Ground. This is the ground reference for the on-chip reference buffer of the part. Connect the V_{REF}GND pin to the AGND plane of the system.
24	V_{REF}	Reference Input/Output. This pin provides access to the internal reference (2.5 V ± 5%) and also allows the internal reference to be overdriven by an external reference source (2.5 V). Connect a 0.1 µF decoupling capacitor between this pin and AGND.
25	AV_{DD}	Analog Positive Supply Voltage, 5.0 V ± 5%.
26	AGND	Analog Ground. Analog ground reference for the DAC circuitry.

Pin No.	Mnemonic	Description
27	$\overline{\text{INT}}$/EXT CLK	Internal/External Clock Select Input. When this pin is at Logic 0, the AD7864 uses its internally generated master clock. When this pin is at Logic 1, the master clock is generated externally to the device.
28	CLKIN	Conversion Clock Input. This is an externally applied clock that allows the user to control the conversion rate of the AD7864. Each conversion needs 14 clock cycles for the conversion to be completed and an $\overline{\text{EOC}}$ pulse to be generated. The clock should have a duty cycle that is no worse than 60/40. See the Using An External Clock section.
29 to 34	DB11 to DB6	Data Bit 11 is the MSB, followed by Data Bit 10 to Data Bit 6. Three-state TTL outputs. Output coding is twos complement for the AD7864-1 and AD7864-3. Output coding is straight (natural) binary for the AD7864-2.
35	DV_{DD}	Positive Supply Voltage for Digital Section, 5.0 V ± 5%. Connect a 0.1 µF decoupling capacitor between this pin and AGND. Both DV_{DD} and AV_{DD} should be externally tied together.
36	V_{DRIVE}	This pin provides the positive supply voltage for the output drivers (DB0 to DB11), BUSY, $\overline{\text{EOC}}$, and FRSTDATA. It is normally tied to DV_{DD}. Decouple V_{DRIVE} with a 0.1 µF capacitor to improve performance when reading during the conversion sequence. To facilitate interfacing to 3 V processors and DSPs, the output data drivers can also be powered by a 3 V ± 10% supply.
37	DGND	Digital Ground. This is the ground reference for digital circuitry. Connect this DGND pin to the AGND plane of the system at the AGND pin.
38, 39	DB5, DB4	Data Bit 5 to Data Bit 4. Three-state TTL outputs.
40 to 43	DB3 to DB0	Data Bit 3 to Data Bit 0. Bidirectional data pins. When a read operation takes place, these pins are three-state TTL outputs. The channel select register is programmed with the data on the DB0 to DB3 pins with standard $\overline{\text{CS}}$ and $\overline{\text{WR}}$ signals. DB0 represents Channel 1, and DB3 represents Channel 4.
44	$\overline{\text{EOC}}$	End-of-Conversion. Active low logic output indicating conversion status. The end of each conversion in a conversion sequence is indicated by a low-going pulse on this line.

TERMINOLOGY

Signal-to-(Noise + Distortion) Ratio
This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio depends on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Signal-to-(Noise + Distortion) = (6.02 *N* + 1.76) dB

Thus, for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7864, it is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the fifth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation terms are those for which neither m nor n are equal to zero. For example, second-order terms include (fa + fb) and (fa − fb), whereas third-order terms include (2 fa + fb), (2 fa − fb), (fa + 2 fb), and (fa − 2 fb).

The AD7864 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second- and third-order terms are of different significance. The second-order terms are usually distanced in frequency from the original sine waves, whereas the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in decibels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale 50 kHz sine wave signal to all nonselected input channels and determining how much that signal is attenuated in the selected channel. The figure given is the worst case across all four channels.

Relative Accuracy
Relative accuracy, or endpoint nonlinearity, is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Positive Full-Scale Error
This is the deviation of the last code transition (01...110 to 01...111) from the ideal, 4 × V_{REF} − 3/2 LSB (AD7864-1, ±10 V), or 2 × V_{REF} − 3/2 LSB (AD7864-1, ±5 V range), or V_{REF} − 3/2 LSB (AD7864-3, ±2.5 V range), after the bipolar offset error has been adjusted out.

Positive Full-Scale Error (AD7864-2, 0 V to 2.5 V and 0 V to 5 V)
This is the deviation of the last code transition (11...110 to 11...111) from the ideal 2 × V_{REF} − 3/2 LSB (AD7864-2, 0 V to 5 V range) or V_{REF} − 3/2 LSB (AD7864-2, 0 V to 2.5 V range), after the unipolar offset error has been adjusted out.

Bipolar Zero Error (AD7864-1, ±10 V/±5 V, AD7864-3, ±2.5 V)
This is the deviation of the midscale transition (all 0s to all 1s) from the ideal, AGND − 1/2 LSB.

Unipolar Offset Error (AD7864-2, 0 V to 2.5 V and 0 V to 5 V)
This is the deviation of the first code transition (00...000 to 00...001) from the ideal, AGND + 1/2 LSB.

Negative Full-Scale Error (AD7864-1, ±10 V/±5 V, and AD7864-3, ±2.5 V)
This is the deviation of the first code transition (10...000 to 10...001) from the ideal, −4 × V_{REF} + 1/2 LSB (AD7864-1, ±10 V), −2 × V_{REF} + 1/2 LSB (AD7864-1, ±5 V range) or −V_{REF} + 1/2 LSB (AD7864-3, ±2.5 V range), after bipolar zero error has been adjusted out.

Track-and-Hold Acquisition Time
Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1/2 LSB, after the end of a conversion (the point at which the track-and-hold returns to track mode). It also applies to situations where there is a step input change on the input voltage applied to the selected V_{INxA}/V_{INxB} input of the AD7864.

It means that the user must wait for the duration of the track-and-hold acquisition time after the end of conversion or after a step input change to V_{INxA}/V_{INxB} before starting another conversion to ensure that the part operates to specification.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7864 is a high speed, low power, 4-channel simultaneous sampling 12-bit ADC that operates from a single 5 V supply. The part contains a 1.65 µs successive approximation ADC, four track-and-hold amplifiers, an internal 2.5 V reference, and a high speed parallel interface. There are four analog inputs that can be simultaneously sampled, thus preserving the relative phase information of the signals on all four analog inputs. Thereafter, conversions are completed on the selected subset of the four channels. The part accepts an analog input range of ±10 V or ±5 V (AD7864-1), ±2.5 V (AD7864-3), and 0 V to +2.5 V or 0 V to +5 V (AD7864-2). Overvoltage protection on the analog inputs of the part allows the input voltage to go to ±20 V, (AD7864-1 ±10 V range), −7 V or +20 V (AD7864-1 ±5 V range), −1 V to +20 V (AD7864-2), and −7 V to +20 V (AD7864-3), without causing damage. The AD7864 has two operating modes: reading-between-conversions and reading-after-the-conversion sequence. These modes are discussed in more detail in the Timing and Control section.

A conversion is initiated on the AD7864 by pulsing the $\overline{\text{CONVST}}$ input. On the rising edge of $\overline{\text{CONVST}}$, all four on-chip track-and-holds are placed into hold simultaneously and the conversion sequence is started on all the selected channels. Channel selection is made via the SL1 to SL4 pins if $\overline{\text{H}}$/S SEL is Logic 0 or via the channel select register if $\overline{\text{H}}$/S SEL is Logic 1—see the Selecting a Conversion Sequence section. The channel select register is programmed via the bidirectional data lines (DB0 to DB3) and a standard write operation. The selected conversion sequence is latched on the rising edge of $\overline{\text{CONVST}}$, therefore, changing a selection only takes effect once a new conversion sequence is initiated. The $\overline{\text{BUSY}}$ output signal is triggered high on the rising edge of $\overline{\text{CONVST}}$ and remains high for the duration of the conversion sequence. The conversion clock for the part is generated internally using a laser trimmed, clock oscillator circuit.

There is also the option of using an external clock, by tying the $\overline{\text{INT}}$/EXT CLK pin logic high, and applying an external clock to the CLKIN pin. However, the optimum throughput is obtained by using the internally generated clock—see the Using an External Clock section. The $\overline{\text{EOC}}$ signal indicates the end of each conversion in the conversion sequence. The BUSY signal indicates the end of the full conversion sequence, and at this time, all four track and holds return to tracking mode. The conversion results can be read either at the end of the full conversion sequence (indicated by $\overline{\text{BUSY}}$ going low), or as each result becomes available (indicated by $\overline{\text{EOC}}$ going low). Data is read from the part via a 12-bit parallel data bus with standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals—see the Timing and Control section.

Conversion time for each channel of the AD7864 is 1.65 µs, and the track-and-hold acquisition time is 0.35 µs. To obtain optimum performance from the part, the read operation should not occur during a channel conversion or during the 100 ns prior to the next $\overline{\text{CONVST}}$ rising edge. This allows the part to operate at throughput rates up to 130 kHz for all four channels and achieve data sheet specifications.

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7864 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the track-and-hold is greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate of 500 kSPS (that is, the track-and-hold can handle input frequencies in excess of 250 kHz).

The track-and-hold amplifiers acquire input signals to 12-bit accuracy in less than 350 ns. The operation of the track-and-holds are essentially transparent to the user. The four track-and-hold amplifiers sample their respective input channels simultaneously, on the rising edge of $\overline{\text{CONVST}}$. The aperture time for the track-and-holds (that is, the delay time between the external $\overline{\text{CONVST}}$ signal and the track-and-hold actually going into hold) is typically 15 ns and, more importantly, is well matched across the four track-and-holds on one device as well as being well matched from device to device. This allows the relative phase information between different input channels to be accurately preserved. It also allows multiple AD7864s to sample more than four channels simultaneously. At the end of a conversion sequence, the part returns to its tracking mode. The acquisition time of the track-and-hold amplifiers begin at this point.

Reference

The AD7864 contains a single reference pin, labeled V_{REF}. The V_{REF} pin provides access to the 2.5 V reference within the part, or it serves as the reference source for the part by connecting V_{REF} to an external 2.5 V reference. The part is specified with a 2.5 V reference voltage. Errors in the reference source result in gain errors in the transfer function of the AD7864 and adds to the specified full-scale errors on the part. On the AD7864-1 and AD7864-3, it also results in an offset error injected in the attenuator stage; see Figure 4 and Figure 6.

The AD7864 contains an on-chip 2.5 V reference. To use this reference as the reference source for the AD7864, simply connect a 0.1 µF disk ceramic capacitor from the V_{REF} pin to AGND. The voltage that appears at this pin is internally buffered before being applied to the ADC. If this reference is used externally to the AD7864, it should be buffered because the part has a FET switch in series with the reference output resulting in a 6 kΩ

nominal source impedance for this output. The tolerance on the internal reference is ±10 mV at 25°C with a typical temperature coefficient of 25 ppm/°C and a maximum error overtemperature of ±20 mV.

If the application requires a reference with a tighter tolerance or the AD7864 needs to be used with a system reference, the user has the option of connecting an external reference to this V_{REF} pin. The external reference effectively overdrives the internal reference and thus provides the reference source for the ADC. The reference input is buffered before being applied to the ADC with the maximum input current of ±100 μA. Suitable reference sources for the AD7864 include the AD680, AD780, REF192, and REF43 precision 2.5 V references.

CIRCUIT DESCRIPTION

ANALOG INPUT

The AD7864 is offered in three models: the AD7864-1, where each input can be configured for ±10 V or a ±5 V input voltage range; the AD7864-3, which handles the input voltage range of ±2.5 V; and the AD7864-2, where each input can be configured to have a 0 V to +2.5 V or 0 V to +5 V input voltage range.

AD7864-1

Figure 4 shows the analog input section of the AD7864-1. Each input can be configured for ±5 V or ±10 V operation on the AD7864-1. For ±5 V (AD7864-1) operation, the V_{INxA} and V_{INxB} inputs are tied together and the input voltage is applied to both. For ±10 V (AD7864-1) operation, the V_{INxB} input is tied to AGND and the input voltage is applied to the V_{INxA} input. The V_{INxA} and V_{INxB} inputs are symmetrical and fully interchangeable. Thus for ease of printed circuit board (PCB) layout on the ±10 V range, the input voltage may be applied to the V_{INxB} input while the V_{INxA} input is tied to AGND.

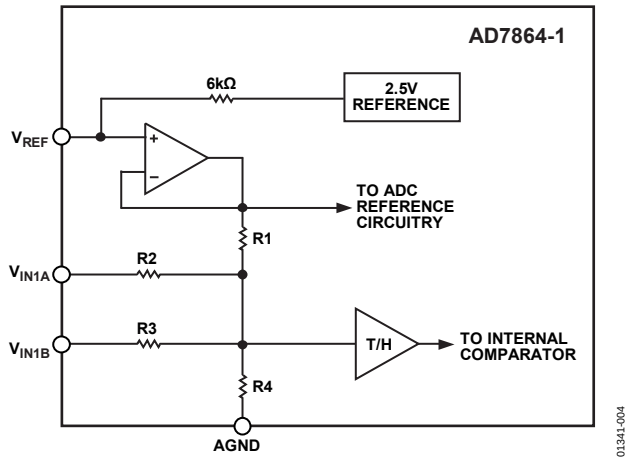


Figure 4. AD7864-1 Analog Input Structure

For the AD7864-1, R1 = 6 kΩ, R2 = 24 kΩ, R3 = 24 kΩ, and R4 = 12 kΩ. The resistor input stage is followed by the high input impedance stage of the track-and-hold amplifier.

The designed code transitions take place midway between successive integer least significant bit values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, and so forth). Least significant bit size is given by the formula 1 LSB = FSR/4096. For the ±5 V range, 1 LSB = 10 V/4096 = 2.44 mV. For the ±10 V range, 1 LSB = 20 V/4096 = 4.88 mV. Output coding is twos complement binary with 1 LSB = FSR/4096. The ideal input/output transfer function for the AD7864-1 is shown in Table 5.

Table 5. Ideal Input/Output Code Table for the AD7864-1

Analog Input[1]	Digital Output Code Transition
+FSR/2 − 3/2 LSB[2]	011...110 to 011...111
+FSR/2 − 5/2 LSB	011...101 to 011...110
+FSR/2 − 7/2 LSB	011...100 to 011...101
AGND + 3/2 LSB	000...001 to 000...010
AGND + 1/2 LSB	000...000 to 000...001
AGND − 1/2 LSB	111...111 to 000...000
AGND − 3/2 LSB	111...110 to 111...111
−FSR/2 + 5/2 LSB	100...010 to 100...011
−FSR/2 + 3/2 LSB	100...001 to 100...010
−FSR/2 + 1/2 LSB	100...000 to 100...001

[1] FSR is full-scale range and is 20 V for the ±10 V range and +10 V for the ±5 V range, with V_{REF} = 2.5 V.
[2] 1 LSB = FSR/4096 = 4.883 mV (±10 V for the AD7864-1) and 2.441 mV (±5 V for the AD7864-1) with V_{REF} = 2.5 V.

AD7864-2

Figure 5 shows the analog input section of the AD7864-2. Each input can be configured for 0 V to 5 V operation or 0 V to 2.5 V operation. For 0 V to 5 V operation, the V_{INxB} input is tied to AGND and the input voltage is applied to the V_{INxA} input. For 0 V to 2.5 V operation, the V_{INxA} and V_{INxB} inputs are tied together and the input voltage is applied to both. The V_{INxA} and V_{INxB} inputs are symmetrical and fully interchangeable. Thus for ease of PCB layout on the 0 V to 5 V range, the input voltage may be applied to the V_{INxB} input while the V_{INxA} input is tied to AGND.

For the AD7864-2, R1 = 6 kΩ and R2 = 6 kΩ. The designed code transitions occur on successive integer least significant bit values. Output coding is straight (natural) binary with 1 LSB = FSR/4096 = 2.5 V/4096 = 0.61 mV, and 5 V/4096 = 1.22 mV, for the 0 V to 2.5 V and 0 V to 5 V options, respectively.

Table 6 shows the ideal input and output transfer function for the AD7864-2.

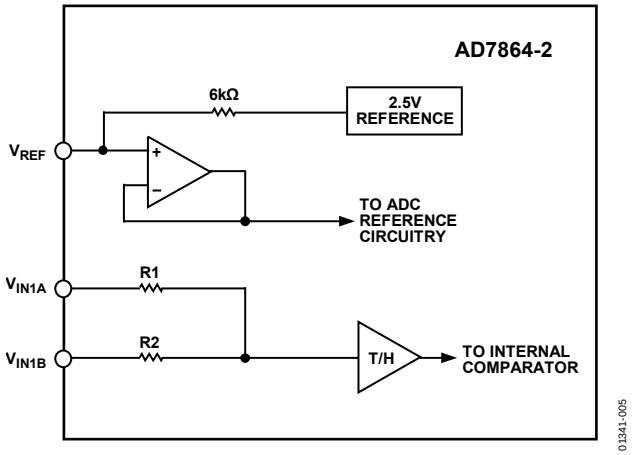


Figure 5. AD7864-2 Analog Input Structure

Table 6. Ideal Input/Output Code Table for the AD7864-2

Analog Input[1]	Digital Output Code Transition
+FSR – 3/2 LSB[2]	111...110 to 111...111
+FSR – 5/2 LSB	111...101 to 111...110
+FSR – 7/2 LSB	111...100 to 111...101
AGND + 5/2 LSB	000...010 to 000...011
AGND + 3/2 LSB	000...001 to 000...010
AGND + 1/2 LSB	000...000 to 000...001

[1] FSR is the full-scale range and is 0 V to 2.5 V and 0 V to 5 V for the AD7864-2 with V_{REF} = 2.5 V.
[2] 1 LSB = FSR/4096 and is 0.61 mV (0 V to 2.5 V) and 1.22 mV (0 V to 5 V) for the AD7864-2 with V_{REF} = 2.5 V.

AD7864-3

Figure 6 shows the analog input section of the AD7864-3. The analog input range is ±2.5 V on the V_{IN1A} input. The V_{IN1B} input can be left unconnected, but if it is connected to a potential, that potential must be AGND.

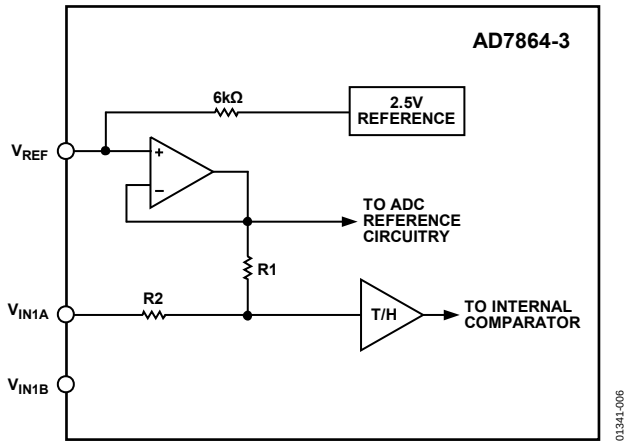


Figure 6. AD7864-3 Analog Input Structure

For the AD7864-3, R1 = 6 kΩ and R2 = 6 kΩ. As a result, drive the V_{IN1A} input from a low impedance source. The resistor input stage is followed by the high input impedance stage of the track-and-hold amplifier.

The designed code transitions take place midway between successive integer least significant bit values (that is, 1/2 LSB, 3/2 LSB, 5/2 LSB, and so on). Least significant bit size is given by the formula 1 LSB = FSR/4096. Output coding is twos complement binary with 1 LSB = FSR/4096 = 5 V/4096 = 1.22 mV. The ideal input/ output transfer function for the AD7864-3 is shown in Table 7.

Table 7. Ideal Input/Output Code Table for the AD7864-3

Analog Input[1]	Digital Output Code Transition
+FSR/2 – 3/2 LSB[2]	011...110 to 011...111
+FSR/2 – 5/2 LSB	011...101 to 011...110
+FSR/2 – 7/2 LSB	011...100 to 011...101
AGND + 3/2 LSB	000...001 to 000...010
AGND + 1/2 LSB	000...000 to 000...001
AGND – 1/2 LSB	111...111 to 000...000
AGND – 3/2 LSB	111...110 to 111...111
–FSR/2 + 5/2 LSB	100...010 to 100...011
–FSR/2 + 3/2 LSB	100...001 to 100...010
–FSR/2 + 1/2 LSB	100...000 to 100...001

[1] FSR is the full-scale range and is 5 V, with V_{REF} = 2.5 V.
[2] 1 LSB = FSR/4096 = 1.22 mV (±2.5 V – AD7864-3) with V_{REF} = 2.5 V.

SELECTING A CONVERSION SEQUENCE

Any subset of the four channels, V_{IN1} to V_{IN4}, can be selected for conversion. The selected channels are converted in ascending order. For example, if the channel selection includes V_{IN4}, V_{IN1}, and V_{IN3}, the conversion sequence is V_{IN1}, V_{IN3}, and then V_{IN4}. The conversion sequence selection can be made either by using the hardware channel select input pins (SL1 through SL4) or by programming the channel select register. A logic high on a hardware channel select pin (or Logic 1 in the channel select register) when CONVST goes logic high marks the associated analog input channel for inclusion in the conversion sequence.

Figure 7 shows the arrangement used. The H/S SEL controls a multiplexer that selects the source of the conversion sequence information, that is, from the hardware channel select pins (SL1 to SL4) or from the channel selection register. When a conversion begins, the output from the multiplexer is latched until the end of the conversion sequence. The data bus bits, DB0 to DB3, (DB0 representing Channel 1 through DB3 representing Channel 4) are bidirectional and become inputs to the channel select register when RD is logic high and CS and WR are logic low. The logic state on DB0 to DB3 is latched into the channel select register when WR goes logic high.

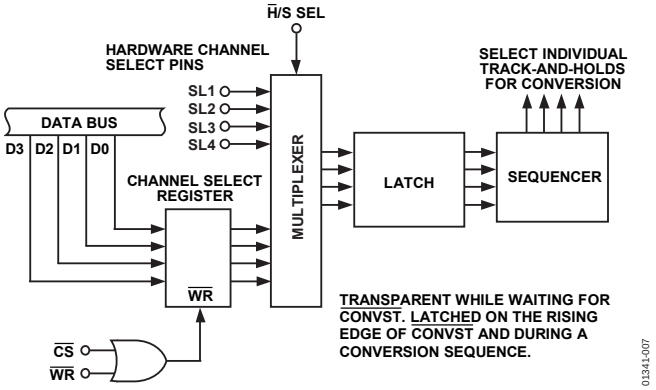


Figure 7. Channel Select Inputs and Registers

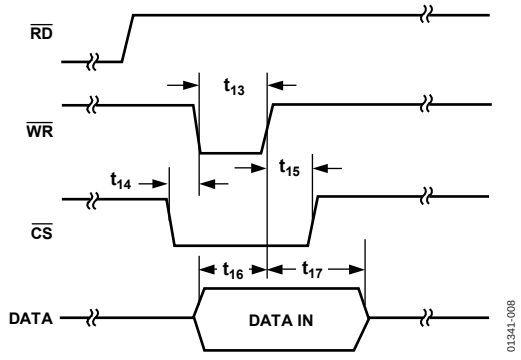


Figure 8. Channel Selection via Software Control

TIMING AND CONTROL

Reading Between Each Conversion in the Conversion Sequence

Figure 9 shows the timing and control sequence required to obtain the optimum throughput rate from the AD7864. To obtain the optimum throughput from the AD7864, the user must read the result of each conversion as it becomes available. The timing diagram in Figure 9 shows a read operation each time the EOC signal goes logic low. The timing in Figure 9 shows a conversion on all four analog channels (SL1 to SL4 = 1, see the Selecting a Conversion Sequence section), thus there are four EOC pulses and four read operations to access the result of each of the four conversions.

A conversion is initiated on the rising edge of CONVST. This places all four track-and-holds into hold simultaneously. New data from this conversion sequence is available for the first channel selected (V_{IN1}) 1.65 µs later. The conversion on each subsequent channel is completed at 1.65 µs intervals. The end of each conversion is indicated by the falling edge of the EOC signal. The BUSY output signal indicates the end-of-conversion for all selected channels (four in this case).

Data is read from the part via a 12-bit parallel data bus with standard CS and RD signals. The CS and RD inputs are internally gated to enable the conversion result onto the data bus. The data lines (DB0 to DB11) leave their high impedance state when both CS and RD are logic low. Therefore, CS can be permanently tied logic low and the RD signal used to access the conversion result. Because each conversion result is latched into its output data register prior to EOC going logic low, another option is to tie the EOC and RD pins together and use the rising edge of EOC to latch the conversion result. Although the AD7864 has some special features that permit reading during a conversion (such as a separate supply for the output data drivers, V_{DRIVE}) for optimum performance it is recommended that the read operation be completed when EOC is logic low, that is, before the start of the next conversion. Although Figure 10 shows the read operation occurring during the EOC pulse, a read operation can occur at any time. Figure 10 shows a timing specification referred to as the quiet time. Quiet time is the amount of time that should be left after a read operation and before the next conversion is initiated. The quiet time depends heavily on data bus capacitance, but 50 ns to 100 ns is typical.

The signal labeled FRSTDATA (first data-word) indicates to the user that the pointer associated with the output data registers is pointing to the first conversion result by going logic high. The pointer is reset to point to the first data location (that is, the first conversion result,) at the end of the first conversion (FRSTDATA

logic high). The pointer is incremented to point to the next register (next conversion result) when that conversion result is available. Thus, FRSTDATA in Figure 9 is shown as going low just prior to the second $\overline{EOC}$ pulse. Repeated read operations during a conversion continue to access the data at the current pointer location until the pointer is incremented at the end of that conversion. Note that FRSTDATA has an indeterminate logic state after initial power-up. This means that for the first conversion sequence after power-up, the FRSTDATA logic output may already be logic high before the end of the first conversion (this condition is indicated by the dashed line in Figure 9). Also, the FRSTDATA logic output may already be high as a result of the previous read sequence, as is the case after the fourth read in Figure 9. The fourth read (rising edge of $\overline{RD}$) resets the pointer to the first data location. Therefore, FRSTDATA is already high when the next conversion sequence initiates. See the Accessing the Output Data Registers section.

Reading After the Conversion Sequence

Figure 10 shows the same conversion sequence as Figure 9. In this case, however, the results of the four conversions (on V_{IN1} to V_{IN4}) are read after all conversions have finished, that is, when BUSY goes logic low. The FRSTDATA signal goes logic high at the end of the first conversion just prior to $\overline{EOC}$ going logic low. As mentioned previously, FRSTDATA has an indeterminate state after initial power-up, therefore FRSTDATA may already be logic high. Unlike the case when reading between each conversion, the output data register pointer is incremented on the rising edge of $\overline{RD}$ because the next conversion result is available. This means FRSTDATA goes logic low after the first rising edge on $\overline{RD}$.

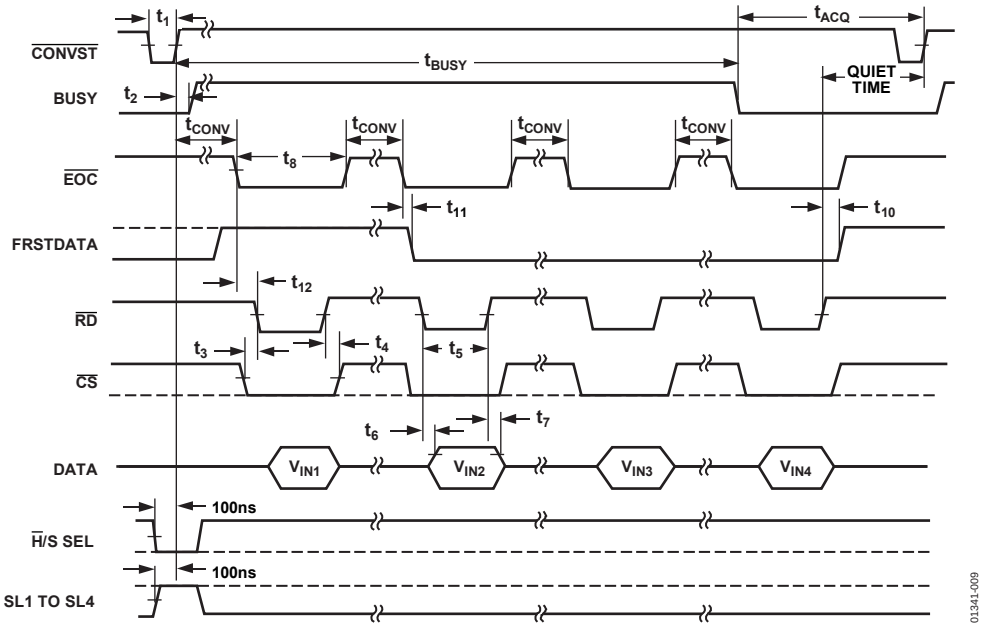


Figure 9. Timing Diagram for Reading During Conversion

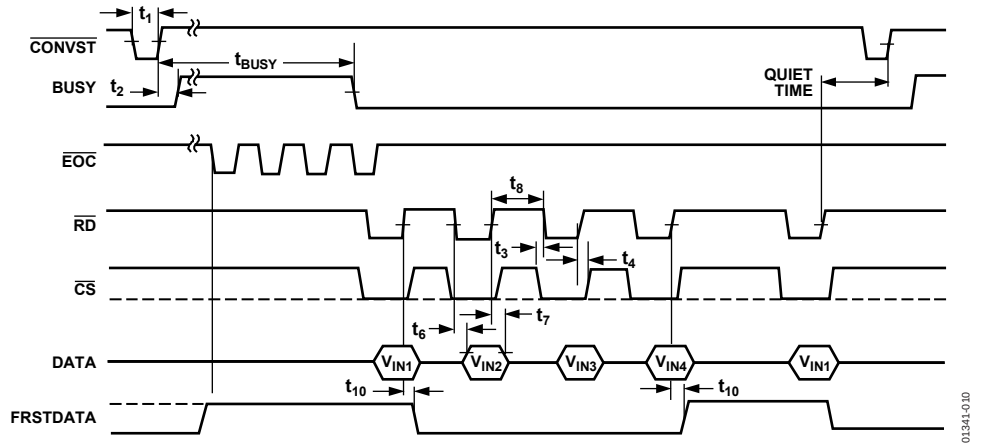


Figure 10. Timing Diagram, Reading After the Conversion Sequence

Successive read operations access the remaining conversion results in an ascending channel order. Each read operation increments the output data register pointer. The read operation that accesses the last conversion result causes the output data register pointer to be reset so that the next read operation accesses the first conversion result again. This is shown in Figure 10, wherein the fifth read after BUSY goes low accessing the result of the conversion on V_{IN1}. Thus, the output data registers act as a circular buffer in which the conversion results are continually accessible. The FRSTDATA signal goes high when the first conversion result is available.

Data is enabled onto the data bus (DB0 to DB11) using $\overline{CS}$ and $\overline{RD}$. Both $\overline{CS}$ and $\overline{RD}$ have the same functionality as described in the previous section. There are no restrictions or performance implications associated with the position of the read operations after BUSY goes low. The only restriction is that there is minimum time between read operations. Notice that the quiet time must be allowed before the start of the next conversion.

USING AN EXTERNAL CLOCK

The logic input $\overline{INT}$/EXT CLK allows the user to operate the AD7864 using the internal clock oscillator or an external clock. To achieve optimum performance on the AD7864, use the internal clock. The highest external clock frequency allowed is 5 MHz. This means a conversion time of 2.6 µs compared to 1.65 µs when using the internal clock. In some instances, however, it may be useful to use an external clock when high throughput rates are not required. For example, two or more AD7864s can be synchronized by using the same external clock for all devices. In this way, there is no latency between output logic signals like $\overline{EOC}$ due to differences in the frequency of the internal clock oscillators. Figure 11 shows how the various logic outputs are synchronized to the CLK signal. Each conversion requires 14 clocks. The output data register pointer is reset to point to the first register location on the falling edge of the 12th clock cycle of the first conversion in the conversion sequence—see the Accessing the Output Data Registers section. At this point, the logic output FRSTDATA goes logic high. The result of the first conversion transfers to the output data registers on the falling edge of the 13th clock cycle. The FRSTDATA signal is reset on the falling edge of the 13th clock cycle of the next conversion, that is, when the result of the second conversion is transferred to its output data register. As mentioned previously, the pointer is incremented by the rising edge of the $\overline{RD}$ signal if the result of the next conversion is available. The $\overline{EOC}$ signal goes logic low on the falling edge of the 13th clock cycle and is reset high again on the falling edge of the 14th clock cycle.

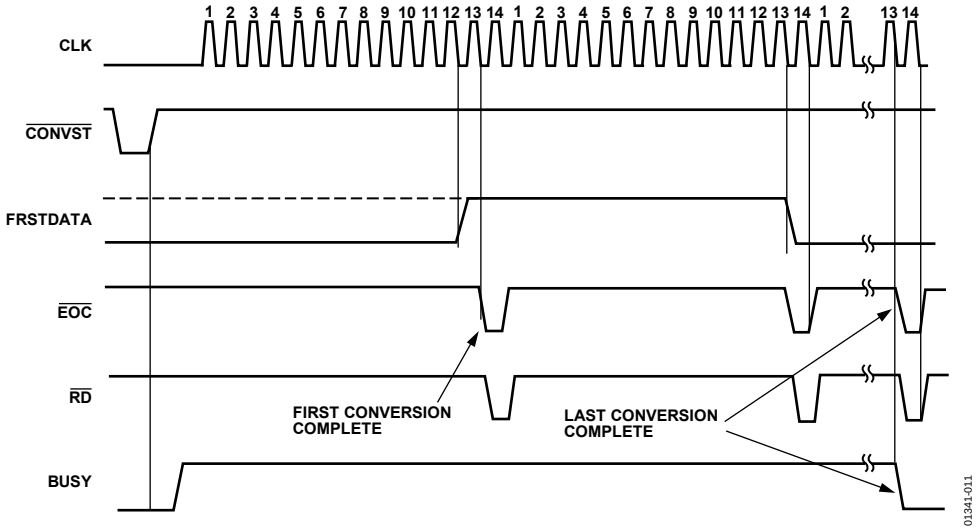


Figure 11. Using an External Clock

STANDBY MODE OPERATION

The AD7864 has a standby mode whereby the device can be placed in a low current consumption mode (5 μA typical). The AD7864 is placed in standby by bringing the Logic Input $\overline{STBY}$ low. The AD7864 can be powered up again for normal operation by bringing $\overline{STBY}$ logic high. The output data buffers remain operational while the AD7864 is in standby. This means the user can continue to access the conversion results while the AD7864 is in standby. This feature can be used to reduce the average power consumption in a system using low throughput rates. To reduce average power consumption, the AD7864 can be placed in standby at the end of each conversion sequence, that is, when BUSY goes low and is taken out of standby again prior to the start of the next conversion sequence. The time it takes the AD7864 to come out of standby is referred to as the wake-up time. The wake-up time limits the maximum throughput rate at which the AD7864 can be operated when powering down between conversion sequences. The AD7864 wakes up in approximately 2 μs when using an external reference. The wake-up time is also 2 μs when the standby time is less than 1 ms while using the internal reference. Figure 12 shows the wake-up time of the AD7864 for standby times greater than 1 ms. Note that when the AD7864 is left in standby for periods of time greater than 1 ms, the part requires more than 2 μs to wake up. For example, after initial power-up using the internal reference, the AD7864 requires 6 ms to power up. The maximum throughput rate that can be achieved when powering down between conversions is $1/(t_{BUSY} + 2\ \mu s)$ = 100 kSPS, approximately. When operating the AD7864 in a standby mode between conversions, the power savings can be significant. For example, with a throughput rate of 10 kSPS, the AD7864 is powered down (I_{DD} = 5 μA) for 90 μs out of every 100 μs (see Figure 13).

Therefore, the average power consumption drops to 125/10 mW or 12.5 mW approximately.

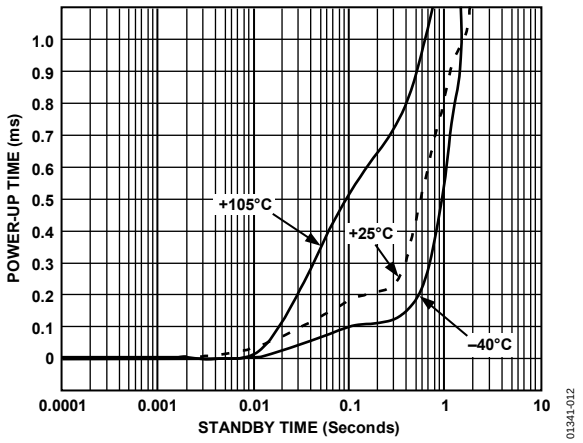


Figure 12. Power-Up Time vs. Standby Time Using the On-Chip Reference (Decoupled with 0.1 μF Capacitor)

ACCESSING THE OUTPUT DATA REGISTERS

There are four output data registers, one for each of the four possible conversion results from a conversion sequence. The result of the first conversion in a conversion sequence is placed in Register 1, the second result is placed in Register 2, and so forth. For example, if the conversion sequence V_{IN1}, V_{IN3}, and V_{IN4} is selected (see the Selecting a Conversion Sequence section), the results of the conversion on V_{IN1}, V_{IN3}, and V_{IN4} are placed in Register 1 to Register 3, respectively. The output data register pointer is reset to point to Register 1 at the end of the first conversion in the sequence, immediately prior to $\overline{EOC}$ going low. At this point, the logic output, FRSTDATA, goes logic high to indicate that the output data register pointer is addressing Register 1. When $\overline{CS}$ and $\overline{RD}$ are both logic low, the contents of the addressed register are enabled onto the data bus (DB0 to DB11).

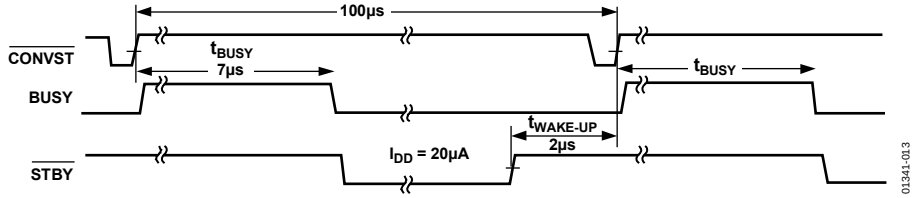


Figure 13. Power-Down Between Conversion Sequences

When reading the output data registers after a conversion sequence, that is, when BUSY goes low, the register pointer is incremented on the rising edge of the $\overline{RD}$ signal, as shown in Figure 14. However, when reading the conversion results during the conversion sequence, the pointer is not incremented until a valid conversion result is in the register to be addressed. In this case, the pointer is incremented when the conversion has ended and the result has been transferred to the output data register. This happens immediately before $\overline{EOC}$ goes low, therefore $\overline{EOC}$ may be used to enable the register contents onto the data bus, as described in the Reading Between Each Conversion in the Conversion Sequence subsection within the Selecting a Conversion Sequence section. The pointer is reset to point to Register 1 on the rising edge of the $\overline{RD}$ signal when the last conversion result in the sequence is being read. In the example shown, this means that the pointer is set to Register 1 when the contents of Register 3 are read.

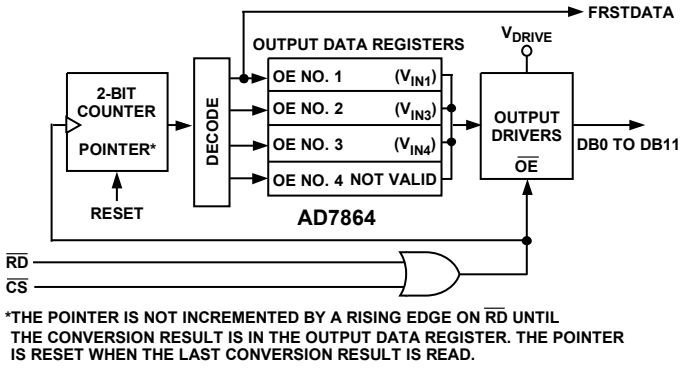


Figure 14. Output Data Registers

OFFSET AND FULL-SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Invariably, some applications require that the input signal spans the full analog input dynamic range. In such applications, offset and full-scale error have to be adjusted to zero.

Figure 15 shows a circuit that can be used to adjust the offset and full-scale errors on the AD7864 (V_{INxA} on the AD7864-1 version is shown for example purposes only). Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7864 while the input voltage is 1/2 LSB below analog ground. The trim procedure is as follows: apply a voltage of −2.44 mV (−1/2 LSB) at V_1 in Figure 15 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000.

Adjust gain error at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows.

POSITIVE FULL-SCALE ADJUST

Apply a voltage of 9.9927 V (FS − 3/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

NEGATIVE FULL-SCALE ADJUST

Apply a voltage of −9.9976 V (−FS + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

An alternative scheme for adjusting full-scale error in systems that use an external reference is to adjust the voltage at the V_{REF} pin until the full-scale error for any of the channels is adjusted out. Good full-scale matching of the channels ensures small full-scale errors on the other channels.

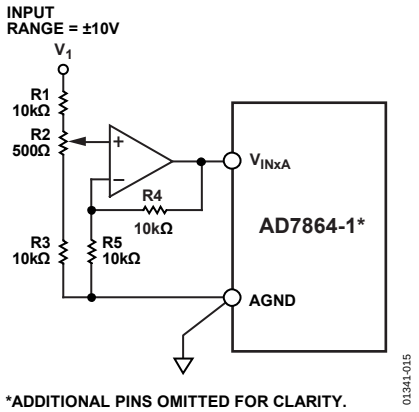


Figure 15. Full-Scale Adjust Circuit

DYNAMIC SPECIFICATIONS

The AD7864 is specified and 100% tested for dynamic performance specifications as well as traditional dc specifications, such as integral and differential nonlinearity. These ac specifications are required for signal processing applications such as phased array sonar, adaptive filters, and spectrum analysis. These applications require information on the effect of the ADC on the spectral content of the input signal. Thus, the parameters for which the AD7864 is specified include SNR, harmonic distortion, intermodulation distortion, and peak harmonics. These terms are discussed in more detail in the following sections.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half of the sampling frequency ($f_S/2$) excluding dc. SNR depends on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ \text{dB} \quad (1)$$

where N is the number of bits.

Thus, for an ideal 12-bit converter, SNR = 74 dB.

Figure 16 shows a histogram plot for 8192 conversions of a dc input using the AD7864 with a 5 V supply. The analog input was set at the center of a code. The figure shows that all the codes appear in the one output bin, indicating very good noise performance from the ADC.

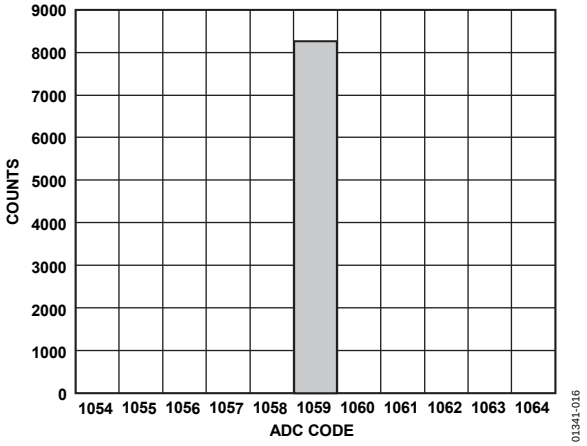


Figure 16. Histogram of 8192 Conversions of a DC Input

The output spectrum from the ADC is evaluated by applying a sine wave signal of very low distortion to the analog input. A fast fourier transform (FFT) plot is generated from which the SNR data can be obtained. Figure 17 shows a typical 4096 point FFT plot of the AD7864 with an input signal of 99.9 kHz and a sampling frequency of 500 kHz. The SNR obtained from this graph is 72.6 dB. Note that the harmonics are taken into account when calculating the SNR.

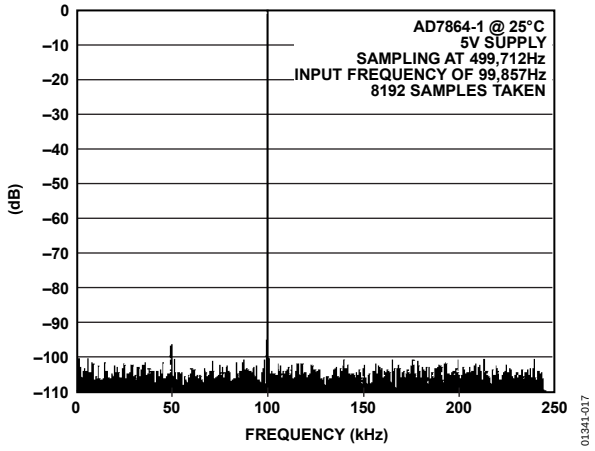


Figure 17. FFT Plot

EFFECTIVE NUMBER OF BITS

The formula given in Equation 1 relates the SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR. Figure 18 shows a typical plot of effective number of bits vs. frequency for an AD7864-2.

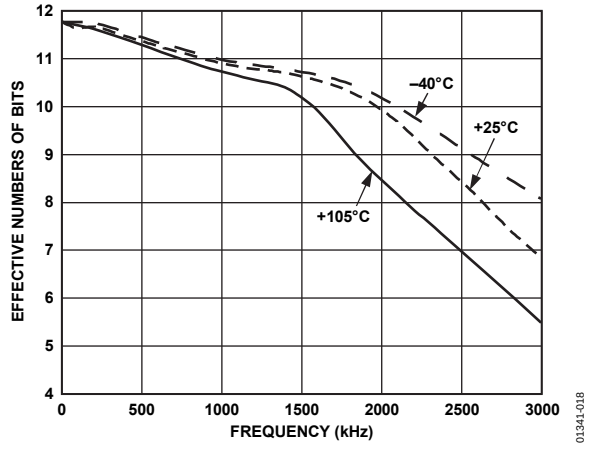


Figure 18. Effective Numbers of Bits vs. Frequency

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so forth. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second-order

terms include (fa + fb) and (fa − fb), whereas the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

Using the CCIF standard where two input frequencies near the top end of the input bandwidth are used, the second- and third-order terms are of different significance. The second-order terms are usually distanced in frequency from the original sine waves, whereas the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in decibels. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 19 shows a typical IMD plot for the AD7864.

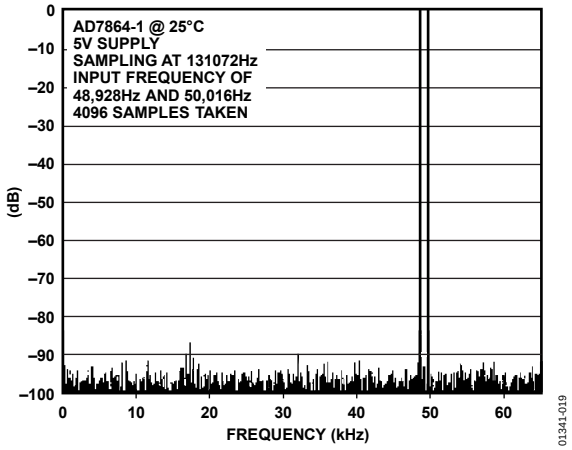


Figure 19. IMD Plot

AC LINEARITY PLOTS

The plots shown in Figure 20 and Figure 21 show typical DNL and INL plots for the AD7864.

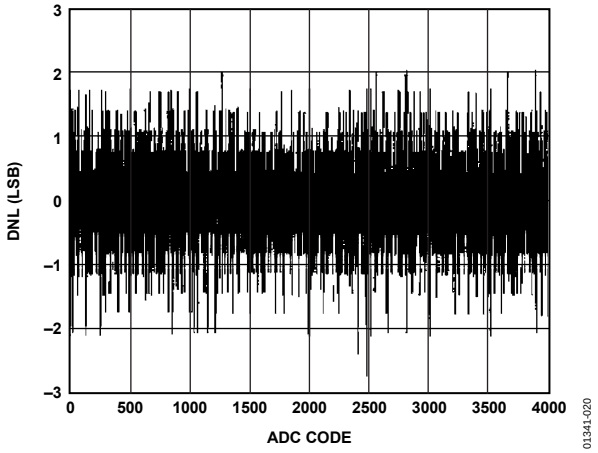


Figure 20. Typical DNL Plot

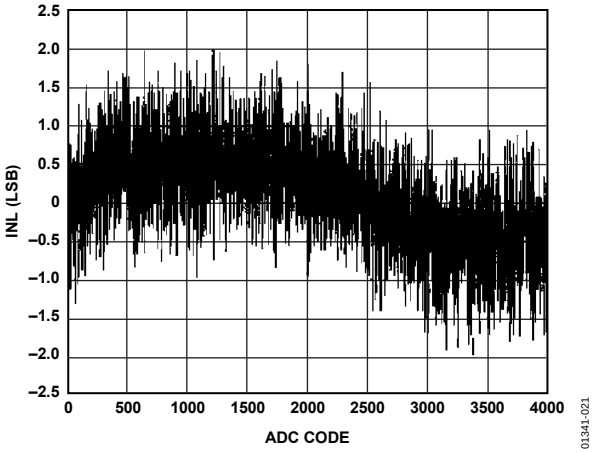


Figure 21. Typical INL Plot

MEASURING APERTURE JITTER

A convenient way to measure aperture jitter is to use the relationship it is known to have with SNR (signal-to-noise plus distortion) given as follows:

$$SNR_{JITTER} = 20 \times \log_{10}\left(\frac{1}{(2 \times \pi \times f_{IN} \times \sigma)}\right) \quad (3)$$

where:

SNR_{JITTER} is the signal-to-noise due to the rms time jitter.

σ is the rms time jitter.

f_{IN} is the sinusoidal input frequency (1 MHz in this case).

Equation 3 demonstrates that the signal-to-noise ratio due to jitter degrades significantly with frequency. At low input frequencies, the measured SNR performance of the AD7864 is indicative of noise performance due to quantization noise and system noise only (72 dB used as a typical figure in this example).

Therefore, by measuring the overall SNR performance (including noise due to jitter, system, and quantization) of the AD7864, a good estimation of the jitter performance of the AD7864 can be calculated.

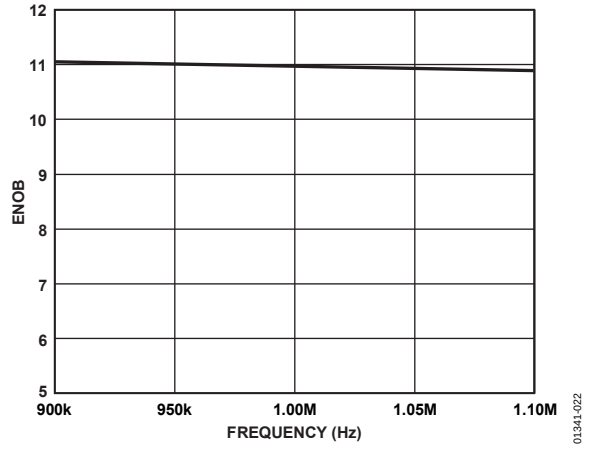


Figure 22. ENOB of the AD7864 at 1 MHz

From Figure 22, the ENOB of the AD7864 at 1 MHz is approximately 11 bits. This is equivalent to 68 dB SNR.

$SNR_{TOTAL} = SNR_{JITTER} + SNR_{QUANT} = 68$ dB

68 dB = SNR_{JITTER} + 72 dB (at 100 kHz)

$SNR_{JITTER} = 70.2$ dB

From Equation 3

$$70.2 \text{ dB} = 20 \times \log_{10}[1/(2 \times \pi \times 1 \text{ MHz} \times \sigma)]$$

$\sigma = 49$ ps

where σ is the rms jitter of the AD7864.

MICROPROCESSOR INTERFACING

The high speed parallel interface of the AD7864 allows easy interfacing to most DSPs and microprocessors. This interface consists of the data lines (DB0 to DB11), $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{EOC}$, and BUSY.

AD7864 TO ADSP-2100/ADSP-2101/ADSP-2102 INTERFACE

Figure 23 shows an interface between the AD7864 and the ADSP-210x. The $\overline{CONVST}$ signal can be generated by the ADSP-210x or from some other external source. Figure 23 shows the $\overline{CS}$ being generated by a combination of the $\overline{DMS}$ signal and the address bus of the ADSP-210x. In this way, the AD7864 is mapped into the data memory space of the ADSP-210x.

The AD7864 BUSY line provides an interrupt to the ADSP-210x when the conversion sequence is complete on all the selected channels. The conversion results can then be read from the AD7864 using successive read operations. Alternately, one can use the $\overline{EOC}$ pulse to interrupt the ADSP-210x when the conversion on each channel is complete when reading between each conversion in the conversion sequence (Figure 9). The AD7864 is read using the following instruction:

```
MR0 = DM(ADC)
```

where MR0 is the ADSP-210x MR0 register and ADC is the AD7864 address.

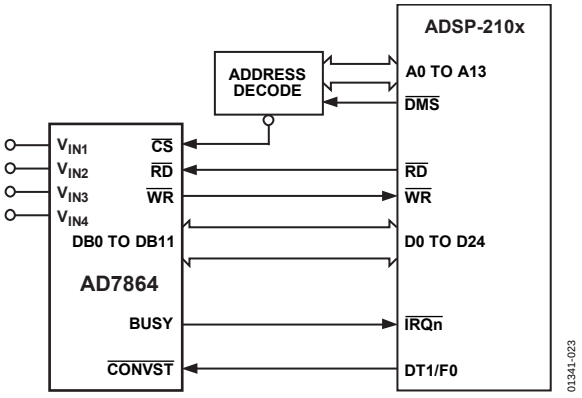


Figure 23. AD7864 to ADSP-210x Interface

AD7864 TO TMS320C5x INTERFACE

Figure 24 shows an interface between the AD7864 and the TMS320C5x. As with the previous interfaces, conversion can be initiated from the TMS320C5x or from an external source, and the processor is interrupted when the conversion sequence is completed. The $\overline{CS}$ signal to the AD7864 is derived from the $\overline{DS}$ signal and a decode of the address bus. This maps the AD7864 into external data memory. The $\overline{RD}$ signal from the TMS320C5x is used to enable the ADC data onto the data bus. The AD7864 has a fast parallel bus, consequently there are no wait state requirements. The following instruction is used to read the conversion results from the AD7864:

```
IN D,ADC
```

where D is the data memory address and ADC is the AD7864 address.

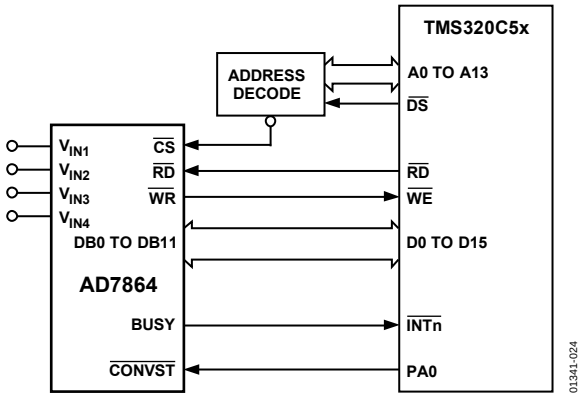


Figure 24. AD7864 to TMS320C5x Interface

AD7864 TO MC68HC000 INTERFACE

An interface between the AD7864 and the MC68HC000 is shown in Figure 25. The conversion can be initiated from the MC68HC000 or from an external source. The AD7864 BUSY line can be used to interrupt the processor or, alternatively, software delays can ensure that the conversion has been completed before a read to the AD7864 is attempted. Because of the nature of its interrupts, the MC68HC000 requires additional logic (not shown in Figure 25) to allow it to be interrupted correctly. For further information on MC68HC000 interrupts, consult the *Addendum to MC68000 Users Manual*.

The MC68HC000 $\overline{AS}$ and R/$\overline{W}$ outputs are used to generate a separate $\overline{RD}$ input signal for the AD7864. $\overline{RD}$ is used to drive the MC68HC000 $\overline{DTACK}$ input to allow the processor to execute a normal read operation to the AD7864. The conversion results are read using the following MC68HC000 instruction:

```
MOVE.W ADC,D0
```

where D0 is the MC68HC000 D0 register and ADC is the AD7864 address.

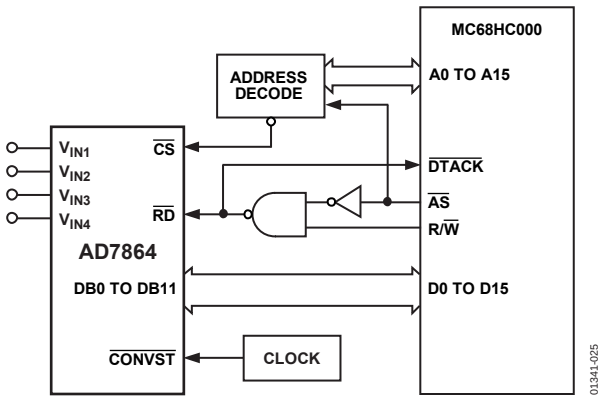


Figure 25. AD7864 to MC68HC000 Interface

VECTOR MOTOR CONTROL

The current drawn by a motor can be split into two components: one produces torque and the other produces magnetic flux. For optimal performance of the motor, control these two components independently. In conventional methods of controlling a three-phase motor, the current (or voltage) supplied to the motor and the frequency of the drive are the basic control variables. However, both the torque and flux are functions of current (or voltage) and frequency. This coupling effect can reduce the performance of the motor because, for example, if the torque is increased by increasing the frequency, the flux tends to decrease.

Vector control of an ac motor involves controlling phase in addition to drive and current frequency. Controlling the phase of the motor requires feedback information on the position of the rotor relative to the rotating magnetic field in the motor. Using this information, a vector controller mathematically transforms the three-phase drive currents into separate torque and flux components. The AD7864, with its 4-channel simultaneous sampling capability, is ideally suited for use in vector motor control applications.

A block diagram of a vector motor control application using the AD7864 is shown in Figure 26. The position of the field is derived by determining the current in each phase of the motor. Only two phase currents need to be measured because the third can be calculated if two phases are known. V_{IN1} and V_{IN2} of the AD7864 are used to digitize this information.

Simultaneous sampling is critical to maintain the relative phase information between the two channels. A current sensing isolation amplifier, transformer, or Hall effect sensor is used between the motor and the AD7864. Rotor information is obtained by measuring the voltage from two of the inputs to the motor. V_{IN3} and V_{IN4} of the AD7864 are used to obtain this information. Once again, the relative phase of the two channels is important. A DSP microprocessor is used to perform the mathematical transformations and control loop calculations on the information fed back by the AD7864.

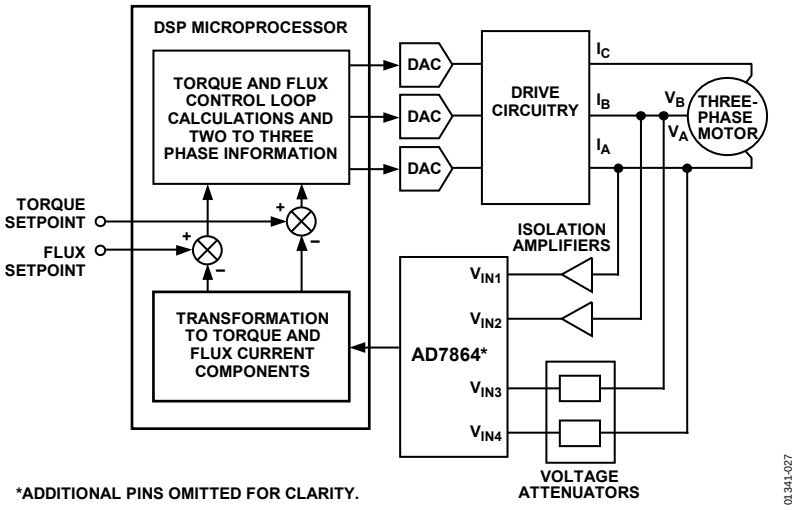


Figure 26. Vector Motor Control Using the AD7864

MULTIPLE AD7864S IN A SYSTEM

Figure 27 shows a system where a number of AD7864s are configured to handle multiple input channels. This type of configuration is common in applications such as sonar and radar. The AD7864 is specified with maximum limits on aperture delay match. This means that the user knows the difference in the sampling instant between all channels. This allows the user to maintain relative phase information between the different channels. The AD7864 has a maximum aperture delay matching of 4 ns.

All AD7864s use the same external SAR clock (5 MHz). Therefore, the conversion time for all devices is identical; consequently, all devices can be read simultaneously. In the example shown in Figure 27, the data outputs of two AD7864s are enabled onto a 32-bit wide data bus when $\overline{EOC}$ goes low.

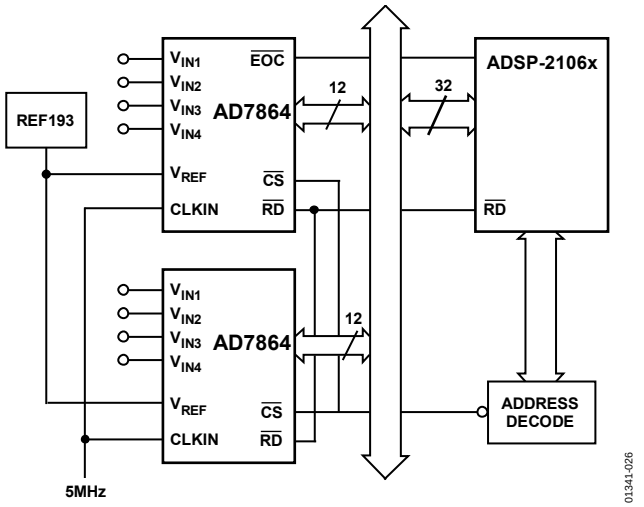
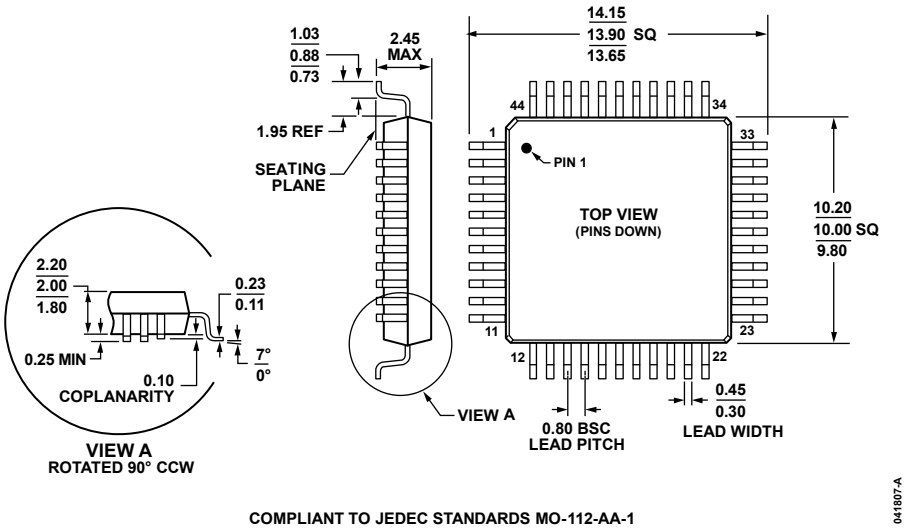


Figure 27. Multiple AD7864s in Multichannel System

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-112-AA-1

Figure 28. 44-Lead Metric Quad Flat Package [MQFP]
(S-44-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Input Ranges	Relative Accuracy	Temperature Range[1]	Package Description	Package Option
AD7864ASZ-1[2]	±5 V, ±10 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864ASZ-1REEL[2]	±5 V, ±10 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864BSZ-1[2]	±5 V, ±10 V	±0.5 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864BSZ-1REEL[2]	±5 V, ±10 V	±0.5 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864ASZ-2[2]	0 V to 2.5 V, 0 V to 5 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864ASZ-2REEL[2]	0 V to 2.5 V, 0 V to 5 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864ASZ-3[2]	±2.5 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
AD7864ASZ-3REEL[2]	±2.5 V	±1 LSB	−40°C to +85°C	44-Lead MQFP	S-44-2
EVAL-AD7864-2CB[3]				Evaluation Board	
EVAL-AD7864-3CB[3]				Evaluation Board	
EVAL-CONTROL BRD2[4]				Controller Board	

[1] The A version is fully specified up to 105°C with a maximum sample rate of 450 kSPS and I_{DD} maximum (normal mode) of 26 mA.
[2] Z = RoHS Compliant Part.
[3] This can be used as a stand alone evaluation board or in conjunction with the Evaluation Controller Board for evaluation/demonstration purposes.
[4] This board is a complete unit, allowing a PC to control and communicate with all Analog Devices, Inc., evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board needs to be ordered, for example, EVAL-AD7864-1CB, the EVAL-CONTROL BRD2, and a 12 V ac transformer. See the Evaluation Board application note for more information.

NOTES

D01341-0-2/09(D)