

60V N-Channel Enhancement Mode MOSFET- ESD Protection

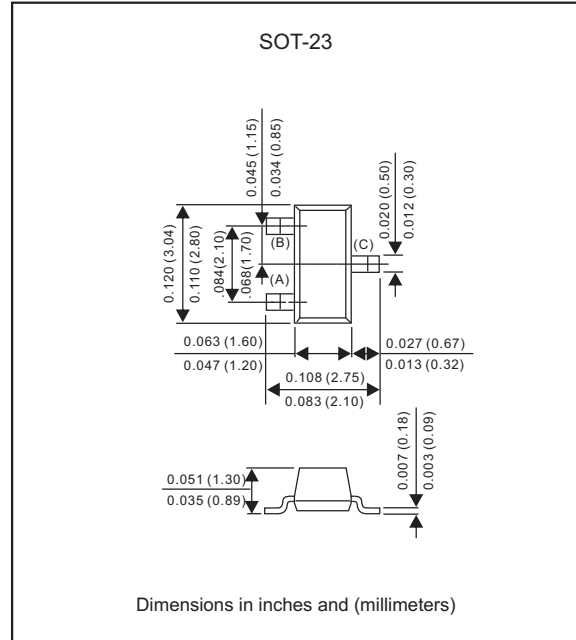
Features

- $R_{DS(ON)}$, $V_{GS}@10V$, $I_D@500mA=3.0\ \Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V$, $I_D@200mA=4.0\ \Omega$
- ESD protection 2KV (Human body mode)
- Advanced trench process technology.
- High density cell design for ultra low on-resistance.
- Very low leakage current in off condition
- Specially designed for battery operated system, solid-state relays drivers, relays, displays, lamps, solenoids, memories, etc.
- In compliance with EU RoHS 2002/95/EC directives.
- Suffix "-H" indicates Halogen-free part, ex. 2N7002E-H.

Mechanical data

- Epoxy:UL94-V0 rated flame retardant
- Case : Molded plastic, SOT-23
- Terminals : Solder plated, solderable per MIL-STD-750, Method 2026
- Mounting Position : Any
- Weight : Approximated 0.008 gram

Package outline



Maximum ratings (AT $T_A=25^\circ C$ unless otherwise noted)

PARAMETER	Symbol	Ratings	UNIT
Drain-Source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current	I_D	300	mA
Pulsed drain current ¹⁾	I_{DM}	2000	mA

PARAMETER	Symbol	MIN.	TYP.	MAX.	UNIT
Total power dissipation $P_D@T_A=25^\circ C$ $P_D@T_A=75^\circ C$	P_D			0.35 0.21	W
Operation junction and storage temperature range	T_J, T_{STG}	-55		+150	$^\circ C$
Thermal resistance(PCB mounted) ²⁾ Junction to ambient	$R_{\theta JA}$		357		$^\circ C/W$

Note : 1. Maximum DC current limited by package

2. Surface mounted on FR4 board, $t \leq 5$ sec

Electrical characteristics (AT $T_A=25^\circ\text{C}$ unless otherwise noted)

STATIC

PARAMETER	CONDITIONS	Symbol	MIN.	TYP.	MAX.	UNIT
Drain-source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\mu A$	BV_{DSS}	60			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(th)}$	1.0		2.5	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 500mA$	$R_{DS(on)}$			3.0	Ω
	$V_{GS} = 4.5V, I_D = 200mA$				4.0	
Zero Gate Voltage Drain Current	$V_{DS} = 60V, V_{GS} = 0V$	I_{DSS}			1	μA
Gate-Body leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}			± 10	μA
Forward TransConductance	$V_{DS} = 15V, I_D = 250mA$	g_{fs}	100			ms

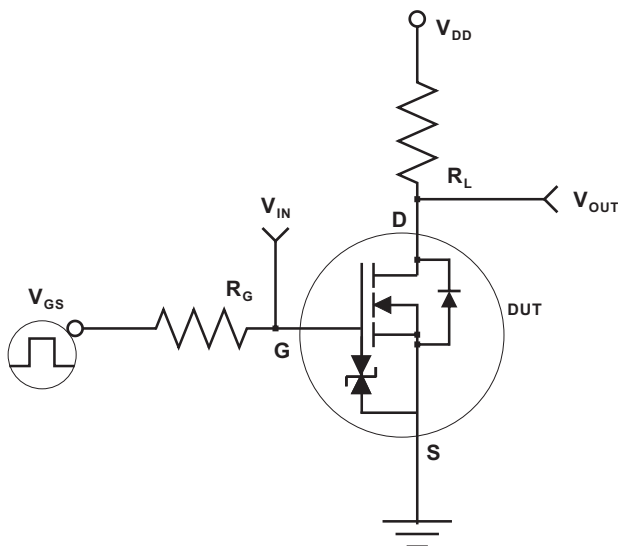
DYNAMIC

Total Gate Charge	$V_{DS} = 15V, I_D = 200mA$ $V_{GS} = 4.5V$	Q_g			0.8	nC
Turn-On Delay Time	$V_{DD} = 30V, R_L = 150\Omega, I_D = 200mA,$ $V_{gen} = 10V, R_G = 10\Omega$	t_{on}			20	ns
Turn-Off Delay Time		t_{off}			40	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V$ $f = 1.0\text{ MHz}$	C_{iss}			35	pF
Output Capacitance		C_{oss}			10	
Reverse Transfer Capacitance		C_{rss}			5	

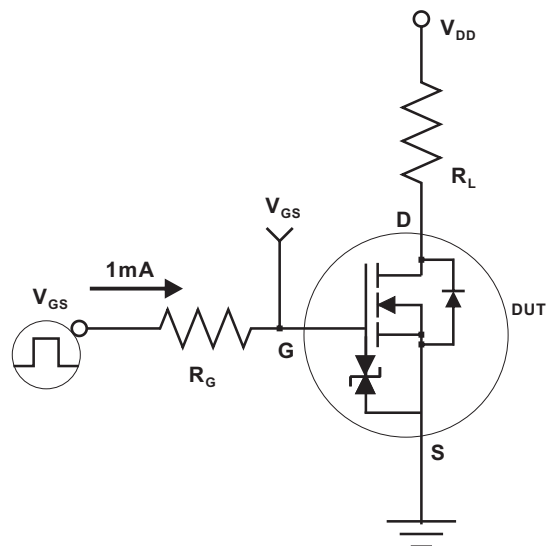
Source-Drain Diode

Diode Forward Voltage	$I_s = 200mA, V_{GS} = 0V$	V_{SD}		0.82	1.3	V
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Switching Test Circuit



Gate Charge Test Circuit



Rating and characteristic curves (2N7002E)

Fig.1 Output Characteristic

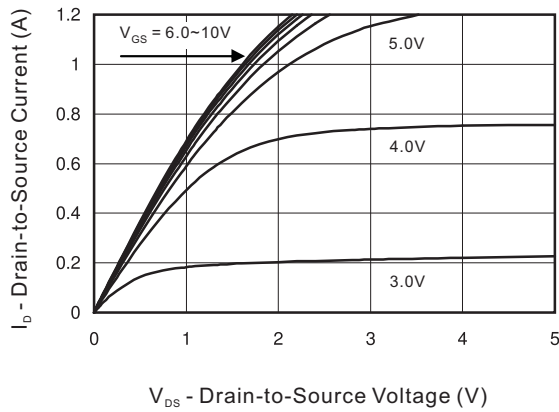


Fig.2 Transfer Characteristic

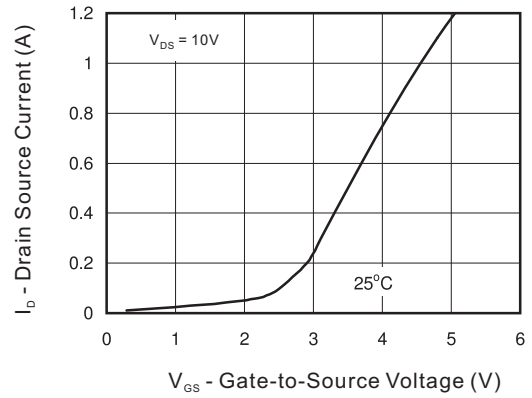


Fig.3 On Resistance vs Drain Current

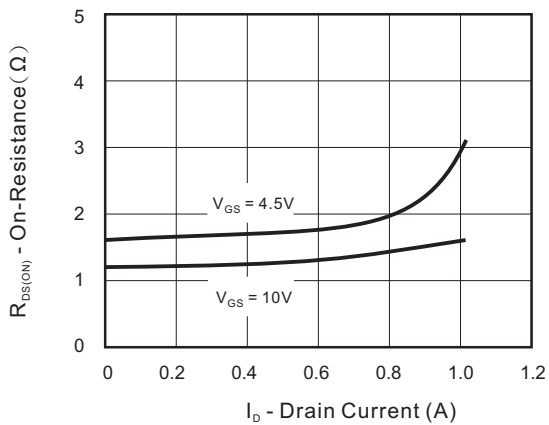


Fig.4 On Resistance vs Gate to Source Voltage

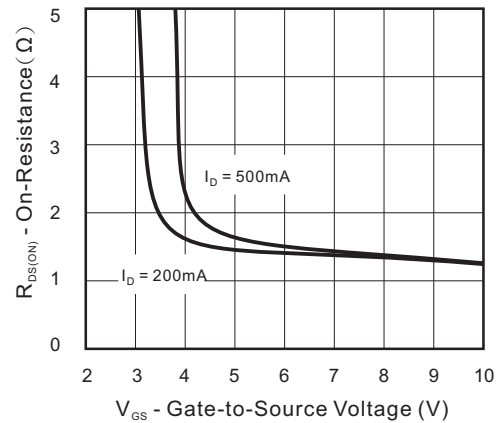
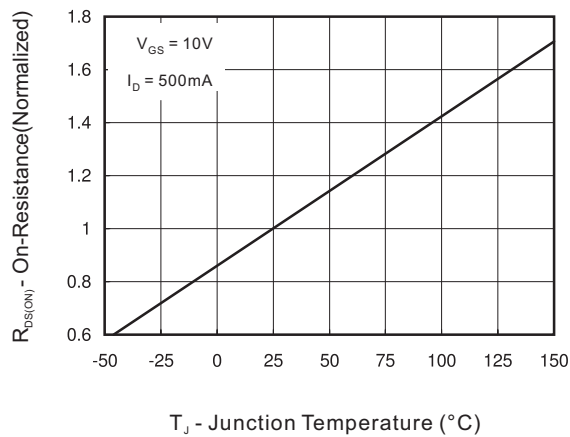


Fig.5 On Resistance vs Junction Temperature



Rating and characteristic curves (2N7002E)

Fig. 6 Gate Charge Waveform

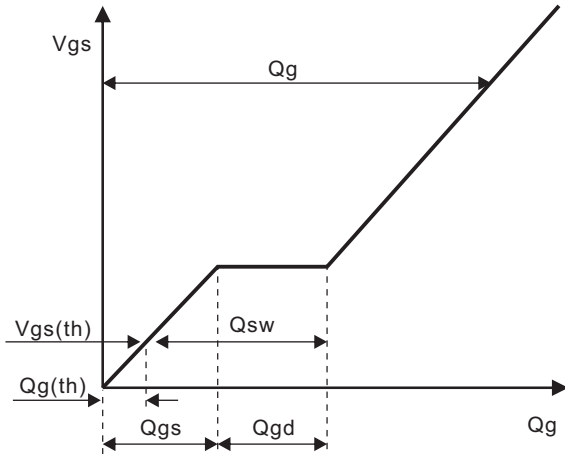


Fig.7 Gate Charge

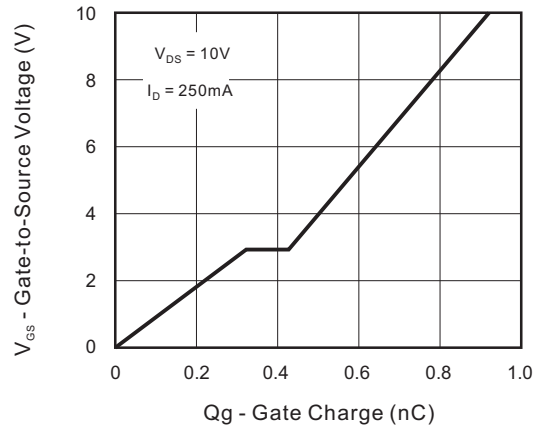


Fig.8 Threshold Voltage vs Temperature

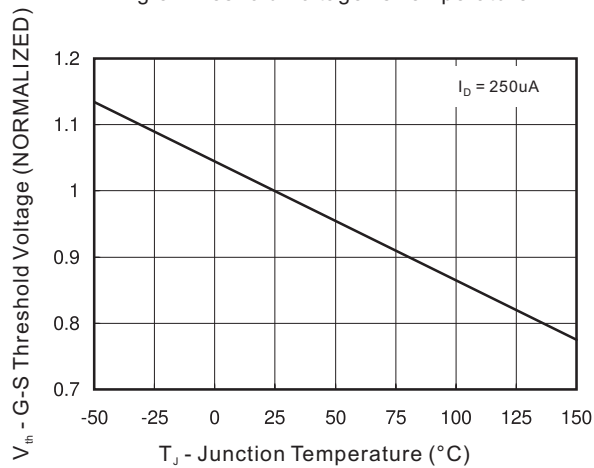


Fig.9 Breakdown Voltage vs Junction Temperature

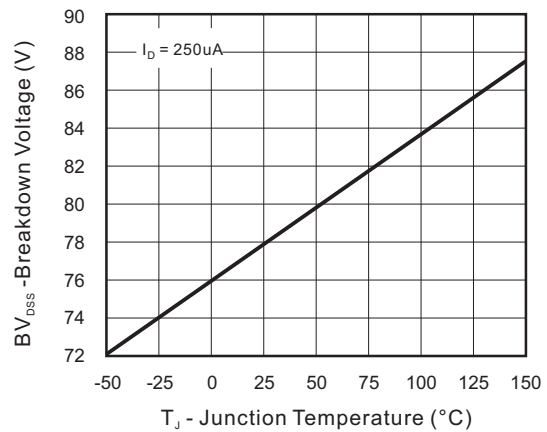
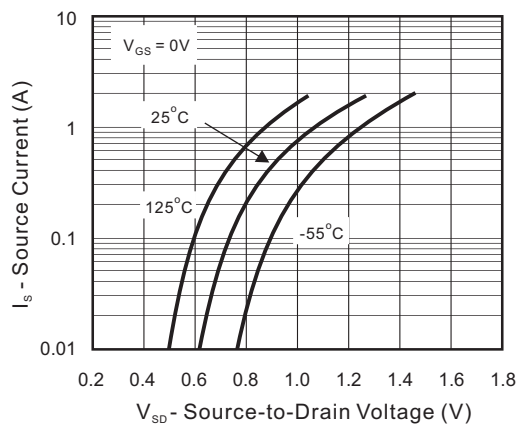
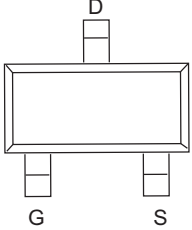
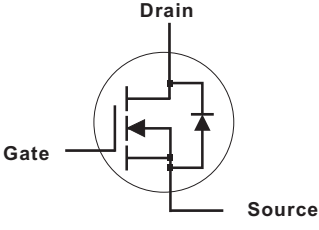


Fig.10 Source-Drain Diode Forward Voltage



Pinning information

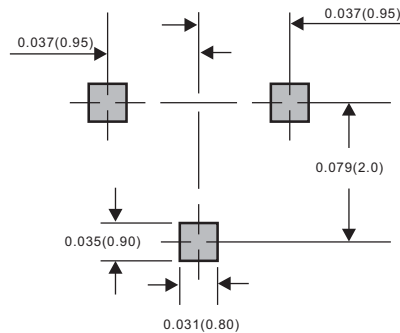
Pin	Simplified outline	Symbol
PinD Drain PinG Gate PinS Source		

Marking

Type number	Marking code
2N7002E	7002E
	72K

Suggested solder pad layout

SOT-23



Dimensions in inches and (millimeters)

Reel packing

PACKAGE	REEL SIZE	REEL (pcs)	COMPONENT SPACING (m/m)	BOX (pcs)	INNER BOX (m/m)	REEL DIA. (m/m)	CARTON SIZE (m/m)	CARTON (pcs)	APPROX. GROSS WEIGHT (kg)
SOT-23	7"	3,000	4.0	30,000	183*123*183	178	382*257*387	240,000	11.6