

SBVS016A - SEPTEMBER 1978 – REVISED JANUARY 2003

DUAL ISOLATED DC/DC CONVERTER

FEATURES

- **DUAL ISOLATED ±5V TO ±16V OUTPUTS**
- **HIGH BREAKDOWN VOLTAGE: 8000V Test**
- **LOW LEAKAGE CURRENT: < 1μA at 240V/60Hz**
- **LOW COST PER ISOLATED CHANNEL**
- **SMALL SIZE: 27.9mm x 27.9mm x 7.6mm (1.1" x 1.1" x 0.3")**

APPLICATIONS

- **MEDICAL EQUIPMENT**
- **INDUSTRIAL PROCESS CONTROL**
- **TEST EQUIPMENT**
- **DATA ACQUISITION SYSTEMS**
- **NUCLEAR INSTRUMENTATION**

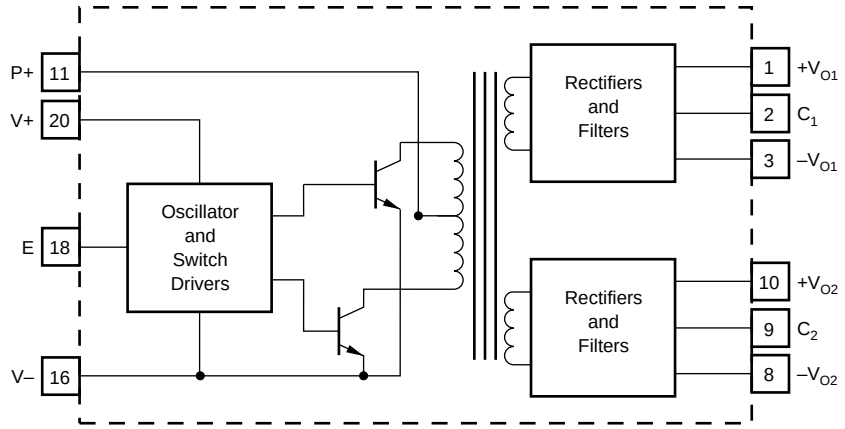
DESCRIPTION

The 722 converts a single $5V_{DC}$ to $16V_{DC}$ input into a pair of bipolar output voltages of the same value as the input voltage. The converter is capable of providing a total output current of 64mA at rated voltage accuracy and up to 200mA without damage.

The two output channels are isolated from the input and from each other. They may be connected independently, in series for higher output voltage or in parallel for higher output current, as a single channel isolated DC/DC converter.

Integrated circuit construction of the 722 reduces size and cost. High isolation breakdown voltages and low leakage currents are assured by special design and construction that includes use of a high dielectric strength, low leakage coating used on the internal assembly.

A self-contained 900kHz oscillator drives switching circuitry, which is designed to eliminate the common problem of input current spiking due to transformer saturation or crossover switching.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE(2)	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
722	DIP-20	JND	–25°C to +85°C	722	722G	Rails, 17
722BG	DIP-20	JND	–25°C to +85°C	722BG	722BG	Rails, 17
722MG	DIP-20	JND	–25°C to +85°C	722MG	722MG	Rails, 17

NOTES: (1) For the most current specifications, and package information, refer to our web site at www.ti.com. (2) –25°C to +60°C for 16mA ≤ I_{LOAD} ≤ 40mA per output.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage, V+ to V–	16V
Input Current	275mA
Operating Temperature	–25°C to +80°C
Storage Temperature	–55°C to +125°C
Junction Temperature	–55°C to +125°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_{IN} = 15VDC, C = 0.47µF, and R_1 selected per typical characteristic, unless otherwise noted.

PARAMETER	CONDITIONS	722			722BG			722MG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT											
Rated Input Voltage			15			✻			✻		VDC
Input Voltage Range(1)		5		16	✻		✻	✻		✻	VDC
Input Current	Total Output Current = 12mA		50			✻			✻		mA
	Total Output Current = 64mA		105	120		✻	✻		✻	✻	mA
	Total Output Current = 64mA at T_A = +85°C		120			✻			✻		mA
	Total Output Current = 160mA		—	—		225	275		—	—	mA
Input Ripple(2)	Total Output Current = 12mA		3			✻			✻		mA, pk
	Total Output Current = 64mA		6			✻			✻		mA, pk
	Total Output Current = 160mA		—			12			—		mA, pk
ISOLATION											
Test Voltages	Input-to-Output, 5 seconds, min			8000			✻			✻	Vpk
	Input-to-Output, 1 minute, min			—			—			2500	Vrms
	Channel-to-Channel, 5 seconds, min			5000			✻			✻	Vpk
Rated Voltages	Input-to-Output, continuous			3500			✻			✻	V
	Channel-to-Channel, continuous			2000	✻		✻			✻	V
Isolation Impedance	Input-to-Output		10 || 6			✻			✻		GΩ || pF
Leakage Current(3)	Input-to-Output, 240V, 60Hz			1			✻			✻	µA
OUTPUT											
Rated Output Voltages(4)	I_{LOAD} = 3mA per Output	15.4		16.2	✻		✻	✻		✻	VDC
	I_{LOAD} = 16mA per Output	14.3		16.2	✻		✻	✻		✻	VDC
	I_{LOAD} = 40mA per Output	—	—	—	13.0	14.2	16.2	—	—	—	VDC
Output Current	Total of All Outputs			200			✻			✻	mA
	Any One Output(5)	3		100	✻		✻	✻		✻	mA
Load Regulation			(5)			✻			✻		
Ripple Voltage	I_{LOAD} = 3mA per Output		15			✻			✻		mVpk
	I_{LOAD} = 16mA per Output		35	100		✻	✻		✻	✻	mVpk
	I_{LOAD} = 40mA per Output		—			50			✻		mVpk
Tracking Error between Dual Outputs	Balanced Loads		±200			✻			✻		mVDC
Sensitivity to Input Voltage Changes			1.13			✻			✻		V/V
Output Voltage Temperature Coefficient	T_A = $T_{SPECIFICATION\ RANGE}$		±0.02			✻			✻		%/°C
TEMPERATURE											
Specification	I_{LOAD} ≤ 16mA per Output	–25		+85	✻		✻	✻		✻	°C
	I_{LOAD} ≤ 40mA per Output	–25		+60	✻		✻	✻		✻	°C
Storage		–55		+125	✻		✻	✻		✻	°C
Junction Temperature				+125			✻			✻	°C

✻ Specifications same as 722.

NOTES: (1) For ambient temperature above +70°C, the input voltage is 12.5V (max). The input voltage remains 16V (max) if case temperature is kept below +85°C. (2) External capacitor across P+ to V– pins and 12" of #24 wire to V_{IN}. (3) Reference UL544, paragraph 27.5, Leakage Current. (4) See Typical Characteristics. (5) A minimum output current of 3mA at each output is recommended to maintain output voltage accuracy.

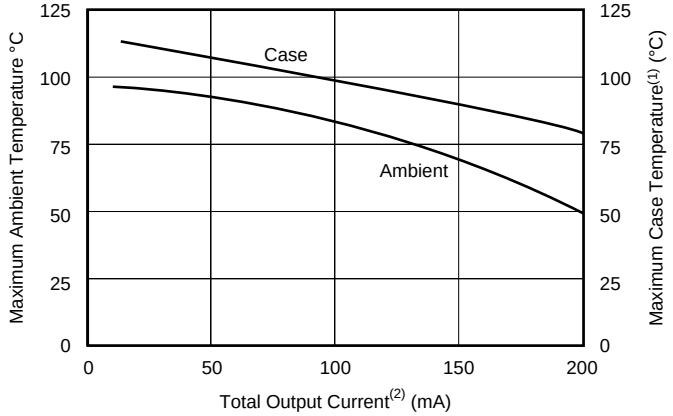
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{IN} = 15VDC, C = 0.47µF, and R_1 selected per typical characteristic, unless otherwise noted.

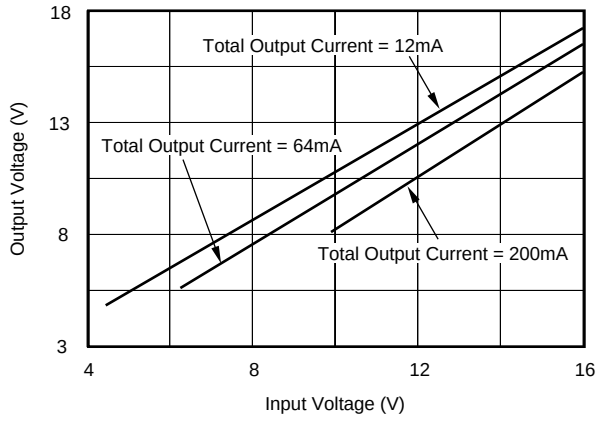
SELECTION OF R_1 OR EXTERNAL VOLTAGE V+
FOR MINIMUM INTERNAL POWER DISSIPATION

		MAXIMUM OUTPUT CURRENT FROM ANY SINGLE OUTPUT		
		<16mA	16mA to 30mA	30mA
Input Voltage (V)	>13	1.3kΩ	820Ω	510Ω
	11 to 13	820Ω	510Ω	200Ω
	9 to 11	510Ω	200Ω	0Ω
	8 to 9	200Ω	0Ω	—
	<8	0Ω	—	—
	$V+_{EXT}$	6.5V	7.5V	9.0V

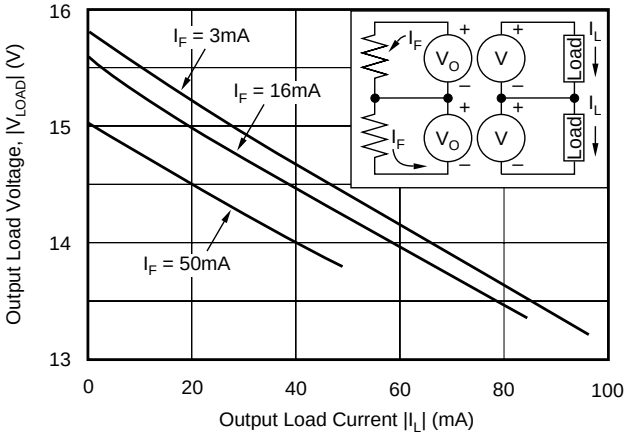
MAXIMUM SAFE OPERATING TEMPERATURE
vs TOTAL OUTPUT CURRENT



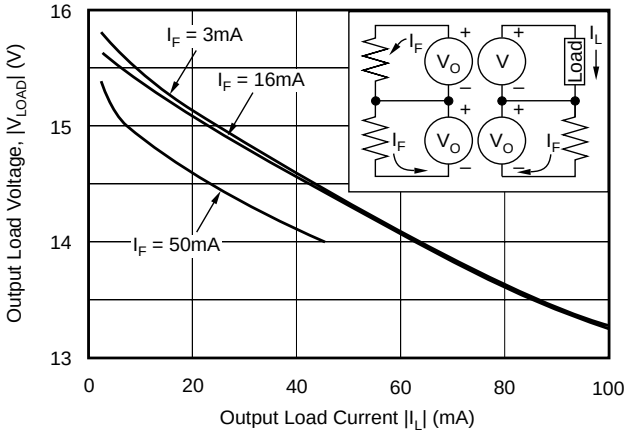
OUTPUT VOLTAGE vs INPUT VOLTAGE



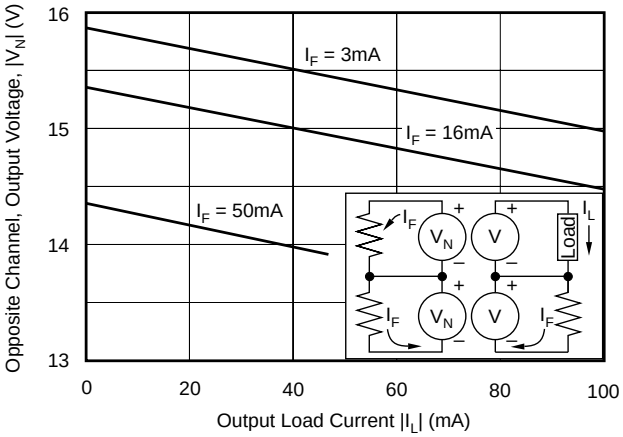
SINGLE-CHANNEL LOAD REGULATION



SINGLE OUTPUT LOAD REGULATION



CHANNEL-TO-CHANNEL INTERACTION

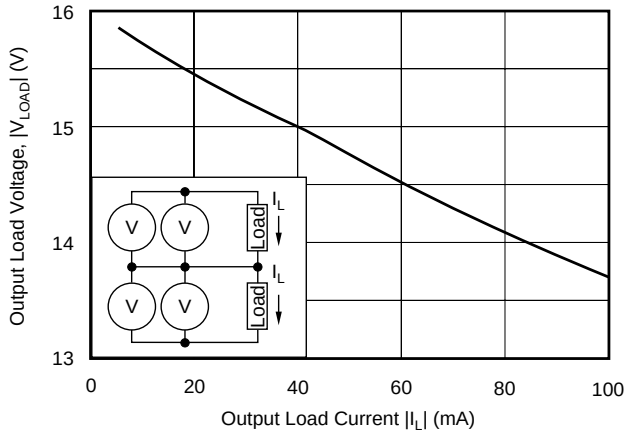


NOTES: (1) Using a 104mm x 19mm x 1.6mm aluminum strip mounted to the bottom of the case with heat sink compound. (2) Total output current is the sum of the currents for each individual output.

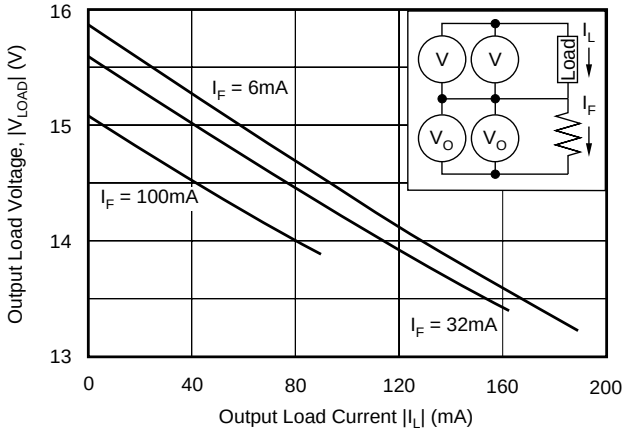
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{IN} = 15VDC, C = 0.47µF, and R_1 selected per typical characteristic, unless otherwise noted.

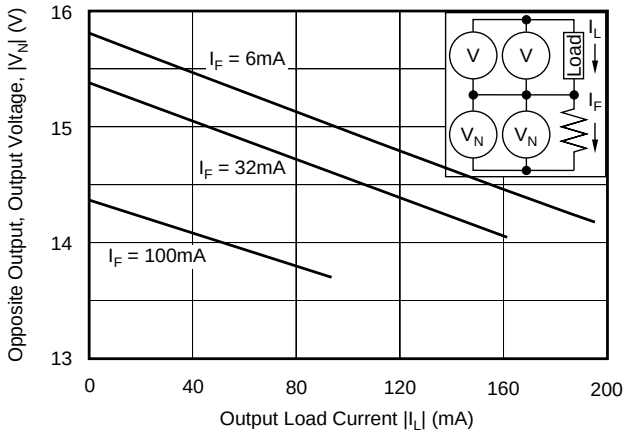
PARALLEL OUTPUT BALANCED
LOAD REGULATION



PARALLEL OUTPUT UNBALANCED
LOAD REGULATION



OUTPUT-TO-OUTPUT INTERACTION



INSTALLATION AND OPERATING INSTRUCTIONS

Typical application connections for the 722 are shown in Figures 1 and 2. Primary power (V_{IN}) is applied at the P+ and V– terminals. The common or ground for V_{IN} may be connected to either P+ or V–; the only requirement is that P+ and V+ must be positive with respects to V–.

Power for the internal oscillator and switch drivers is derived from the primary power by a voltage dropping resistor, R_1. The value of R_1 as a function of V_{IN} is shown in the Typical Characteristics section. Alternately, voltage for the V+ terminal can be obtained from a separate source. V+ should be +5V to +7.5V positive with respect to V–. If a separate source is used, the V+ input must be applied before the P+ input in order to avoid possible damage to the unit. P+ and V+ must remain positive with respect to V– at all times (including transients). If necessary, diode clamps should be attached across these inputs.

The E pin enables the converter when connected to V+ and disables it when connected to V–.

An external capacitor, C (0.47µF ceramic), is used to reduce input ripple. It should be connected as close to the P+ and V– pins as practical. Input leads to these terminals should also be kept as short as possible. External shielding may be appropriate in applications where RFI at the 900kHz nominal oscillator frequency is a problem because the 722 is not internally shielded.

Each output is filtered with an internal 0.22µF capacitor. Output ripple voltage can be reduced below the specified value by adding external capacitors up to 10µF between each output and its common.

DISCUSSION

OUTPUT CURRENT RATINGS

At rated output voltage accuracy, the 722 is capable of providing 64mA divided among its four outputs(1). A minimum average output current of 3mA is recommended at each output to maintain voltage accuracy.

Output channels(2) can be connected in series or parallel for higher output voltage or current.

ISOLATION CONFIGURATIONS

The fact that the two outputs of the 722 are isolated from the input and from each other allows both two-port and three-port isolation connections.

Figure 1 shows TI's 3650 optically coupled isolation amplifier connected in three-port configuration. One of the 722 channels provides power to the 3650 input. The other channel supplies power to the 3650 output. The amplifier input and output are isolated from each other and the system power supply common. In this configuration, the 722 channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

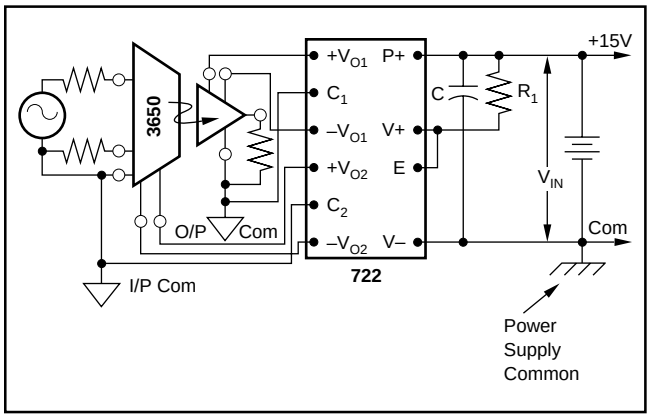


FIGURE 1. Three-Port Isolation.

NOTES: (1) "Output" denotes a single output terminal (+V or –V) and its associated common. (2) "Channel" denotes a pair of outputs (+V and –V) and their associated common.

Figure 2 illustrates how the 722 can provide isolated input power to the input stage of two 3650s connected in the two-port configuration. Power for the output stage is provided by the system +15V and –15V supplies. Input stages are isolated from each other and from the system supply. In this situation, the 722 input-to-output isolation specification applies to the amplifier input-to-output voltages, whereas the channel-to-channel 722 specification applies to the voltage existing between I/P Com #1 and I/P Com #2.

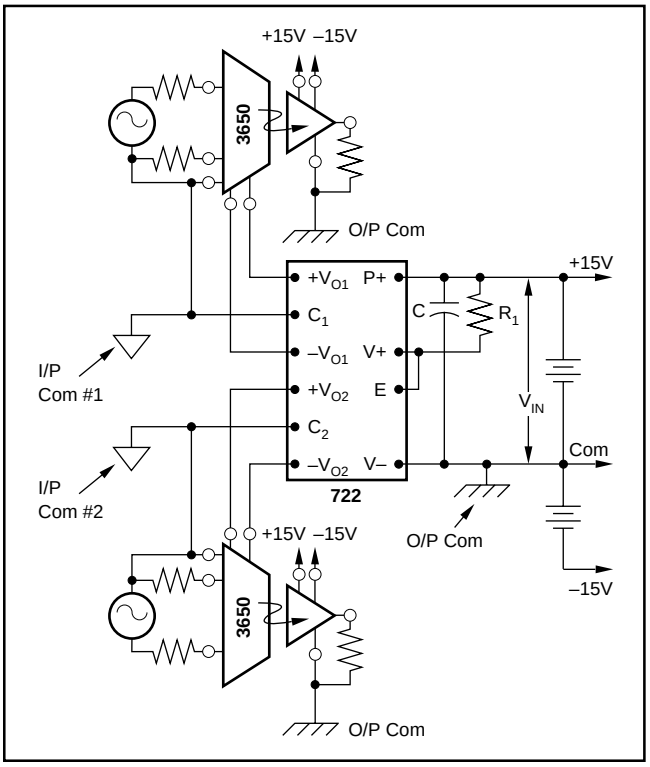


FIGURE 2. Two-Port Isolation with Two 3650s.

SHORT CIRCUIT PROTECTION

The circuit in Figure 3 may be added to the input of the 722 to protect it from damage in situations where too much current is demanded from the outputs—such as a short circuit from an output to its common. The circuit limits input current to approximately 150mA for an input voltage of 15VDC (for ß of 2N2219 of 50).

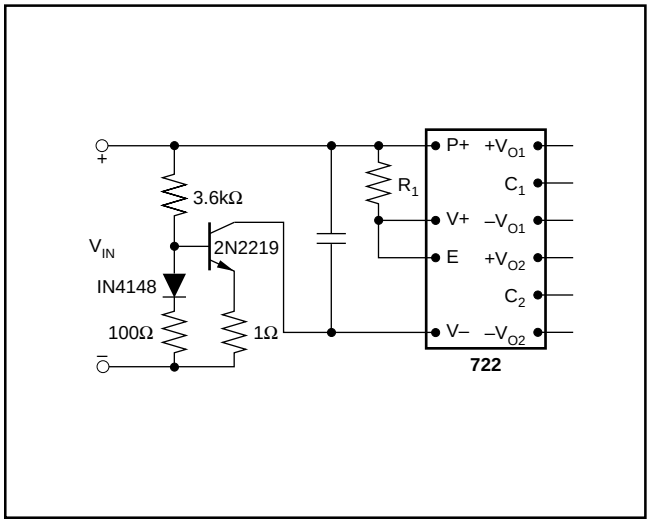
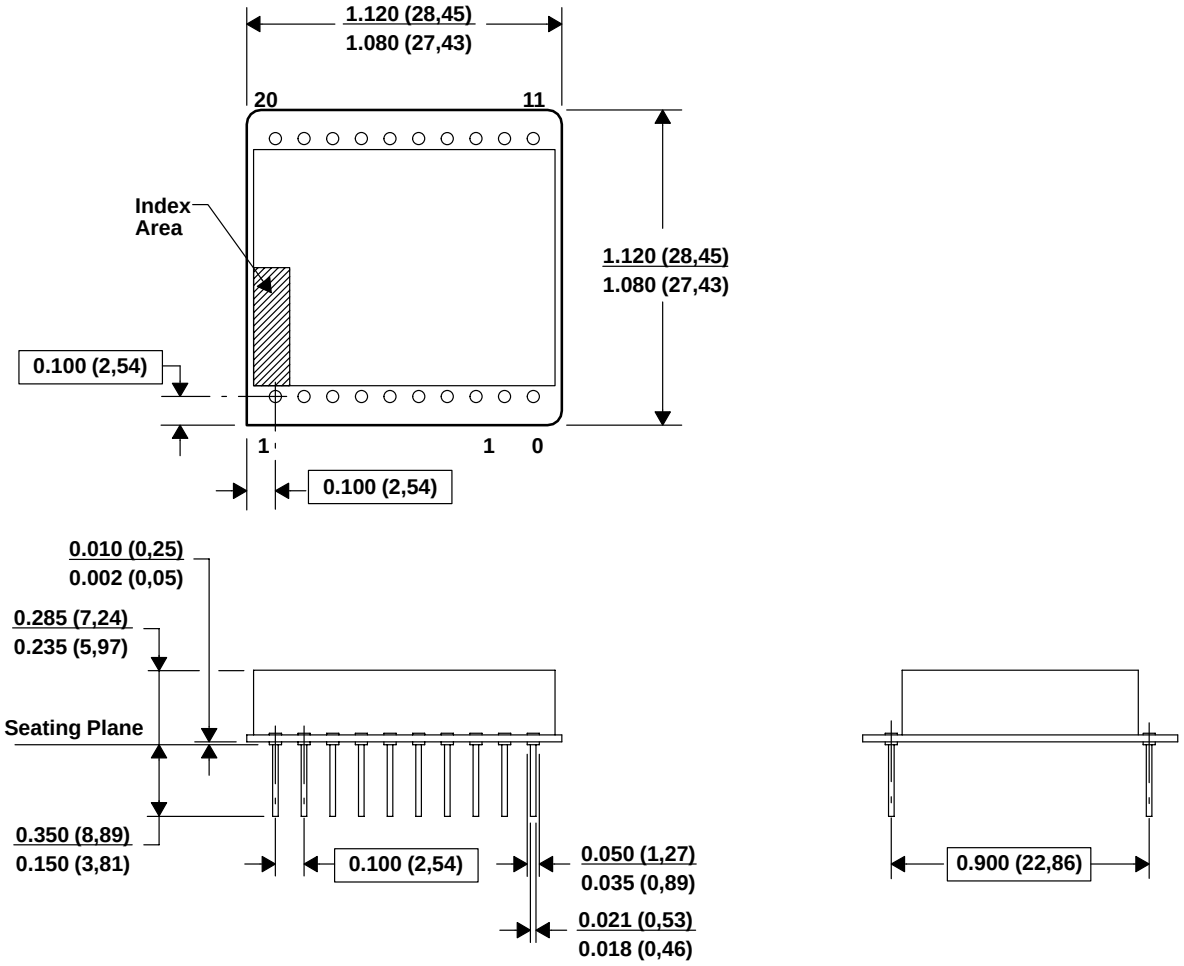


FIGURE 3. Short-Circuit Protection.

JND (R-CDIP–P20) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. A visual index feature must be located within the cross–hatched area.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
0722BG	NRND	CDIP	JND	20	17
0722MG	NRND	CDIP	JND	20	17
722G	ACTIVE	CDIP	JND	20	17

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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