

IN74AC109

Dual J-K Flip-Flop with Set and Reset

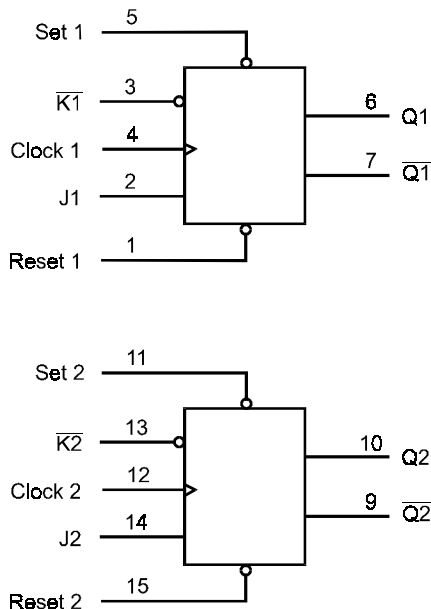
High-Speed Silicon-Gate CMOS

The IN74AC109 is identical in pinout to the LS/ALS109, HC/HCT109. The device inputs are compatible with standard CMOS outputs, with pullup resistors, they are compatible with LS/ALS outputs.

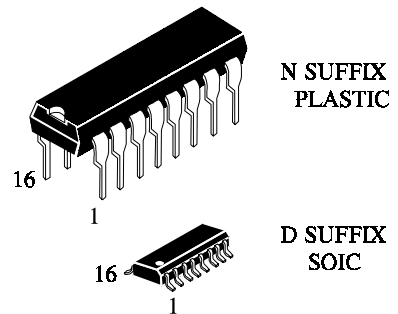
This device consists of two J-K flip-flops with individual set, reset, and clock inputs. Changes at the inputs are reflected at the outputs with the next low-to-high transition of the clock. Both Q to Q outputs are available from each flip-flop.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- High Noise Immunity Characteristic of CMOS Devices
- Outputs Source/Sink 24 mA

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



ORDERING INFORMATION

IN74AC109N Plastic

IN74AC109D SOIC

$T_A = -40^\circ$ to 85° C for all packages

PIN ASSIGNMENT

RESET 1	1	16	V_{CC}
J1	2	15	RESET 2
$\overline{K1}$	3	14	J2
CLOCK 1	4	13	$\overline{K2}$
SET 1	5	12	CLOCK 2
Q1	6	11	SET 2
$\overline{Q1}$	7	10	Q2
GND	8	9	$\overline{Q2}$

FUNCTION TABLE

Inputs					Outputs	
Set	Reset	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H		L	L	L	H
H	H		H	L	Toggle	
H	H		L	H	No Change	
H	H		H	H	H	L
H	H	L	X	X	No Change	

X = Don't care

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V	
T _J	Junction Temperature (PDIP)		140	°C	
T _A	Operating Temperature, All Package Types	-40	+85	°C	
I _{OH}	Output Current - High		-24	mA	
I _{OL}	Output Current - Low		24	mA	
t _r , t _f	Input Rise and Fall Time * (except Schmitt Inputs)	V _{CC} =3.0 V V _{CC} =4.5 V V _{CC} =5.5 V	0 0 0	150 40 25	ns/V

* V_{IN} from 30% to 70% V_{CC}

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit		Unit
				25 °C	-40°C to 85°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0 4.5 5.5	2.1 3.15 3.85	2.1 3.15 3.85	V
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V	3.0 4.5 5.5	0.9 1.35 1.65	0.9 1.35 1.65	V
V _{OH}	Minimum High-Level Output Voltage	I _{OUT} ≤ -50 µA	3.0 4.5 5.5	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V _{IN} =V _{IH} or V _{IL} I _{OH} =-12 mA	3.0	2.56	2.46	
		I _{OH} =-24 mA	4.5	3.86	3.76	
		I _{OH} =-24 mA	5.5	4.86	4.76	
V _{OL}	Maximum Low-Level Output Voltage	I _{OUT} ≤ 50 µA	3.0 4.5 5.5	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V _{IN} =V _{IH} or V _{IL} I _{OL} =12 mA	3.0	0.36	0.44	
		I _{OL} =24 mA	4.5	0.36	0.44	
		I _{OL} =24 mA	5.5	0.36	0.44	
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	5.5	±0.1	±1.0	µA
I _{OLD}	+Minimum Dynamic Output Current	V _{OLD} =1.65 V Max	5.5		75	mA
I _{OHD}	+Minimum Dynamic Output Current	V _{OHD} =3.85 V Min	5.5		-75	mA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND	5.5	4.0	40	µA

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}

AC ELECTRICAL CHARACTERISTICS($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V _{CC} [*] V	Guaranteed Limits				Unit
			25 °C		-40°C to 85°C		
			Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency (Figure 1)	3.3 5.0	125 150		100 125		MHz
t _{PLH}	Propagation Delay , Clock to Q or Q [¯] (Figure 1)	3.3 5.0	4.0 2.5	13.5 10.0	3.5 2.0	16.0 10.5	ns
t _{PHL}	Propagation Delay , Clock to Q or Q [¯] (Figure 1)	3.3 5.0	3.0 2.0	14.0 10.0	3.0 1.5	14.5 10.5	ns
t _{PLH}	Propagation Delay , Set or Reset to Q or Q [¯] (Figure 2)	3.3 5.0	3.0 2.5	12.0 9.0	2.5 2.0	13.0 10.0	ns
t _{PHL}	Propagation Delay , Set or Reset to Q or Q [¯] (Figure 2)	3.3 5.0	3.0 2.0	12.0 9.5	3.0 2.0	13.5 10.5	ns
C _{IN}	Maximum Input Capacitance	5.0	4.5		4.5		pF

C _{PD}	Power Dissipation Capacitance	Typical @25°C,V _{CC} =5.0 V	pF
		35	

*Voltage Range 3.3 V is 3.3 V $\pm$ 0.3 V

Voltage Range 5.0 V is 5.0 V $\pm$ 0.5 V

TIMING REQUIREMENTS($C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

Symbol	Parameter	V_{CC}^* V	Guaranteed Limits		Unit
			25 °C	-40°C to 85°C	
t_{su}	Minimum Setup Time, J or $\overline{K}$ to Clock (Figure 3)	3.3 5.0	6.5 4.5	7.5 5.0	ns
t_h	Minimum Hold Time, Clock to J or $\overline{K}$ (Figure 3)	3.3 5.0	0 0.5	0 0.5	ns
t_w	Minimum Pulse Width, Set, Reset, Clock (Figures 1,2)	3.3 5.0	4.0 3.5	4.5 3.5	ns
t_{rec}	Minimum Recovery Time, Set or Reset to Clock (Figure 2)	3.3 5.0	0 0	0 0	ns

*Voltage Range 3.3 V is 3.3 V $\pm$ 0.3 V

Voltage Range 5.0 V is 5.0 V $\pm$ 0.5 V

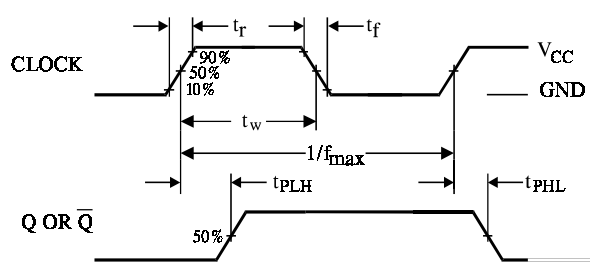


Figure 1. Switching Waveform

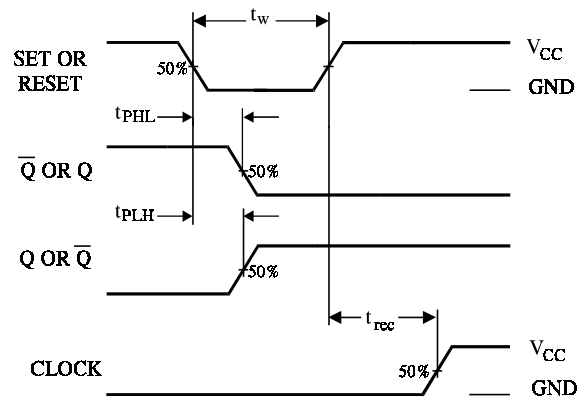


Figure 2. Switching Waveform

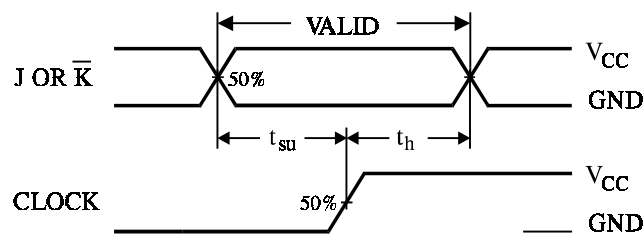


Figure 3. Switching Waveform

EXPANDED LOGIC DIAGRAM

