CC2550
Low-Cost Low-Power 2.4 GHz RF Transmitter

Applications

- *2400-2483.5 MHz ISM/SRD band systems*
- *Consumer electronics*
- *Wireless game controllers*
- *Wireless audio*
- *RF enabled remote controls*

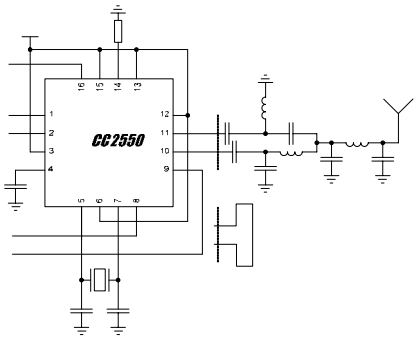
Product Description

The ***CC2550*** is a low-cost 2.4 GHz transmitter designed for very low-power wireless applications. The circuit is intended for the 2400-2483.5 MHz ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency band.

The RF transmitter is integrated with a highly configurable baseband modulator. The modulator supports various modulation formats and has a configurable data rate up to 500 kBaud.

The ***CC2550*** provides extensive hardware support for packet handling, data buffering and burst transmissions.

The main operating parameters and the 64-byte transmit FIFO of ***CC2550*** can be controlled via an SPI interface. In a typical system, the ***CC2550*** will be used together with a micro-controller and a few passive components.



Key Features

RF Performance

- Programmable output power up to +1 dBm
- Programmable data rate from 1.2 to 500 kBaud
- Frequency range: 2400 – 2483.5 MHz

Analog Features

- OOK, 2-FSK, GFSK, and MSK supported
- Suitable for frequency hopping and multi-channel systems due to a fast settling frequency synthesizer with 90 us settling time
- Integrated analog temperature sensor

Digital Features

- Flexible support for packet oriented systems: On-chip support for sync word insertion, flexible packet length, and automatic CRC handling
- Efficient SPI interface: All registers can be programmed with one “burst” transfer
- Optional automatic whitening of data

Low-Power Features

- 200 nA SLEEP mode current consumption
- Fast startup time: 240 us from SLEEP to TX mode (measured on EM design [3])
- 64-byte TX data FIFO (enables burst mode data transmission)

General

- Few external components: Complete on-chip frequency synthesizer, no external filters needed
- Green package: RoHS compliant and no antimony or bromine
- Small size (QLP 4x4 mm package, 16 pins)
- Suited for systems compliant with EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Support for asynchronous and synchronous serial transmit mode for backwards compatibility with existing radio communication protocols

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Abbreviations

Abbreviations used in this data sheet are described below.

ACP	Adjacent Channel Power
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
ARIB	Association of Radio Industries and Businesses
ASK	Amplitude Shift Keying
BER	Bit Error Rate
BT	Bandwidth-Time product
CFR	Code of Federal Regulations
CRC	Cyclic Redundancy Check
DC	Direct Current
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FEC	Forward Error Correction
FHSS	Frequency Hopping Spread Spectrum
FIFO	First-In-First-Out
2-FSK	Frequency Shift Keying
GFSK	Gaussian shaped Frequency Shift Keying
I/Q	In-Phase/Quadrature
ISM	Industrial, Scientific and Medical
LC	Inductor-Capacitor
LO	Local Oscillator
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSK	Minimum Shift Keying
NA	Not Applicable
NRZ	Non Return to Zero (coding)
LO	Local Oscillator
OBW	Occupied Bandwidth
OOK	On Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
POR	Power-on Reset
QPSK	Quadrature Phase Shift Keying
QLP	Quad Leadless Package
RF	Radio Frequency
RX	Receive, Receive Mode
SMD	Surface Mount Device
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SRD	Short Range Device
TX	Transmit, Transmit Mode
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Networks
XOSC	Crystal Oscillator
XTAL	Crystal

1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Parameter	Min	Max	Units	Condition/Note
Supply voltage	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N and DCOUPL	–0.3	2.0	V	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020D
ESD		<500	V	According to JEDEC STD 22, method A114, Human Body Model

Table 1: Absolute Maximum Ratings

2 Operating Conditions

The *CC2550* operating conditions are listed in Table 2 below.

Parameter	Min	Max	Unit	Condition/Note
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	2400		2483.5	MHz	
Data rate	1.2		500	kBaud	2-FSK
	1.2		250	kBaud	GFSK and OOK
	26		500	kBaud	(Shaped) MSK (also known as differential offset QPSK)
					Optional Manchester encoding (the data rate in kbps will be half the baud rate).

Table 3: General Characteristics

4 Electrical Specifications

4.1 Current Consumption

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurement results obtained using the CC2550EM reference design ([3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Current consumption in power down modes		200		nA	Voltage regulator to digital part off (SLEEP state). All GD0 pins programmed to 0x2F (HW to o)
		160		μA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		1.4		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		7.3		mA	Only the frequency synthesizer is running (FSTXON state). This current consumption is also representative for the other intermediate states when going from IDLE to TX, including the calibration state.
Current consumption, TX states		11.2		mA	Transmit mode, –12 dBm output power
		14.7		mA	Transmit mode, -6 dBm output power
		19.4		mA	Transmit mode, 0 dBm output power
		21.3		mA	Transmit mode, +1 dBm output power

Table 4: Current Consumption

4.2 RF Transmit Section

Tc = 25°C, VDD = 3.0 V, 0 dBm if nothing else stated. All measurement results obtained using the CC2550EM reference design ([3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance		80 + j74		Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC2550EM reference design ([3]) available from the TI website.
Output power, highest setting		+1		dBm	Output power is programmable and full range is available across the entire frequency band. Delivered to 50 Ω single-ended load via CC2550EM reference design ([3]) RF matching network.
Output power, lowest setting		–30		dBm	Output power is programmable and full range is available across the entire frequency band. Delivered to 50 Ω single-ended load via CC2550EM reference design ([3]) RF matching network. It is possible to program less than -30 dBm output power, but this is not recommended due to large variation in output power across operating conditions and processing corners for these settings.
Adjacent channel power (ACP) @2440 MHz		-25 -25 -25 -24		dBc dBc dBc dBc	2.4 kBaud, 38.2 kHz deviation, 2-FSK, 250 kHz channel spacing 10 kBaud, 38.2 kHz deviation, 2-FSK, 250 kHz channel spacing 250 kBaud, MSK, 750 kHz channel spacing 500 kBaud, MSK, 1 MHz channel spacing
Spurious emissions 25 MHz – 1 GHz 47-74, 87.5-118, 174-230, 470-862 MHz 1800-1900 MHz At 2·RF and 3·RF Otherwise above 1 GHz			 –36 –54 –47 –41 –30	 dBm dBm dBm dBm dBm	 Restricted band in Europe Restricted bands in USA
TX latency		8		bit	Serial operation. Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports.

Table 5: RF Transmit Parameters

4.3 Crystal Oscillator

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurement results obtained using the CC2550EM reference design ([3]).

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
ESR			100	Ω	
Start-up time		150		µs	Measured on CC2500EM reference design ([3]) using crystal AT-41CD2 from NDK. This parameter is to a large degree crystal dependent.

Table 6: Crystal Oscillator Parameters

4.4 Frequency Synthesizer Characteristics

Tc = 25°C, VDD = 3.0 V if nothing else stated. All measurement results obtained using the CC2550EM reference design ([3]). Min figures are given using a 27 MHz crystal. Typ and max figures are given using a 26 MHz crystal.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	427	Hz	26-27 MHz crystal.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise @2440 MHz		–74		dBc/Hz	@ 50 kHz offset from carrier
		–74		dBc/Hz	@ 100 kHz offset from carrier
		–77		dBc/Hz	@ 200 kHz offset from carrier
		–97		dBc/Hz	@ 1 MHz offset from carrier
		–106		dBc/Hz	@ 2 MHz offset from carrier
		–114		dBc/Hz	@ 5 MHz offset from carrier
		–117		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on / hop time	85.1	88.4	88.4	µs	Time from leaving the IDLE state until arriving in the FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL calibration time	694	721	721	µs	Calibration can be initiated manually or automatically before entering or after leaving RX/TX.

Table 7: Frequency Synthesizer Parameters

4.5 Analog Temperature Sensor

The characteristics of the analog temperature sensor at 3.0 V supply voltage are listed in Table 8 below. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.660		V	
Output voltage at 0°C		0.755		V	
Output voltage at +40°C		0.859		V	
Output voltage at +80°C		0.958		V	
Temperature coefficient		2.54		mV/°C	Fitted from –20°C to +80°C
Error in calculated temperature, calibrated	-2 *	0	2 *	°C	From –20°C to +80°C when using 2.54 mV / °C, after 1-point calibration at room temperature * The indicated minimum and maximum error with 1-point calibration is based on simulated values for typical process parameters
Current consumption increase when enabled		0.3		mA	

Table 8: Analog Temperature Sensor Parameters

4.6 DC Characteristics

Tc = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition/Note
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	NA	-50	nA	Input equals 0 V
Logic "1" input current	NA	50	nA	Input equals VDD

Table 9: DC Characteristics

4.7 Power-On Reset

When the power supply complies with the requirements in Table 10 below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. See Section 16.1 on page 25 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0 V until reaching 1.8 V
Power off time	1			ms	Minimum time between power off and power-on.

Table 10: Power-on Reset Requirements

5 Pin Configuration

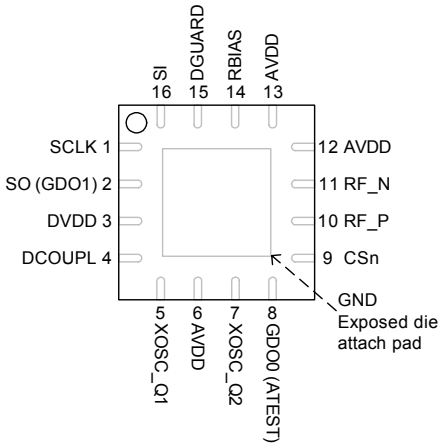

Figure 1: Pinout Top View

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

Pin #	Pin Name	Pin Type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when CSn is high
3	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator
4	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling. NOTE: This pin is intended for use with the ***CC2550*** only. It can not be used to provide supply voltage to other devices.
5	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
6	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
7	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
8	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clock output, down-divided from XOSC • Serial input TX data Also used as analog test I/O for prototype/production testing
9	CSn	Digital Input	Serial configuration interface, chip select
10	RF_P	RF Output	Positive RF output signal from PA
11	RF_N	RF Output	Negative RF output signal from PA
12	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
13	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
14	RBIAS	Analog I/O	External bias resistor for reference current
15	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
16	SI	Digital Input	Serial configuration interface, data input

Table 11: Pinout Overview

6 Circuit Description

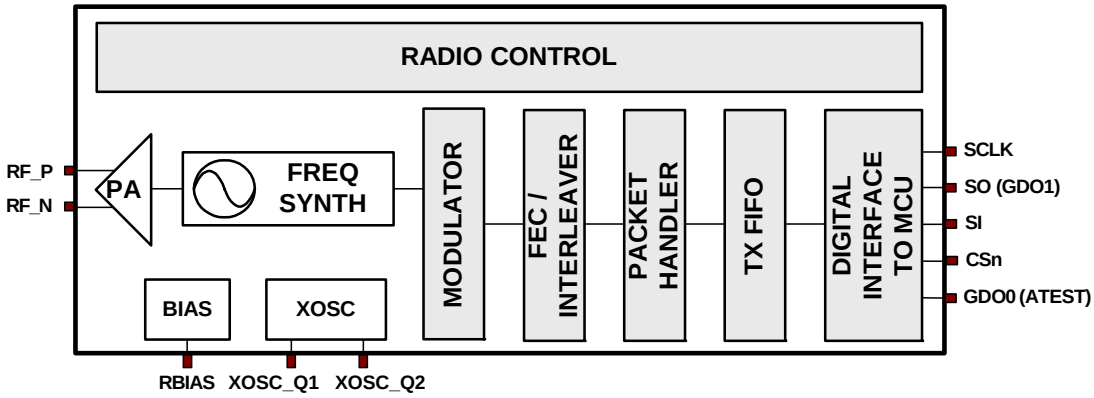

Figure 2: *CC2550* Simplified Block Diagram

A simplified block diagram of ***CC2550*** is shown in Figure 2.

The ***CC2550*** transmitter is based on direct synthesis of the RF frequency.

The frequency synthesizer includes a completely on-chip LC VCO.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

7 Application Circuit

Only a few external components are required for using the ***CC2550***. The recommended application circuit is shown in Figure 3. The external components are described in Table 12, and typical values are given in Table 13.

Bias resistor

The bias resistor R141 is used to set an accurate bias current.

Balun and RF matching

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C102, C112, L101, and L111) form a balun that converts the differential RF signal on ***CC2550*** to a single-ended RF signal. C101 and C111 are needed for DC blocking. Together with an appropriate LC network, the balun components also transform the impedance to match a 50 Ω antenna (or cable). Suggested values are listed in Table 13.

The balun and LC filter component values and their placement are important to keep the performance optimized. It is highly recommended to follow the CC2550EM reference design ([3]).

Crystal

The crystal oscillator uses an external crystal with two loading capacitors (C51 and C71). See Section 22 on page 32 for details.

Power supply decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. The CC2550EM reference design ([3]) should be followed closely.

Component	Description
C41	Decoupling capacitor for on-chip voltage regulator to digital part
C51/C71	Crystal loading capacitors, see Section 22 on page 32 for details
C101/C111	RF balun DC blocking capacitors
C102/C112	RF balun/matching capacitors
C103/C104	RF LC filter/matching capacitors
L101/L111	RF balun/matching inductors (inexpensive multi-layer type)
L102	RF LC filter inductor (inexpensive multi-layer type)
R141	Resistor for internal bias current reference
XTAL	26-27 MHz crystal, see Section 22 on page 32 for details

Table 12: Overview of External Components (excluding supply decoupling capacitors)

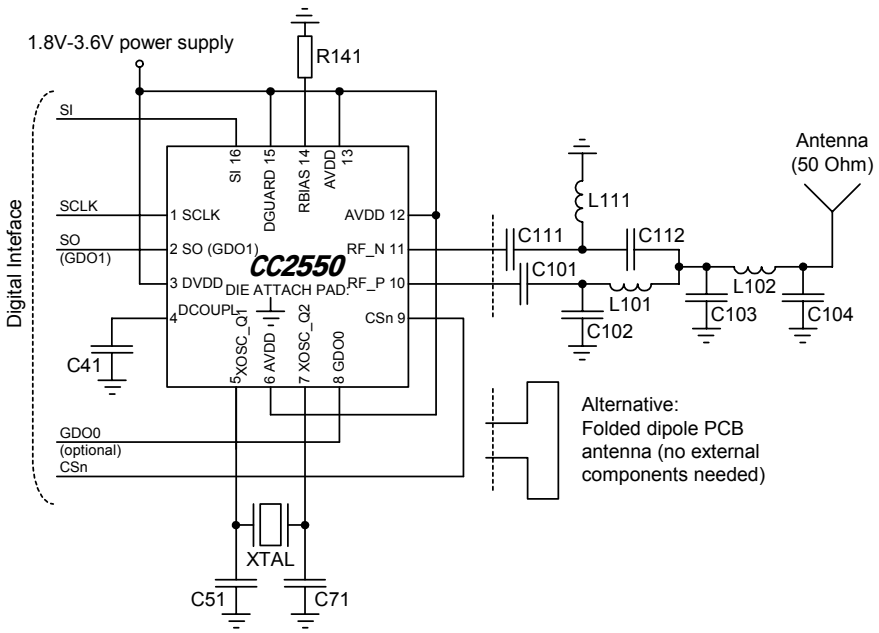

Figure 3: Typical Application and Evaluation Circuit (excluding supply decoupling capacitors)

Component	Value	Manufacturer
C41	100 nF±10%, 0402 X5R	Murata GRM15 series
C51	27 pF±5%, 0402 NP0	Murata GRM15 series
C71	27 pF±5%, 0402 NP0	Murata GRM15 series
C101	100 pF±5%, 0402 NP0	Murata GRM15 series
C102	1.0 pF±0.25pF, 0402 NP0	Murata GRM15 series
C103	1.8 pF±0.25pF, 0402 NP0	Murata GRM15 series
C104	1.5 pF±0.25pF, 0402 NP0	Murata GRM15 series
C111	100 pF±5%, 0402 NP0	Murata GRM15 series
C112	1.0 pF±0.25pF, 0402 NP0	Murata GRM15 series
L101	1.2 nH±0.3nH, 0402 monolithic	Murata LQG15 series
L102	1.2 nH±0.3nH, 0402 monolithic	Murata LQG15 series
L111	1.2 nH±0.3nH, 0402 monolithic	Murata LQG15 series
R141	56 kΩ±1%, 0402	Koa RK73 series
XTAL	26.0 MHz surface mount crystal	NDK, AT-41CD2

Table 13: Bill of Materials for the Application Circuit

Measurements have been performed with multi-layer inductors from other manufacturers (e.g. Würth) and the measurement results were the same as when using the Murata part.

The Gerber files for the CC2550EM reference design ([3]) are available from the TI website.

8 Configuration Overview

CC2550 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power – down
- Transmit mode
- RF channel selection
- Data rate
- Modulation format
- RF output power
- Data buffering with 64-byte transmit FIFO
- Packet radio hardware support
- Forward Error Correction (FEC) with interleaving
- Data Whitening

Details of each configuration register can be found in Section 28, starting on page 37.

Figure 4 shows a simplified state diagram that explains the main ***CC2550*** states, together with typical usage and current consumption. For detailed information on controlling the ***CC2550*** state machine, and a complete state diagram, see Section 16, starting on page 25.

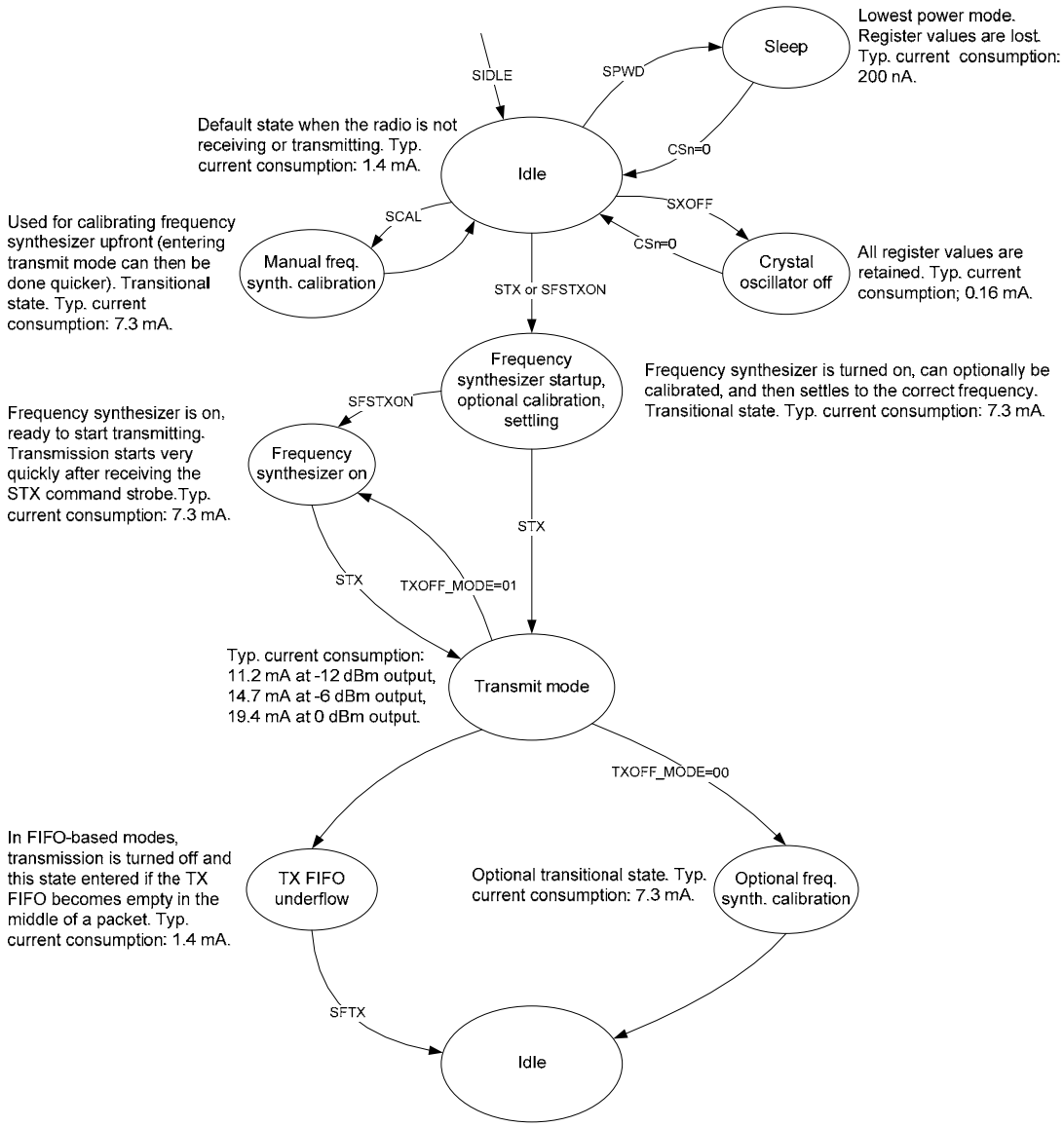

Figure 4: Simplified State Diagram with Typical Current Consumption

9 Configuration Software

CC2550 can be configured using the SmartRF® Studio software ([4]). The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF® Studio user interface for ***CC2550*** is shown in Figure 5.

After chip reset, all the registers have default values as shown in the tables in Section 28. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

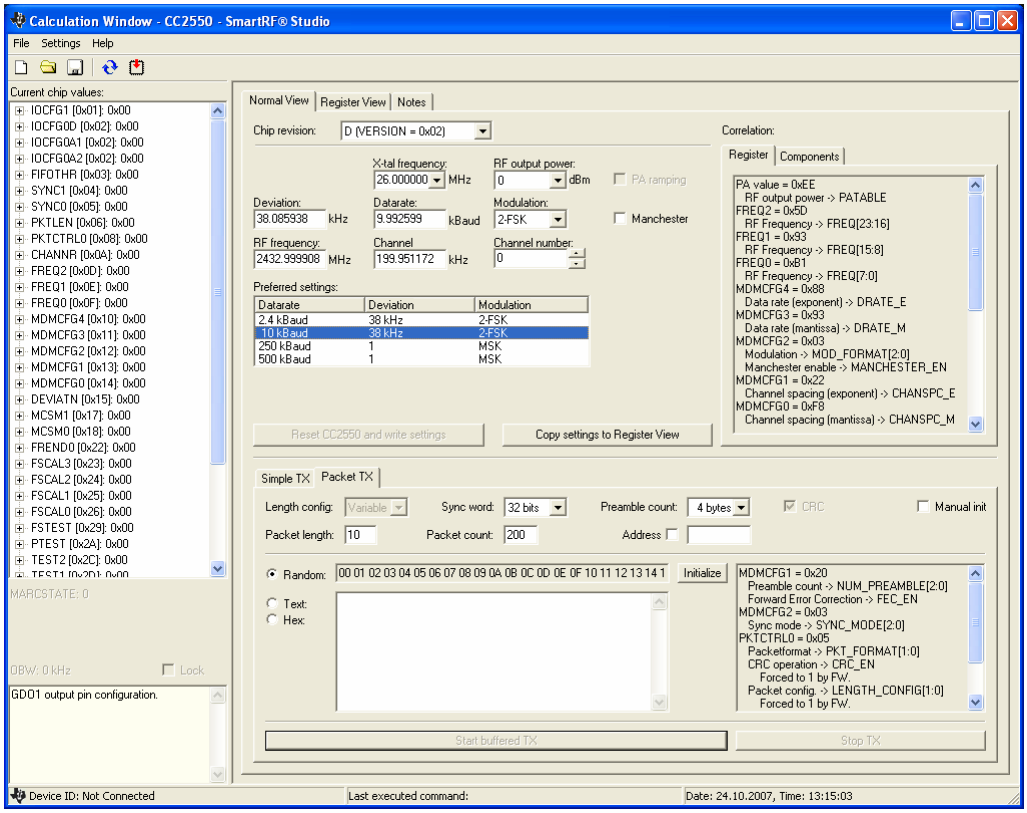

Figure 5: SmartRF® Studio [4] User Interface

10 4-wire Serial Configuration and Data Interface

CC2550 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where ***CC2550*** is the slave. This interface is also used to write buffered data. All transfer on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R/W bit, a burst access bit (B), and a 6-bit address (A_5 – A_0).

The CSn pin must be kept low during transfers on the SPI bus. If CSn goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 6 with reference to Table 14.

When CSn is pulled low, the MCU must wait until ***CC2500*** SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

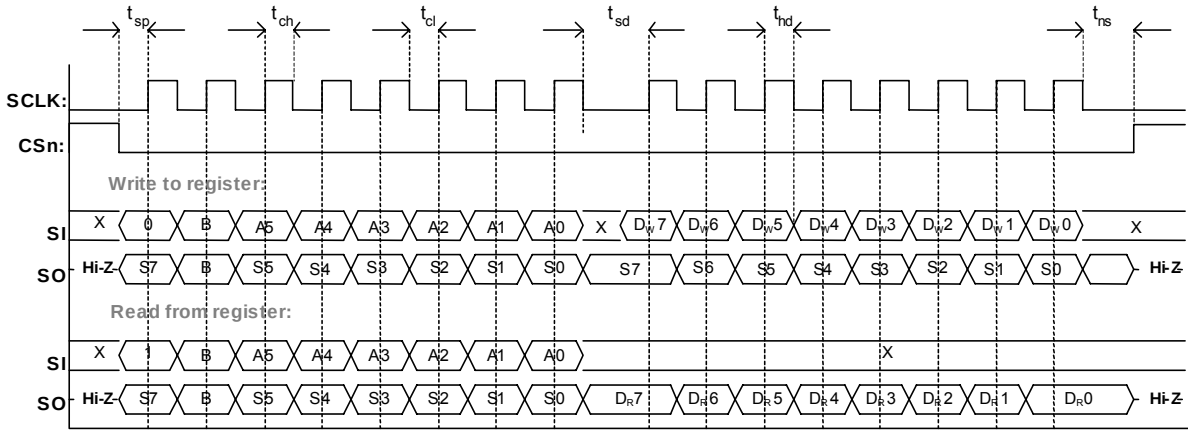

Figure 6: Configuration Registers Write and Read Operations

Parameter	Description		Min	Max	Units
f_{SCLK}	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).		-	10	MHz
	SCLK frequency, single access No delay between address and data byte			9	MHz
	SCLK frequency, burst access No delay between address and data byte, or between data bytes			6.5	MHz
$t_{sp,pd}$	CSn low to positive edge on SCLK, in power-down mode		150	-	µs
t_{sp}	CSn low to positive edge on SCLK, in active mode		20	-	ns
t_{ch}	Clock high		50	-	ns
t_{cl}	Clock low		50	-	ns
t_{rise}	Clock rise time		-	5	ns
t_{fall}	Clock fall time		-	5	ns
t_{sd}	Setup data (negative SCLK edge) to positive edge on SCLK (t_{sd} applies between address and data bytes, and between data bytes)	Single access	55	-	ns
		Burst access	76	-	ns
t_{hd}	Hold data after positive edge on SCLK		20	-	ns
t_{ns}	Negative edge on SCLK to CSn high		20	-	ns

Table 14: SPI Interface Timing Requirements

Note: The minimum $t_{sp,pd}$ figure in Table 14 can be used in cases where the user does not read the CHIP_RDYn signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150 us in Table 14 is the crystal oscillator start-up time measured on CC2550EM reference design ([3]) using crystal AT-41CD2 from NDK.

10.1 Chip Status Byte

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the ***CC2550*** on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the CHIP_RDYn signal; this signal must go low before the first positive edge of SCLK. The CHIP_RDYn signal indicates that the crystal is running.

Bits 6, 5, and 4 comprise the STATE value. This value reflects the state of the chip. The XOSC and power to the digital core is on in the IDLE state, but all other modules are in power

down. The frequency and channel configuration should only be updated when the chip is in this state. The TX state is active when the chip is transmitting.

The last four bits (3:0) in the status byte contains FIFO_BYTES_AVAILABLE. For write operations (the R/W bit in the header byte is set to 0), the FIFO_BYTES_AVAILABLE field contains the number of bytes that can be written to the TX FIFO. When FIFO_BYTES_AVAILABLE=15, 15 or more bytes are available/free.

Table 15 gives a status byte summary.

Bits	Name	Description
7	CHIP_RDYn	Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.
6:4	STATE[2:0]	Indicates the current main state machine mode
3:0	FIFO_BYTES_AVAILABLE[3:0]	The number of free bytes in the TX FIFO (the R/W bit in the header byte must be set to 0)

Value	State	Description
000	IDLE	Idle state (Also reported for some transitional states instead of SETTLING or CALIBRATE)
001	Not used	
010	TX	Transmit mode
011	FSTXON	Frequency synthesizer is on, ready to start transmitting
100	CALIBRATE	Frequency synthesizer calibration is running
101	SETTLING	PLL is settling
110	Not used	
111	TXFIFO_UNDERFLOW	TX FIFO has underflowed. Acknowledge with SFTX

Table 15: Status Byte Summary

10.2 Registers Access

The configuration registers on the ***CC2550*** are located on SPI addresses from 0x00 to 0x2E. Table 24 on page 39 lists all configuration registers. It is highly recommended to use SmartRF® Studio [4] to generate optimum register settings. The detailed description of each register is found in Section 28.1, starting on page 41. All configuration registers can be both written to and read. The R/W bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit (B) in the header byte. The address bits (A_5 – A_0) sets the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30-0x3D, the burst bit is used to select between status registers, burst bit is one, and command strobes, burst bit is zero (see Section 10.4 below). Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

10.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated

by the radio hardware (e.g. MARCSTATE or TXBYTES), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from TXBYTES being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the *CC2550* Errata Note [1] for more details.

10.4 Command Strobes

Command strobes may be viewed as single byte instructions to *CC2550*. By addressing a command strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable transmit mode, flush the TX FIFO etc. The 9 command strobes are listed in Table 23 on page 38.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the R/W bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an SRES strobe is being issued, one will have to wait for SO to go low again before the next header byte can be issued as shown in Figure 7. The command strobes are executed immediately, with the exception of the SPWD and the SXOFF strobes that are executed when CSn goes high.

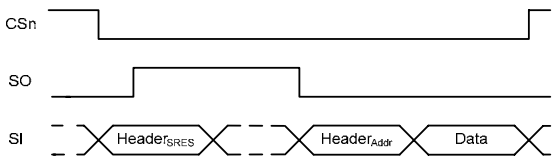

Figure 7: SRES Command Strobe

10.5 FIFO Access

The 64-byte TX FIFO is accessed through the 0x3F address and is write-only.

The burst bit is used to determine if the FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte a new header byte is expected; hence, CSn can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the FIFO:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO

When writing to the TX FIFO, the status byte (see Section 10.1) is output for each new data byte on SO, as shown in Figure 6. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free *before* writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted on SI, the status byte received concurrently on SO will indicate that one byte is free in the TX FIFO.

The TX FIFO may be flushed by issuing a SFTX command strobe. A SFTX command strobe can only be issued in the IDLE or TX_UNDERFLOW states. The TX FIFO is flushed when going to the SLEEP state.

Figure 8 gives a brief overview of different register access types possible.

10.6 PATABLE Access

The 0x3E address is used to access the PATABLE, which is used for selecting PA power control settings. The PATABLE is an 8-byte table, but not all entries into this table are used. The entries to use are selected by the 3-bit value FREND0.PA_POWER.

- When using 2-FSK, GFSK, or MSK modulation only the first entry into this table is used (index 0).
- When using OOK modulation the first two entries into this table are used (index 0 and index 1).

Since the PATABLE is an 8-byte table, the table is written and read from the lowest setting (0) to the highest (7), one byte at a time. An index counter is used to control the access to the table. This counter is incremented each time a byte is read or written to the table, and set to the lowest index when CSn is high. When the highest value is reached the counter restarts at 0.

The access to the PATABLE is either single byte or burst access depending on the burst bit. When using burst access the index counter will count up; when reaching 7 the counter will restart at 0. The R/W bit controls whether the access is a write access (R/W=0) or a read access (R/W=1).

If one byte is written to the PATABLE and this value is to be read out then CSn must be set high before the read access in order to set the index counter back to zero.

Note that the content of the PATABLE is lost when entering the SLEEP state.

See Section 21 on page 30 for output power programming details.

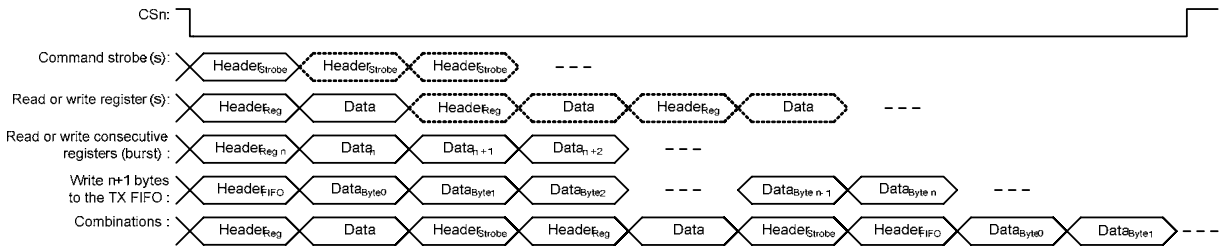

Figure 8: Register Access Types

11 Microcontroller Interface and Pin Configuration

In a typical system, ***CC2550*** will interface to a microcontroller. This microcontroller must be able to:

- Program ***CC2550*** into different modes
- Write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn)

11.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 14 on page 14.

11.2 General Control and Status Pins

The ***CC2550*** has one dedicated configurable pin (GDO0) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See Section 25 page 33 for more details of the signals that can be programmed. GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

The GDO0 pin can also be used for an on-chip analog temperature sensor. By measuring the voltage on the GDO0 pin with an external ADC, the temperature can be calculated. Specifications for the temperature sensor are found in Section 4.5 on page 8.

With default PTEST register setting (0x7F) the temperature sensor output is only available when the frequency synthesizer is enabled (e.g. the MANCAL, FSTXON and TX states). It is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state. Before leaving the IDLE state, the PTEST register should be restored to its default value (0x7F).

12 Data Rate Programming

The data rate used when transmitting is programmed by the MDMCFG3.DRATE_M and the MDMCFG4.DRATE_E configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE_M) \cdot 2^{DRATE_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE_E = \left\lfloor \log_2 \left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}} \right) \right\rfloor$$

$$DRATE_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE_E}} - 256$$

If DRATE_M is rounded to the nearest integer and becomes 256, increment DRATE_E and use DRATE_M=0.

The data rate can be set from 1.2 kBaud to 500 kBaud with a minimum step size of:

Data Rate Start [kBaud]	Typical Data Rate [kBaud]	Data Rate Stop [kBaud]	Data Rate Step Size [kBaud]
0.8	1.2/2.4	3.17	0.0062
3.17	4.8	6.35	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.4	0.0496
25.4	38.4	50.8	0.0992
50.8	76.8	101.6	0.1984
101.6	153.6	203.1	0.3967
203.1	250	406.3	0.7935
406.3	500	500	1.5869

Table 16: Data Rate Step Size

13 Packet Handling Hardware Support

The *CC2550* has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler can be configured to add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes
- A two byte synchronization (sync) word. Can be duplicated to give a 4-byte sync word. It is not possible to only insert preamble or only insert a sync word.
- A CRC checksum computed over the data field.

In a system where *CC2550* is used as the transmitter and *CC2500* as the receiver, the recommended setting is 4-byte preamble and 4-byte sync word, except for 500 kBaud data rate where the recommended preamble length is 8 bytes.

In addition, the following can be implemented on the data field and the optional 2-byte CRC checksum:

- Whitening of the data with a PN9 sequence.
- Forward error correction by the use of interleaving and coding of the data (convolutional coding).

Note that register fields that control the packet handling features should only be altered when *CC2550* is in the IDLE state.

13.1 Data whitening

From a radio perspective, the ideal over the air data are random and DC free. This results in the smoothest power distribution over the occupied bandwidth. This also gives the regulation loops in the receiver uniform operation conditions (no data dependencies).

Real world data often contain long sequences of zeros and ones. Performance can then be improved by whitening the data before transmitting, and de-whitening the data in the receiver. With *CC2550*, in combination with a *CC2500* at the receiver end, this can be done automatically by setting PKTCTRL0

.WHITE_DATA=1. All data, except the preamble and the sync word, are then XOR-ed with a 9-bit pseudo-random (PN9) sequence before being transmitted as shown in Figure 9. At the receiver end, the data are XOR-ed with the same pseudo-random sequence. This way, the whitening is reversed, and the original data appear in the receiver. The PN9 sequence is reset to all 1's.

Data whitening can only be used when PKTCTRL0.CC2400_EN=0 (default).

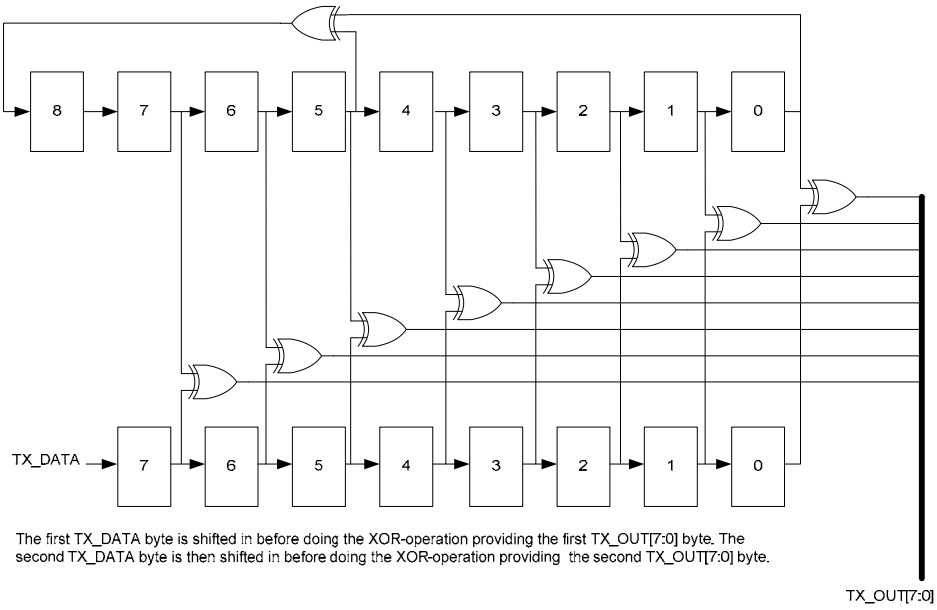

Figure 9: Data Whitening in TX Mode

13.2 Packet Format

The format of the data packet can be configured and consists of the following items (see Figure 10):

- Preamble
- Synchronization word
- Optional length byte
- Optional address byte
- Payload
- Optional 2 byte CRC

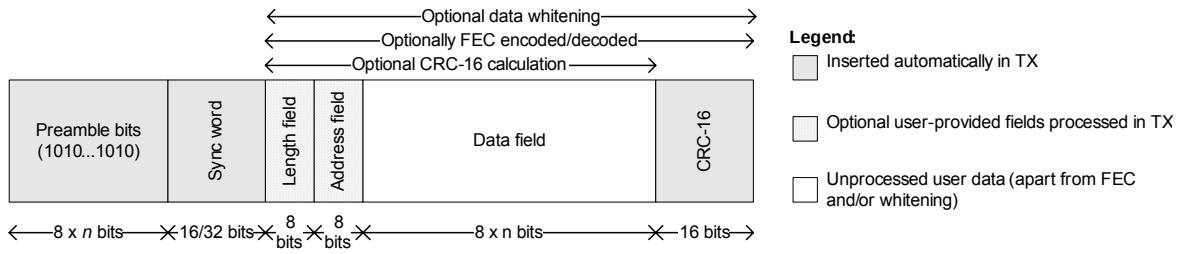

Figure 10: Packet Format

The preamble pattern is an alternating sequence of ones and zeros (101010101…). The minimum length of the preamble is programmable. When enabling TX, the modulator will start transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator will send the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator will continue to send preamble bytes until the first byte is written to the TX FIFO. The modulator will then send the

sync word and then the data bytes. The number of preamble bytes is programmed with the MDMCFG1.NUM_PREAMBLE value.

The synchronization word is a two-byte value set in the SYNC1 and SYNC0 registers. A one-byte sync word can be emulated by setting the SYNC1 value to the preamble pattern. It is also possible to emulate a 32 bit sync word by using MDMCFG2.SYNC_MODE=3 or 7. The sync word will then be repeated twice.

CC2550 supports both fixed packet length protocols and variable packet length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting PKTCTRL0.LENGTH_CONFIG=0. The desired packet length is set by the PKTLEN register.

In variable packet length mode, PKTCTRL0.LENGTH_CONFIG=1, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional automatic CRC.

With PKTCTRL0.LENGTH_CONFIG=2, the packet length is set to infinite and transmission will continue until turned off manually. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by ***CC2550***. One should make sure that TX mode is not turned off during the transmission of the first half of any byte. Refer to the ***CC2550*** Errata Notes [1] for more details.

Note that the minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

13.2.1 Packet Length > 255

Reprogramming the packet automation control register, PCKCTRL0, during TX mode opens the possibility to transmit packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode (PCKCTRL0.LENGTH_CONFIG=2) must be active. The PKTLEN register is set to mod(length, 256). When less than 256 bytes remains of the packet the MCU disables infinite packet length mode and activates fixed packet length mode. When the internal byte counter reaches the PKTLEN value, the transmission ends the radio enters the state determined by TXOFF_MODE). Automatic CRC appending can be used (by setting PKTCTRL0.CRC_EN=1).

When for example a 600-byte packet is to be transmitted, the MCU should do the following (see also Figure 11):

- Set PKTCTRL0.LENGTH_CONFIG=2.
- Pre-program the PKTLEN register to mod(600,256)=88.
- Transmit at least 345 bytes (600 – 255), for example by filling the 64-byte TX FIFO six times (384 bytes transmitted).
- Set PKTCTRL0.LENGTH_CONFIG=0.
- The transmission ends when the packet counter reaches 88. A total of 600 bytes are transmitted.

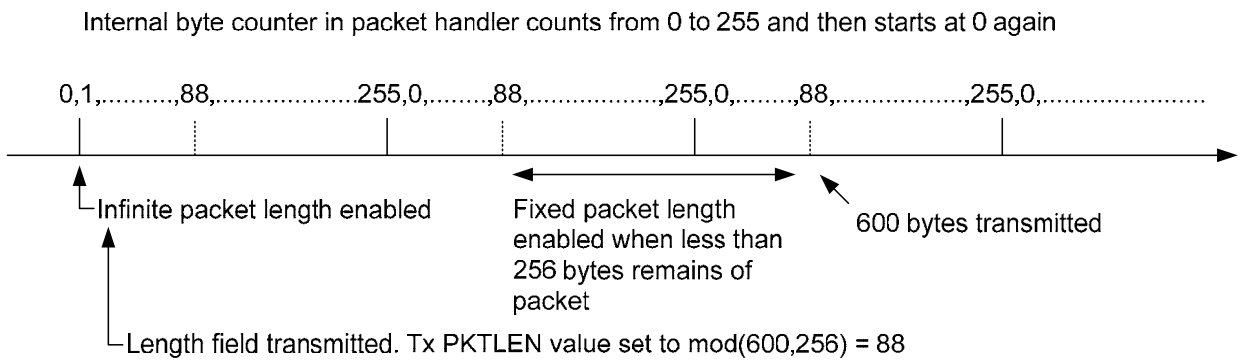

Figure 11: Packet Length > 255

13.3 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If fixed packet length is enabled, then the first byte written to the TX FIFO is interpreted as the destination address, if this feature is enabled in the device that receives the packet.

The modulator will first send the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator will send the two-byte (optionally 4-byte) sync word and then the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO and the result is sent as two extra bytes at the end of the payload data. If the TX FIFO runs empty before the complete packet has been transmitted, the radio will enter TXFIFO_UNDERFLOW state. The only way to exit this state is by issuing an `SFTX` strobe. Writing to the TX FIFO after it has underflowed will not restart TX mode.

If whitening is enabled, everything following the sync words will be whitened. This is done before the optional FEC/Interleaver stage. Whitening is enabled by setting `PKTCTRL0.WHITE_DATA=1`.

If FEC/Interleaving is enabled, everything following the sync words will be scrambled by the interleaver, and FEC encoded before being modulated. FEC is enabled by setting `MDMCFG.FEC_EN=1`.

13.4 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been transmitted. Additionally, for packets longer than 64 bytes the TX FIFO needs to be refilled while in TX. This means that the MCU needs to know the number of bytes that can be written to TX FIFO. There are two possible solutions to get the necessary status information:

a) Interrupt driven solution

It is possible to use one of the `GDO` pins to give an interrupt when a sync word has been transmitted and/or when a complete packet has been transmitted (`IOCFGx=0x06`). In addition, there are 2 configurations for the `IOCFGx` register that are associated with the TX FIFO (`IOCFGx=0x02` and `IOCFG=0x03`) that can be used as interrupt sources to provide information on how many bytes are in the TX FIFO. See Table 22.

b) SPI polling

The `PKTSTATUS` register can be polled at a given rate to get information about the current `GDO0` value. The `TXBYTES` register can be polled at a given rate to get information about the number of bytes in the TX FIFO. Alternatively, the number of bytes in the TX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus. This only valid when R/W = 0.

As explained in Section 10.3 and the ***CC2550*** Errata Notes [1], when using SPI polling there is a small, but finite, probability that a single read from registers `PKTSTATUS` and `TXBYTES` is being corrupt. The same is the case when reading the chip status byte. It is therefore recommended to employ an interrupt driven solution.

Refer to the TI website for SW examples ([5] and [6]).

14 Modulation Formats

CC2550 supports amplitude, frequency and phase shift modulation formats. The desired modulation format is set in the `MDMCFG2.MOD_FORMAT` register.

Optionally, the data stream can be Manchester coded by the modulator. This option is enabled by setting `MDMCFG2.MANCHESTER_EN=1`. Manchester encoding is not supported at the same time as using the FEC/Interleaver option.

14.1 Frequency Shift Keying

2-FSK can optionally be shaped by a Gaussian filter with BT=1, producing a GFSK modulated signal.

The frequency deviation is programmed with the `DEVIATION_M` and `DEVIATION_E` values in the `DEVIATN` register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION_M) \cdot 2^{DEVIATION_E}$$

The symbol encoding is shown in Table 17.

Format	Symbol	Coding
2-FSK\GFSK	'0'	– Deviation
	'1'	+ Deviation

Table 17: Symbol Encoding for 2-FSK/GFSK Modulation

14.2 Minimum Shift Keying

When using MSK[1], the complete transmission (preamble, sync word and payload) will be MSK modulated.

Phase shifts are performed with a constant transition time.

The fraction of a symbol period used to change the phase can be modified with the `DEVIATN.DEVIATION_M` setting. This is equivalent to changing the shaping of the symbol.

The MSK modulation format implemented in ***CC2550*** inverts the sync word and data compared to e.g. signal generators.

14.3 Amplitude Modulation

The supported amplitude modulation On-Off Keying (OOK) simply turns on or off the PA to modulate 1 and 0 respectively.

[1] Identical to offset QPSK with half-sine shaping (data coding may differ)

15 Forward Error Correction with Interleaving

15.1 Forward Error Correction (FEC)

CC2550 has built in support for Forward Error Correction (FEC) that can be used with ***CC2500*** [9] at the receiver end. To enable this option, set `MDMCFG1.FEC_EN=1`. FEC is employed on the data field and CRC word in order to reduce the gross bit error rate when operating near the sensitivity limit. Redundancy is added to the transmitted data in such a way that the ***CC2500*** [9] can restore the original data in the presence of some bit errors.

The use of FEC allows correct reception at a lower SNR, thus extending communication range. Alternatively, for a given SNR, using FEC decreases the bit error rate (BER). As the packet error rate (PER) is related to BER by:

$$PER = 1 - (1 - BER)^{packet_length}$$

a lower BER can be used to allow longer packets, or a higher percentage of packets of a given length, to be transmitted successfully. Finally, in realistic ISM radio environments, transient and time-varying phenomena will produce occasional errors even in otherwise good reception conditions. FEC will mask such errors and, combined with interleaving of the coded data, even correct relatively long periods of faulty reception (burst errors).

The FEC scheme adopted for ***CC2550*** is convolutional coding, in which *n* bits are generated based on *k* input bits and the *m* most recent input bits, forming a code stream able to withstand a certain number of bit errors between each coding state (the *m*-bit window).

The convolutional coder is a rate 1/2 code with a constraint length of m=4. The coder codes one input bit and produces two output bits; hence, the effective data rate is halved. I.e. to transmit at the same effective data rate when using FEC, it is necessary to use twice as high over-the-air data rate. I.e. to transmit at the same effective data rate when using FEC, it is necessary to use twice as high over-the-air data rate. This will require a higher ***CC2500*** [9] receiver bandwidth, and thus reduced sensitivity. In other words, the improved reception by using FEC and the degraded

sensitivity from a higher receiver bandwidth will be counteracting factors.

15.2 Interleaving

Data received through radio channels will often experience burst errors due to interference and time-varying signal strengths. In order to increase the robustness to errors spanning multiple bits, interleaving is used when FEC is enabled. After de-interleaving on the receiver side, a continuous span of errors in the received stream will become single errors spread apart.

CC2550 employs matrix interleaving, which is illustrated in Figure 12. The on-chip interleaving buffer is a 4 x 4 matrix. The data bits from the rate ½ convolutional coder are written into the rows of the matrix, whereas the bit sequence to be transmitted is read from the columns of the matrix. Conversely, in a ***CC2500*** [9] receiver, the received symbols are written into the rows of the matrix, whereas the data passed onto the convolutional decoder is read from the columns of the matrix.

When FEC and interleaving is used at least one extra byte is required for trellis termination. In addition, the amount of data transmitted over the air must be a multiple of the size of the interleaver buffer (two bytes). The packet control hardware therefore automatically inserts one or two extra bytes at the end of the packet, so that the total length of the data to be interleaved is an even number. Note that these extra bytes are invisible to the user, as they are removed before the received packet enters the RX FIFO in a ***CC2500***[9].

When FEC and interleaving is used the minimum data payload is 2 bytes.

Note that for the ***CC2500***[9] transceiver FEC is only supported in fixed packet length mode (`PKTCTRL0.LENGTH_CONFIG=0`).

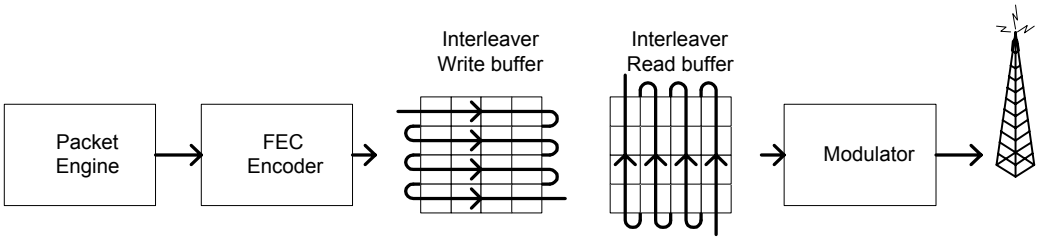

Figure 12: General Principle of Matrix Interleaving

16 Radio Control

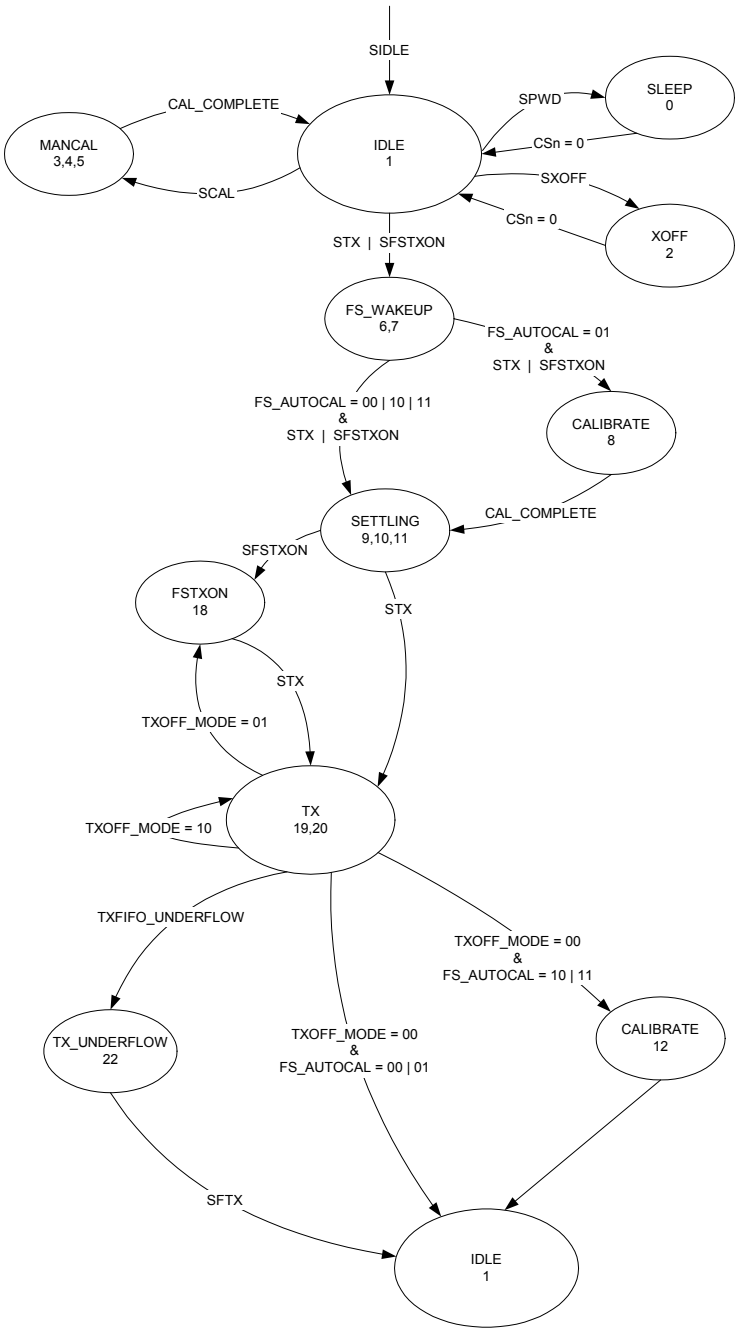

Figure 13: Complete Radio Control State Diagram

CC2550 has a built-in state machine that is used to switch between different operation states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 4 on page 13. The complete radio control state diagram is shown in Figure 13. The numbers refer to the state number readable in the `MARCSTATE` status register. This register is primarily for test purposes.

16.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. One of the following two

sequences must be followed: Automatic power-on reset (POR) or manual reset.

16.1.1 Automatic POR

A power-on reset circuit is included in the ***CC2550***. The minimum requirements stated in Section 4.7 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when CHIP_RDYn goes low. CHIP_RDYn is observed on the SO pin after CSn is pulled low. See Section 10.1 for more details on CHIP_RDYn.

When the ***CC2550*** reset is completed the chip will be in the IDLE state and the crystal oscillator will be running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed the SO pin will first go high, indicating that the crystal oscillator is not stabilized, before going low as shown in Figure 14.

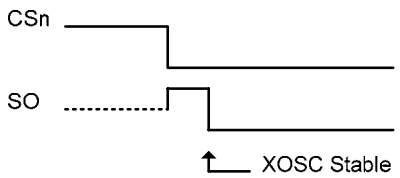

Figure 14: Power-On Reset

16.1.2 Manual Reset

The other global reset possibility on ***CC2550*** is the SRES command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see Figure 15):

- Strobe CSn low / high.
- Hold CSn high for at least 40 µs relative to pulling CSn low
- Pull CSn low and wait for SO to go low (CHIP_RDYn).
- Issue the SRES strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

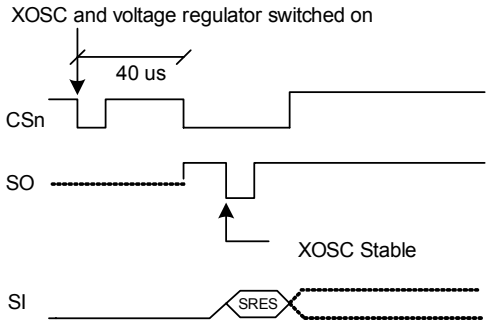

Figure 15: Power-On Reset with SRES

Note that the above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the ***CC2550*** after this, it is only necessary to issue an SRES command strobe.

16.2 Crystal Control

The crystal oscillator is automatically turned on when CSn goes low. It will be turned off if the SXOFF or SPWD command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from the IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used; as described in Section 10.1 on page 15.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in Section 4.3 on page 7.

16.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state, which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a SPWD command strobe has been sent on the SPI interface. The chip is now in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

All ***CC2550*** register values (with the exception of the MCSM0.PO_TIMEOUT field) are lost in

the SLEEP state. After the chip gets back to the IDLE state, the registers will have default (reset) contents and must be reprogrammed over the SPI interface.

16.4 TX Mode

Transmit mode is activated by the MCU by using the STX command strobe.

The frequency synthesizer must be calibrated regularly. ***CC2550*** has one manual calibration option (using the SCAL strobe), and three automatic calibration options, controlled by the MCSM0.FS_AUTOCAL setting:

- Calibrate when going from IDLE to TX (or FSTXON)
- Calibrate when going from TX to IDLE automatically
- Calibrate every fourth time when going from TX to IDLE automatically

If the radio goes from TX to IDLE by issuing an SIDLE strobe, calibration will not be performed. The calibration takes a constant number of XOSC cycles (see Table 18 for timing details).

After activating TX mode, the chip will remain in the TX state until the current packet has been successfully transmitted. Then the state will change as indicated by the MCSM1.TXOFF_MODE setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with STX.
- TX: Start sending preambles

The SIDLE command strobe can always be used to force the radio controller to go to the IDLE state.

16.5 Timing

The radio controller controls most timing in ***CC2550***, such as synthesizer calibration and PLL lock time. Timing from IDLE to TX is constant, dependent on the auto calibration setting. The calibration time is constant 18739 clock periods. Table 18 shows timing in crystal clock cycles for key state transitions.

Power on time and XOSC start-up times are variable, but within the limits stated in Table 6.

Note that in a frequency hopping spread spectrum or a multi-channel protocol the calibration time can be reduced from 721 µs to approximately 150 µs. This is explained in Section 27.2.

Description	XOSC Periods	26 MHz Crystal
Idle to TX/FSTXON, no calibration	2298	88.4 µs
Idle to TX/FSTXON, with calibration	~21037	809 µs
TX to IDLE, no calibration	2	0.1 µs
TX to IDLE, including calibration	~18739	721 µs
Manual calibration	~18739	721 µs

Table 18: State Transition Timing

17 TX FIFO

The ***CC2550*** contains a 64 byte FIFO for data to be transmitted. The SPI interface is used for writing to the TX FIFO. Section 10.5 contains details on the SPI FIFO access. The FIFO controller will detect underflow in the TX FIFO.

When writing to the TX FIFO it is the responsibility of the MCU to avoid TX FIFO overflow. A TX FIFO overflow will result in an error in the TX FIFO content.

The chip status byte that is available on the S0 pin while transferring the SPI address contains the fill grade of the TX FIFO if the R/W bit in the header byte is 0. Section 10.1 on page 15 contains more details on this.

The number of bytes in the TX FIFO can also be read from the TXBYTES.NUM_TXBYTES status register.

The 4-bit FIFOTHR.FIFO_THR setting is used to program threshold points in the FIFO. Table 19 lists the 16 FIFO_THR settings and the corresponding thresholds for the TX FIFO.

A signal will assert when the number of bytes in the FIFO is equal to or higher than the programmed threshold. The signal can be

viewed on the GDO pins (see Section 25 on page 33).

Figure 17 shows the number of bytes in the TX FIFO when the threshold flag toggles, in the case of FIFO_THR=13. Figure 16 shows the signal as the FIFO is filled above the threshold, and then drained below.

FIFO_THR	Bytes in TX FIFO
0 (0000)	61
1 (0001)	57
2 (0010)	53
3 (0011)	49
4 (0100)	45
5 (0101)	41
6 (0110)	37
7 (0111)	33
8 (1000)	29
9 (1001)	25
10 (1010)	21
11 (1011)	17
12 (1100)	13
13 (1101)	9
14 (1110)	5
15 (1111)	1

Table 19: FIFO_THR Settings and the Corresponding FIFO Thresholds

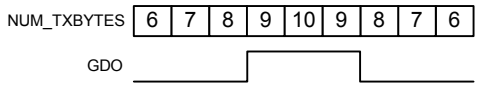

Figure 16: FIFO_THR=13 vs. Number of Bytes in FIFO (GDOx_CFG=0x02)

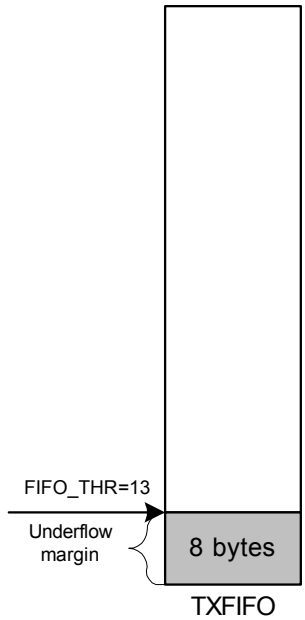

Figure 17: Example of FIFO at Threshold

18 Frequency Programming

The frequency programming in ***CC2550*** is designed to minimize the programming needed in a channel-oriented system.

To set up a system with channel numbers, the desired channel spacing is programmed with the MDMCFG0.CHANSPC_M and MDMCFG1.CHANSPC_E registers. The channel spacing registers are mantissa and exponent respectively.

The base or start frequency is set by the 24 bit frequency word located in the FREQ2, FREQ1 and FREQ0 registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, CHANNR.CHAN, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot \left(FREQ + CHAN \cdot \left(\left(256 + CHANSPC_M\right) \cdot 2^{CHANSPC_E-2}\right)\right)$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get e.g. 1 MHz channel spacing one solution is to use 333 kHz channel spacing and select each third channel in CHANNR.CHAN.

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency programming should only be updated when the radio is in the IDLE state.

19 VCO

The VCO is completely integrated on-chip.

19.1 VCO and PLL Self-Calibration

The VCO characteristics will vary with temperature and supply voltage changes, as well as the desired operating frequency. In order to ensure reliable operation, ***CC2550*** includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 18 on page 27.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the MCSM0.FS_AUTOCAL register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

The calibration values are not maintained in sleep mode. Therefore, the ***CC2550*** must be recalibrated after reprogramming the configuration registers when the chip has been in the SLEEP state.

To check that the PLL is in lock the user can program register IOCFGx.GDOx_CFG to 0x0A and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0 or 1). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F. Refer also to the ***CC2550*** Errata Notes [1]. For more robust operation the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

20 Voltage Regulators

CC2550 contains several on-chip linear voltage regulators, which generate the supply voltage needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 1 and Table 11 are not exceeded. The voltage regulator for the digital core requires one external decoupling capacitor.

Setting the CSn pin low turns on the voltage regulator to the digital core and starts the crystal oscillator. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in Table 14).

If the chip is programmed to enter power-down mode, (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator output should only be used for driving the ***CC2550***.

21 Output Power Programming

The RF output power level from the device has two levels of programmability, as illustrated in Figure 18.

The RF output power level from the device is programmed through the PATABLE register.

- If 2-FSK, GFSK or MSK modulation is used the desired output power is programmed to index 0 in the PATABLE register (PATABLE(0)[7:0]). The 3-bit FREND0.PA_POWER value shall be set to 0 (reset default value).
- If OOK modulation is used the desired output power for the logic 0 and logic 1 power levels are programmed to index 0 and index 1 in the PATABLE register respectively (PATABLE(0)[7:0] and PATABLE(1)[7:0]). The 3-bit FREND0.PA_POWER value shall be set to 1.

Table 20 contains recommended PATABLE settings for various output levels and frequency bands. See Section 10.6 on page 17 for PATABLE programming details. The SmartRF® Studio software [4] should be used to obtain optimum PATABLE settings for various output powers.

PATABLE must be programmed in burst mode if writing to other entries than PATABLE(0) (OOK modulation). Note that all content of the PATABLE is lost when entering the SLEEP state.

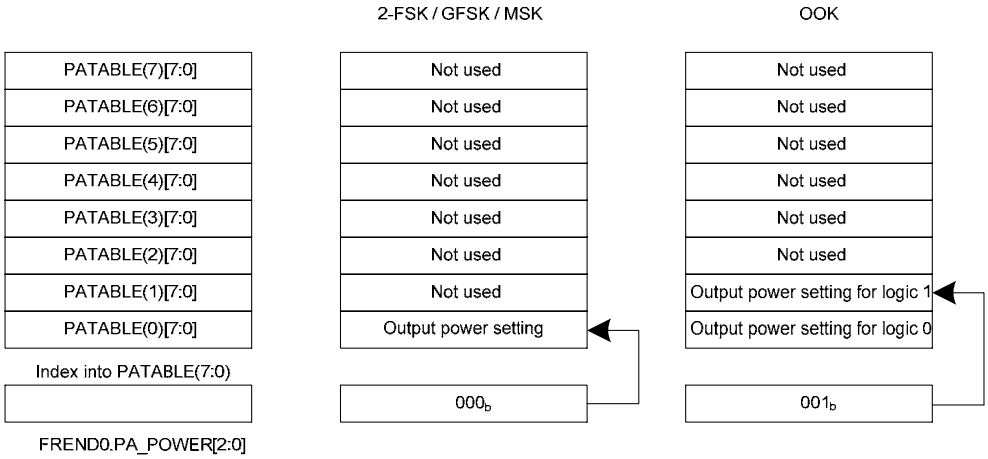

Figure 18: PA_POWER and PATABLE

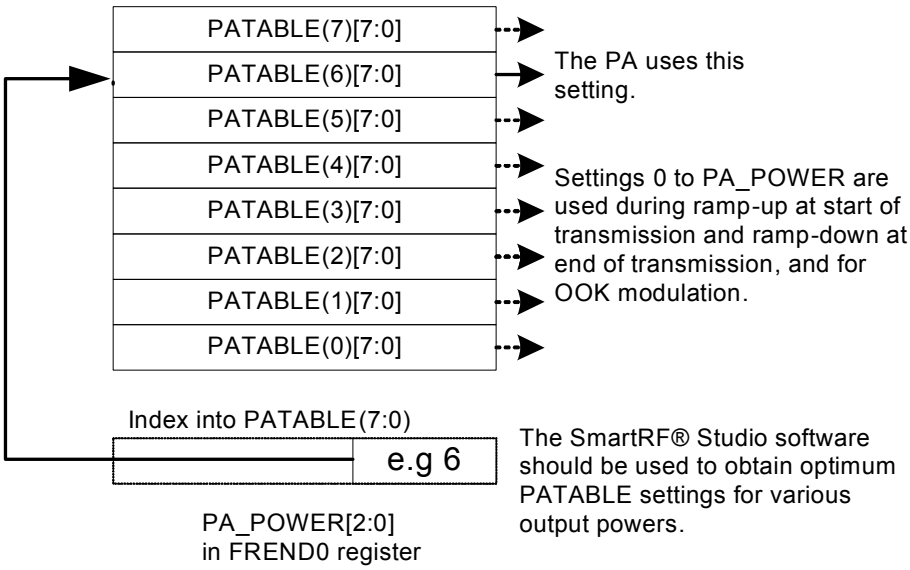

Figure 19: PA_POWER and PATABLE

Output Power, Typical, +25°C, 3.0 V [dBm]	PATABLE Value	Current Consumption, Typical [mA]
(–55 or less)	0x00	8.0
–30	0x44	9.3
–28	0x41	9.2
–26	0x43	9.7
–24	0x84	9.8
–22	0x82	9.7
–20	0x47	10.0
–18	0xC8	11.6
–16	0x85	10.2
–14	0x59	11.6
–12	0xC6	11.2
–10	0x97	12.0
–8	0xD6	12.9
–6	0x7F	14.7
–4	0xA9	16.2
–2	0xBF	18.1
0	0xEE	19.4
1	0xFF	21.3

Table 20: Optimum PATABLE Settings for Various Output Power Levels

22 Crystal Oscillator

A crystal in the frequency range 26-27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C51 and C71) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{51}} + \frac{1}{C_{71}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator circuit is shown in Figure 20. Typical component values for different values of C_L are given in Table 21.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see Section 4.3 on page 7).

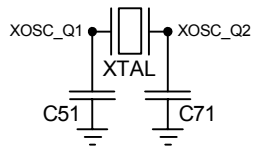

Figure 20: Crystal Oscillator Circuit

Component	C_L= 10 pF	C_L=13 pF	C_L=16 pF
C51	15 pF	22 pF	27 pF
C71	15 pF	22 pF	27 pF

Table 21: Crystal Oscillator Component Values

22.1 Reference Signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. When using a full-swing digital signal this capacitor can be omitted. The XOSC_Q2 line must be left un-connected. C51 and C71 can be omitted when using a reference signal

23 External RF Match

The balanced RF output of ***CC2550*** is designed for a simple, low-cost matching and balun network on the printed circuit board. A few passive external components ensure proper matching.

Although ***CC2550*** has a balanced RF output, the chip can be connected to a single-ended antenna with few external low cost capacitors and inductors.

The passive matching/filtering network connected to ***CC2550*** should have the following differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna:

$$Z_{out} = 80 + j74\ \Omega$$

To ensure optimal matching of the ***CC2550*** differential output it is highly recommended to follow the CC2550EM reference design [3] as closely as possible. Gerber files for the reference designs are available for download from the TI website.

24 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground. In the CC2550EM reference designs [3] 5 vias are placed inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using "tented" vias reduces the solder paste coverage below 100%.

See Figure 21 for top solder resist and top paste masks. See Figure 24 for recommended PCB layout for QLP 16 package.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line by separate vias. The best routing is from the power line to the decoupling capacitor and then to the ***CC2550*** supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane using a separate via. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components smaller than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC2500/2550DK Development Kit with a fully assembled CC2550EM Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The schematic, BOM and layout Gerber files are all available from the TI website [3].

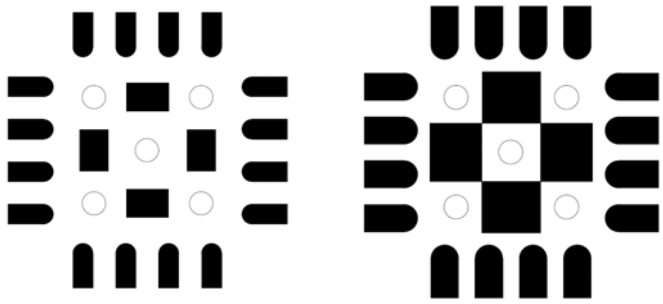

Figure 21: Left: Top Paste Mask. Right: Top Solder Resist Mask (negative). Circles are Vias.

25 General Purpose / Test Output Control Pins

The two digital output pins `GDO0` and `GDO1` are general control pins configured with `IOCFG0.GDO0_CFG` and `IOCFG1.GDO1_CFG` respectively. Table 22 shows the different signals that can be monitored on the `GDO` pins. These signals can be used as inputs to the MCU. `GDO1` is the same pin as the `SO` pin on the SPI interface, thus the output programmed on this pin will only be valid when `CSn` is high. The default value for `GDO1` is 3-stated, which is useful when the SPI interface is shared with other devices.

The default value for `GDO0` is a 135-141 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-

reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to IOCFG0.GDO0_CFG.

An on-chip analog temperature sensor is enabled by writing the value 128 (0x80) to the IOCFG0.GDO0_CFG register. The voltage on the GDO0 pin is then proportional to temperature. See Section 4.5 on page 8 for temperature sensor specifications.

In SLEEP mode, GDO1 will be hardwired to 1 and GDO0 will be high impedance.

GDOx_CFG[5:0]	Description	
0 (0x00)	Reserved – defined in the transceiver version.	
1 (0x01)	Reserved – defined in the transceiver version.	
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled at or above the TX FIFO threshold. De-asserts when the TX FIFO is below the same threshold.	
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below theTX FIFO threshold.	
4 (0x04)	Reserved – defined in the transceiver version.	
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.	
6 (0x06)	Asserts when sync word has been sent, and de-asserts at the end of the packet. The pin will also de-assert if the TX FIFO underflows.	
7 (0x07) to 9 (0x09)	Reserved	
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.	
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. In TX mode, data is sampled by *CC2550* on the rising edge of the serial clock when GDOx_INV=0.	
12 (0x0C) to 40 (0x28)	Reserved – used for test.	
41 (0x29)	CHIP_RDY	
42 (0x2A)	Reserved – used for test.	
43 (0x2B)	XOSC_STABLE	
44 (0x2C)	Reserved – used for test.	
45 (0x2D)	GDO0_Z_EN_N. When this output is 0, GDO0 is configured as input (for serial TX data).	
46 (0x2E)	High impedance (3-state)	
47 (0x2F)	HW to 0 (HW1 achieved with _INV signal). Can be used to control an external PA	
48 (0x30)	CLK_XOSC/1	Note: There are 2 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other GDO pin must be configured to a value less than 0x30. The GDO0 default value is CLK_XOSC/192.
49 (0x31)	CLK_XOSC/1.5	
50 (0x32)	CLK_XOSC/2	
51 (0x33)	CLK_XOSC/3	
52 (0x34)	CLK_XOSC/4	
53 (0x35)	CLK_XOSC/6	
54 (0x36)	CLK_XOSC/8	
55 (0x37)	CLK_XOSC/12	
56 (0x38)	CLK_XOSC/16	
57 (0x39)	CLK_XOSC/24	
58 (0x3A)	CLK_XOSC/32	
59 (0x3B)	CLK_XOSC/48	
60 (0x3C)	CLK_XOSC/64	
61 (0x3D)	CLK_XOSC/96	
62 (0x3E)	CLK_XOSC/128	
63 (0x3F)	CLK_XOSC/192	

Table 22: GDOx Signal Selection (x = 0 or 1)

26 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the *CC2550* to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller and simplify software development.

26.1 Asynchronous Operation

For backward compatibility with systems already using the asynchronous data transfer from other Chipcon products, asynchronous

transfer is also included in *CC2550*. When asynchronous transfer is enabled, several of the support mechanisms for the MCU that are included in *CC2550* will be disabled, such as packet handling hardware, buffering in the FIFO and so on. The asynchronous transfer mode does not allow the use of the data whitener, interleaver and FEC, and it is not possible to use Manchester encoding.

Note that MSK is not supported for asynchronous transfer.

Setting `PKTCTRL0.PKT_FORMAT` to 3 enables asynchronous serial mode.

The `GDO0` pin is used for data input (TX data).

The *CC2550* modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

26.2 Synchronous Serial Operation

Setting `PKTCTRL0.PKT_FORMAT` to 1 enables synchronous serial operation mode. In the synchronous mode, data is transferred on a two wire serial interface. The *CC2550* provides a clock that is used to set up new data on the data input line. Data input (TX data) is the `GDO0` pin. This pin will automatically be configured as an input when TX is active.

Preamble and sync word insertion may or may not be active, dependent on the sync mode set by the `MDMCFG3.SYNC_MODE`. If preamble and sync word is disabled, all other packet handler features and FEC should also be disabled. The MCU must then handle preamble and sync word insertion in software. If preamble and sync word insertion is left on, all packet handling features and FEC can be used.

When using the packet handling features in synchronous serial mode, the *CC2550* will insert the preamble and sync word and the MCU will only provide the data payload. This is equivalent to the recommended FIFO operation mode.

27 System considerations and Guidelines

27.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. The most important regulations for the 2.4 Ghz band are EN 300 440 and EN 300 328 (Europe), FCC CFR47 part 15.247 and 15.249 (USA), and ARIB STD-T66 (Japan). A summary of the most important aspects of these regulations can be found in Application Note AN032 [2].

Please note that compliance with regulations is dependent on complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

27.2 Frequency Hopping and Multi-Channel Systems

The 2.400 – 2.4835 GHz band is shared by many systems both in industrial, office and home environments. It is therefore recommended to use frequency hopping spread spectrum (FHSS) or a multi-channel protocol because the frequency diversity makes the system more robust with respect to interference from other systems operating in the same frequency band. FHSS also combats multipath fading.

CC2550 is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface. Using the packet handling support and data buffering is also beneficial in such systems as these features will significantly offload the host controller.

Charge pump current, VCO current and VCO capacitance array calibration data is required for each frequency when implementing frequency hopping for *CC2550*. There are 3 ways of obtaining the calibration data from the chip:

1) Frequency hopping with calibration for each hop. The PLL calibration time is approximately 720 µs. The blanking interval between each frequency hop is then approximately 810 us.

2) Fast frequency hopping without calibration for each hop can be done by calibrating each frequency at startup and saving the resulting

FSCAL3, FSCAL2 and FSCAL1 register values in MCU memory. Between each frequency hop, the calibration process can then be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency. The PLL turn on time is approximately 90 µs. The blanking interval between each frequency hop is then approximately 90 us. The VCO current calibration result is available in FSCAL2 and is not dependent on the RF frequency. Neither is the charge pump current calibration result available in FSCAL3. The same value can therefore be used for all frequencies.

3) Run calibration on a single frequency at startup. Next write 0 to FSCAL3[5:4] to disable the charge pump calibration. After writing to FSCAL3[5:4] strobe STX with MCSM0.FS_AUTOCAL=1 for each new frequency hop. That is, VCO current and VCO capacitance calibration is done but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from approximately 720 µs to approximately 150 µs. The blanking interval between each frequency hop is then approximately 240 us

There is a trade off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. Solution 3) gives approximately 570 µs smaller blanking interval than solution 1).

27.3 Wideband Modulation not Using Spread Spectrum

Digital modulation systems under FCC part 15.247 includes 2-FSK and GFSK modulation. A maximum peak output power of 1 W (+30 dBm) is allowed if the 6 dB bandwidth of the modulated signal exceeds 500 kHz. In addition, the peak power spectral density conducted to the antenna shall not be greater than +8 dBm in any 3 kHz band.

Operating at high data rates and high frequency separation, the ***CC2550*** is suited for systems targeting compliance with digital modulation systems as defined by FCC part 15.247. An external power amplifier is needed to increase the output above +1 dBm.

27.4 Data Burst Transmissions

The high maximum data rate of ***CC2550*** opens up for burst transmissions. A low average data rate link (e.g. 10 kBaud), can be realized using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (e.g. 500 kBaud) will reduce the time in TX mode, and hence also reduce the average current consumption significantly. Reducing the time in TX mode will reduce the likelihood of collisions with other systems, e.g. WLAN.

27.5 Continuous Transmissions

In data streaming applications the ***CC2550*** opens up for continuous transmissions at 500 kBaud effective data rate. As the modulation is done with a closed loop PLL, there is no limitation in the length of a transmission (open loop modulation used in some transceivers often prevents this kind of continuous data streaming and reduces the effective data rate.)

27.6 Spectrum Efficient Modulation

CC2500 also has the possibility to use Gaussian shaped 2-FSK (GFSK). This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. In 'true' 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift 'softer', the spectrum can be made significantly narrower. Thus, higher data rates can be transmitted in the same bandwidth using GFSK.

27.7 Low Cost Systems

A differential antenna will eliminate the need for a balun, and the DC biasing can be achieved in the antenna topology, see Figure 3. The CC25XX Folded Dipole reference design [7] contains schematics and layout files for a CC2500EM with a folded dipole PCB antenna. This design note can also be used with the ***CC2550***. Please see DN004 [8] for more details on this design.

A HC-49 type SMD crystal is used in the CC2550EM reference design. Note that the crystal package strongly influences the price. In a size constrained PCB design a smaller, but more expensive, crystal may be used.

27.8 Battery Operated Systems

In low power applications, the SLEEP state should be used when the ***CC2550*** is not active.

27.9 Increasing Output Power

In some applications it may be necessary to extend the link range by adding an external power amplifier.

The power amplifier should be inserted between the antenna and the balun as shown in Figure 22.

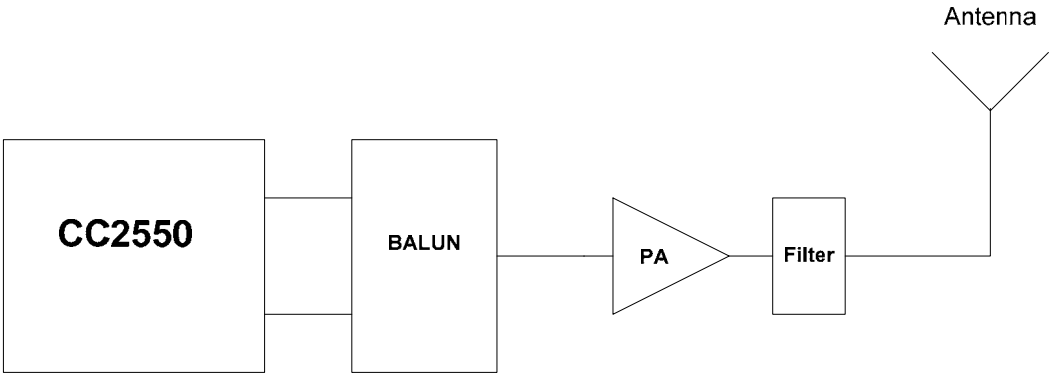

Figure 22: Block Diagram of *CC2550* Usage with External Power Amplifier

28 Configuration Registers

The configuration of ***CC2550*** is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF® Studio software [4]. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 9 command strobe registers, listed in Table 23. Accessing these registers will initiate the change of an internal state or mode. There are 29 normal 8-bit configuration registers, listed in Table 24. Some of these registers are for test purposes only, and need not be written for normal operation of ***CC2550***.

There are also 6 status registers, which are listed in Table 25. These registers, which are read-only, contain information about the status of ***CC2550***.

The TX FIFO is accessed through one 8-bit register. Only write operations are allowed to the TX FIFO.

During the header byte transfer and while writing data to a register or the TX FIFO, a status byte is returned on the `SO` line. This status byte is described in Table 15 on page 16.

Table 26 summarizes the SPI address space. Registers that are only defined in the ***CC2500*** transceiver are also listed. ***CC2500*** and ***CC2550*** are register compatible, but registers and fields only implemented in the transceiver always contain 0 in ***CC2550***. The address to use is given by adding the base address to the left and the burst and R/W bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

Note that all registers, (with the exception of the `MSCM0.PO_TIMEOUT` field) will lose their content in SLEEP mode.

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if `MCSM0.FS_AUTOCAL=1`).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off (enables quick start). `SCAL` can be strobed in IDLE state without setting manual calibration mode (`MCSM0.FS_AUTOCAL=0`).
0x35	STX	Enable TX. Perform calibration first if `MCSM0.FS_AUTOCAL=1`.
0x36	SIDLE	Exit TX and turn off frequency synthesizer.
0x39	SPWD	Enter power down mode when `CSn` goes high.
0x3B	SFTX	Flush the TX FIFO buffer.
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Table 23: Command Strobes

Address	Register	Description	Details on Page Number
0x01	IOCFG1	GDO1 output pin configuration	41
0x02	IOCFG0	GDO0 output pin configuration	41
0x03	FIFOTHR	FIFO threshold	41
0x04	SYNC1	Sync word, high byte	42
0x05	SYNC0	Sync word, low byte	42
0x06	PKTLEN	Packet length	42
0x08	PKTCTRL0	Packet automation control	42
0x0A	CHANNR	Channel number	43
0x0D	FREQ2	Frequency control word, high byte	43
0x0E	FREQ1	Frequency control word, middle byte	43
0x0F	FREQ0	Frequency control word, low byte	43
0x10	MDMCFG4	Modulator configuration	43
0x11	MDMCFG3	Modulator configuration	43
0x12	MDMCFG2	Modulator configuration	44
0x13	MDMCFG1	Modulator configuration	45
0x14	MDMCFG0	Modulator configuration	45
0x15	DEVIATN	Modulator deviation setting	46
0x17	MCSM1	Main Radio Control State Machine configuration	46
0x18	MCSM0	Main Radio Control State Machine configuration	47
0x22	FREND0	Front end TX configuration	47
0x23	FSCAL3	Frequency synthesizer calibration	48
0x24	FSCAL2	Frequency synthesizer calibration	48
0x25	FSCAL1	Frequency synthesizer calibration	48
0x26	FSCAL0	Frequency synthesizer calibration	48
0x29	FSTEST	Frequency synthesizer calibration control	49
0x2A	PTEST	Production test	49
0x2C	TEST2	Various test settings	49
0x2D	TEST1	Various test settings	49
0x2E	TEST0	Various test settings	49

Table 24: Configuration Registers Overview

Address	Register	Description	Details on Page Number
0x30 (0xF0)	PARTNUM	*CC2550* part number	49
0x31 (0xF1)	VERSION	Current version number	49
0x35 (0xF5)	MARCSTATE	Control state machine state	50
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	50
0x39 (0xF9)	VCO_VC_DAC	Current setting from PLL calibration module	51
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	51

Table 25: Status Registers Overview

	Write		Read		
	Single byte	Burst	Single byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	Reserved				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	Reserved				
0x08	PKTCTRL0				
0x09	Reserved				
0x0A	CHANNR				
0x0B	Reserved				
0x0C	Reserved				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	Reserved				
0x17	MCSM1				
0x18	MCSM0				
0x19	Reserved				
0x1A	Reserved				
0x1B	Reserved				
0x1C	Reserved				
0x1D	Reserved				
0x1E	Reserved				
0x1F	Reserved				
0x20	Reserved				
0x21	Reserved				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	Reserved				
0x28	Reserved				
0x29	FSTEST				
0x2A	PTEST				
0x2B	Reserved				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F					
0x30	SRES		SRES	PARTNUM	Command strobes, status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	Reserved	
0x34	Reserved		Reserved	Reserved	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	Reserved	
0x37				Reserved	
0x38	Reserved		Reserved	PKTSTATUS	
0x39	SPWD		SPWD	VCO_VC_DAC	
0x3A	Reserved		Reserved	TXBYTES	
0x3B	SFTX		SFTX	Reserved	
0x3C	Reserved		Reserved		
0x3D	SNOP		SNOP		
0x3E	PATABLE	PATABLE	Reserved	Reserved	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 26: SPI Address Space

28.1 Configuration Register Details

0x01: IOCFG1 – GD01 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (0x2E)	R/W	Default is 3-state (see Table 22 on page 34)

0x02: IOCFG0 – GD00 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	TEMP_SENSOR_ENABLE	0	R/W	Enable analog temperature sensor. Write 0 in all other register bits when using temperature sensor. Note: PTEST must be written to 0xBF to make the on-chip temperature sensor available in the IDLE state.
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (see Table 22on page 34)

0x03: FIFOTHR – TX FIFO Threshold

Bit	Field Name	Reset	R/W	Description
7:4	Reserved	0 (0000)	R/W	Write 0 (0000) for compatibility with possible future extensions
3:0	FIFO_THR[3:0]	7 (0111)	R/W	Set the threshold for the TX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.

Setting	Bytes in TX FIFO
0 (0000)	61
1 (0001)	57
2 (0010)	53
3 (0011)	49
4 (0100)	45
5 (0101)	41
6 (0110)	37
7 (0111)	33
8 (1000)	29
9 (1001)	25
10 (1010)	21
11 (1011)	17
12 (1100)	13
13 (1101)	9
14 (1110)	5
15 (1111)	1

0x04: SYNC1– Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 – Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN – Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length is enabled.

0x08: PKTCTRL0 – Packet Automation Control

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6	WHITE_DATA	1	R/W	Turn data whitening on / off 0: Whitening off 1: Whitening on Data whitening can only be used when PKTCTRL0.CC2400_EN=0 (default).
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of TX data Setting: Packet format 0 (00): Normal mode, use TX FIFO 1 (01): Synchronous serial mode, used for backwards compatibility 2 (10): Random TX mode; sends random data using PN9 generator. Used for test. 3 (11): Asynchronous serial mode. Data in on GDO0.
3	CC2400_EN	0	R/W	Enable CC2400 support. Use same CRC implementation as CC2400. PKTCTRL0.WHITE_DATA must be 0 if PKTCTRL0.CC2400_EN=1.
2	CRC_EN	1	R/W	1: CRC calculation enabled 0: CRC disabled
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length Setting: Packet length configuration 0 (00): Fixed packet length mode. Length configured in PKTLEN register 1 (01): Variable packet length mode. Length configured by the first byte after sync word 2 (10): Infinite packet length mode 3 (11): Reserved

0x0A: CHANNR – Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0D: FREQ2 – Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	1 (01)	R	FREQ[23:22] is always binary 01 (the FREQ2 register is in the range 85 to 95 with 26-27 MHz crystal)
5:0	FREQ[21:16]	30 (0x1E)	R/W	FREQ[23:0] is the base frequency for the frequency synthesiser in increments of $F_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 – Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. FREQ2 register

0x0F: FREQ0 – Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. FREQ2 register

0x10: MDMCFG4 – Modulator Configuration

Bit	Field Name	Reset	R/W	Description
7:4	Reserved		R0	Defined in the transceiver version
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 – Modulator Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE_M) \cdot 2^{DRATE_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 – Modulator Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th>Description</th></tr>
<tr><td>7</td><td>Reserved</td><td></td><td>R0</td><td></td></tr>
<tr><td>6:4</td><td>MOD_FORMAT[2:0]</td><td>1 (001)</td><td>R/W</td><td>The modulation format of the radio signal
<table>
<tr><th>Setting</th><th>Modulation format</th></tr>
<tr><td>0 (000)</td><td>2-FSK</td></tr>
<tr><td>1 (001)</td><td>GFSK</td></tr>
<tr><td>2 (010)</td><td>-</td></tr>
<tr><td>3 (011)</td><td>OOK</td></tr>
<tr><td>4 (100)</td><td>-</td></tr>
<tr><td>5 (101)</td><td>-</td></tr>
<tr><td>6 (110)</td><td>-</td></tr>
<tr><td>7 (111)</td><td>MSK</td></tr>
</table></td></tr>
<tr><td>3</td><td>MANCHESTER_EN</td><td>0</td><td>R/W</td><td>Enables Manchester encoding
0 = Disable
1 = Enable (Only supported for fixed packet length mode, i.e. PKTCTRL0.LENGTH_CONFIG=0)</td></tr>
<tr><td>2:0</td><td>SYNC_MODE[2:0]</td><td>2 (010)</td><td>R/W</td><td>Sync-word mode.
<table>
<tr><th>Setting</th><th>Sync-word mode</th></tr>
<tr><td>0 (000)</td><td>Disable preamble and sync word transmission</td></tr>
<tr><td>1 (001)</td><td>Enable 16-bit sync word transmission</td></tr>
<tr><td>2 (010)</td><td>Enable 16-bit sync word transmission</td></tr>
<tr><td>3 (011)</td><td>Repeated sync word transmission</td></tr>
<tr><td>4 (100)</td><td>Disable preamble and sync word transmission</td></tr>
<tr><td>5 (101)</td><td>Enable 16-bit sync word transmission</td></tr>
<tr><td>6 (110)</td><td>Enable 16-bit sync word transmission</td></tr>
<tr><td>7 (111)</td><td>Repeated sync word transmission</td></tr>
</table></td></tr>
</table>

0x13: MDMCFG1 – Modulator Configuration

Bit	Field Name	Reset	R/W	Description
7	FEC_EN	0	R/W	Enable Forward Error Correction (FEC) with interleaving for packet payload 0 = Disable 1 = Enable
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted Setting / Number of preamble bytes 0 (000) / 2 1 (001) / 3 2 (010) / 4 3 (011) / 6 4 (100) / 8 5 (101) / 12 6 (110) / 16 7 (111) / 24
3:2	Reserved		R0	
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing

0x14: MDMCFG0 – Modulator Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing (initial 1 assumed). The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC_M) \cdot 2^{CHANSPC_E} \cdot CHAN$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN – Modulator Deviation Setting

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:4	DEVIATION_E[2:0]	4 (100)	R/W	Deviation exponent
3	Reserved		R0	
2:0	DEVIATION_M[2:0]	7 (111)	R/W	When MSK modulation is enabled: Sets fraction of symbol period used for phase change. Refer to the SmartRF® Studio software [4] for correct DEVIATN setting when using MSK. When 2-FSK/GFSK modulation is enabled: Deviation mantissa, interpreted as a 4-bit value with MSB implicit 1. The resulting deviation is given by: $f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION_M) \cdot 2^{DEVIATION_E}$ The default values give ±47.607 kHz deviation, assuming 26.0 MHz crystal frequency.

0x17: MCSM1 – Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:2	Reserved		R0	Defined in the transceiver version
1:0	TXOFF_MODE[1:0]	0 (00)	R/W	Select what should happen when a packet has been sent (TX) Setting: Next state after finishing packet transmission 0 (00): IDLE 1 (01): FSTXON 2 (10): Stay in TX (start sending preamble) 3 (11): Do not use, not implemented in *CC2550* (Go to RX)

0x18: MCSM0 – Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	FS_AUTOCAL[1:0]	0 (00)	R/W	Automatically calibrate when going to TX or back to IDLE Setting: When to perform automatic calibration 0 (00): Never (manually calibrate using SCAL strobe) 1 (01): When going from IDLE to TX (or FSTXON) 2 (10): When going from TX back to IDLE 3 (11): Every 4th time when going from TX to IDLE
3:2	PO_TIMEOUT	2 (10)	R/W	Programs the number of times the six-bit ripple counter must expire after XOSC has stabilized before CHP_RDYn goes low. If XOSC is on (stable) during power-down, PO_TIMEOUT should be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 us. If XOSC is off during power-down and the regulated digital supply voltage has sufficient time to stabilize while waiting for the crystal to be stable, PO_TIMEOUT can be set to 0. For robust operation it is recommended to use PO_TIMEOUT=2. Setting / Expire count / Timeout after XOSC start 0 (00) / 1 / Approx. 2.3 – 2.4 µs 1 (01) / 16 / Approx. 37 – 39 µs 2 (10) / 64 / Approx. 149 – 155 µs 3 (11) / 256 / Approx. 597 – 620 µs Exact timeout depends on crystal frequency. In order to reduce start up time from the SLEEP state, this field is preserved in powerdown (SLEEP state).
1:0	Reserved		R0	Defined in the transceiver version

0x22: FREND0 – Front End TX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF® Studio software [4].
3	Reserved		R0	
2:0	PA_POWER[2:0]	0 (000)	R/W	Selects PA power setting. This value is an index to the PATABLE. In OOK mode, this selects the PATABLE index to use when transmitting a '1'. PATABLE index zero is used in OOK when transmitting a '0'.

0x23: FSCAL3 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (10)	R/W	Frequency synthesizer calibration configuration. The value to write in this register before calibration is given by the SmartRF® Studio software [4].
5:4	CHP_CURR_CAL_EN[1:0]	2 (10)	R/W	Disable charge pump calibration stage when 0
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $IOUT=I_0 \cdot 2^{FSCAL3[3:0]/4}$ Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x24: FSCAL2 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[5:0]	10 (0x0A)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x25: FSCAL1 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	Reserved		R0	
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Fast frequency hopping without calibration for each hop can be done by calibrating upfront for each frequency and saving the resulting FSCAL3, FSCAL2 and FSCAL1 register values. Between each frequency hop, calibration can be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values corresponding to the next RF frequency.

0x26: FSCAL0 – Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7	Reserved		R0	
6:5	Reserved	0 (00)	R0	Defined in the transceiver version
4:0	FSCAL0[4:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in register field is given by the SmartRF® Studio software [4].

0x29: FSTEST – Frequency Synthesizer Calibration Control

Bit	Field Name	Reset	R/W	Description
7:0	FSTEST[7:0]	87 (0x57)	R/W	For test only. Do not write to this register.

0x2A: PTEST – Production Test

Bit	Field Name	Reset	R/W	Description
7	PTEST[7:0]	127 (0x7F)	R/W	Writing 0xBF to this register makes the on-chip temperature sensor available in the IDLE state. The default 0x7F value should then be written back before leaving the IDLE state. Other use of this register is for test only.

0x2C: TEST2 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	152 (0x98)	R/W	The value to use in this register is given by the SmartRF® Studio software [4].

0x2D: TEST1 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	The value to use in this register is given by the SmartRF® Studio software [4].

0x2E: TEST0 – Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (0x02)	R/W	The value to use in this register is given by the SmartRF® Studio software [4].
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	The value to use in this register is given by the SmartRF® Studio software [4].

28.2 Status Register Details

0x30 (0xF0): PARTNUM – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	130 (0x82)	R	Chip part number

0x31 (0xF1): VERSION – Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	2 (0x02)	R	Chip version number

0x35 (0xF5): MARCSTATE – Main Radio Control State Machine State

Bit	Field Name	Reset	R/W	Description
7:5	Reserved		R0	
4:0	MARC_STATE[4:0]		R	Main Radio Control FSM State

Value	State name	State (Figure 13, page 25)
0 (0x00)	SLEEP	SLEEP
1 (0x01)	IDLE	IDLE
2 (0x02)	XOFF	XOFF
3 (0x03)	VCOON_MC	MANCAL
4 (0x04)	REGON_MC	MANCAL
5 (0x05)	MANCAL	MANCAL
6 (0x06)	VCOON	FS_WAKEUP
7 (0x07)	REGON	FS_WAKEUP
8 (0x08)	STARTCAL	CALIBRATE
9 (0x09)	BWBOOST	SETTLING
10 (0x0A)	FS_LOCK	SETTLING
11 (0x0B)	IFADCON	SETTLING
12 (0x0C)	ENDCAL	CALIBRATE
13 (0x0D)	NA	NA
14 (0x0E)	NA	NA
15 (0x0F)	NA	NA
16 (0x10)	NA	NA
17 (0x11)	NA	NA
18 (0x12)	FSTXON	FSTXON
19 (0x13)	TX	TX
20 (0x14)	TX_END	TX
21 (0x15)	NA	NA
22 (0x16)	TX_UNDERFLOW	TX_UNDERFLOW

Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.

0x38 (0xF8): PKTSTATUS – Current GD0x Status and Packet Status

Bit	Field Name	Reset	R/W	Description
7:2	Reserved		R0	Defined in the transceiver version
1	Reserved		R0	
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective what IOCFG0.GDO0_INV is programmed to. It is not recommended to check for PLL lock by reading PKTSTATUS[0] with GDO0_CFG = 0x0A.

0x39 (0xF9): VCO_VC_DAC – Current Setting from PLL Calibration Module

Bit	Field Name	Reset	R/W	Description
7:0	VCO_VC_DAC[7:0]		R	Status register for test only

0x3A (0xFA): TXBYTES – Underflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

29 Package Description (QLP 16)

All dimensions are in millimetres, angles in degrees. NOTE: The ***CC2550*** is available in RoHS lead-free package only.

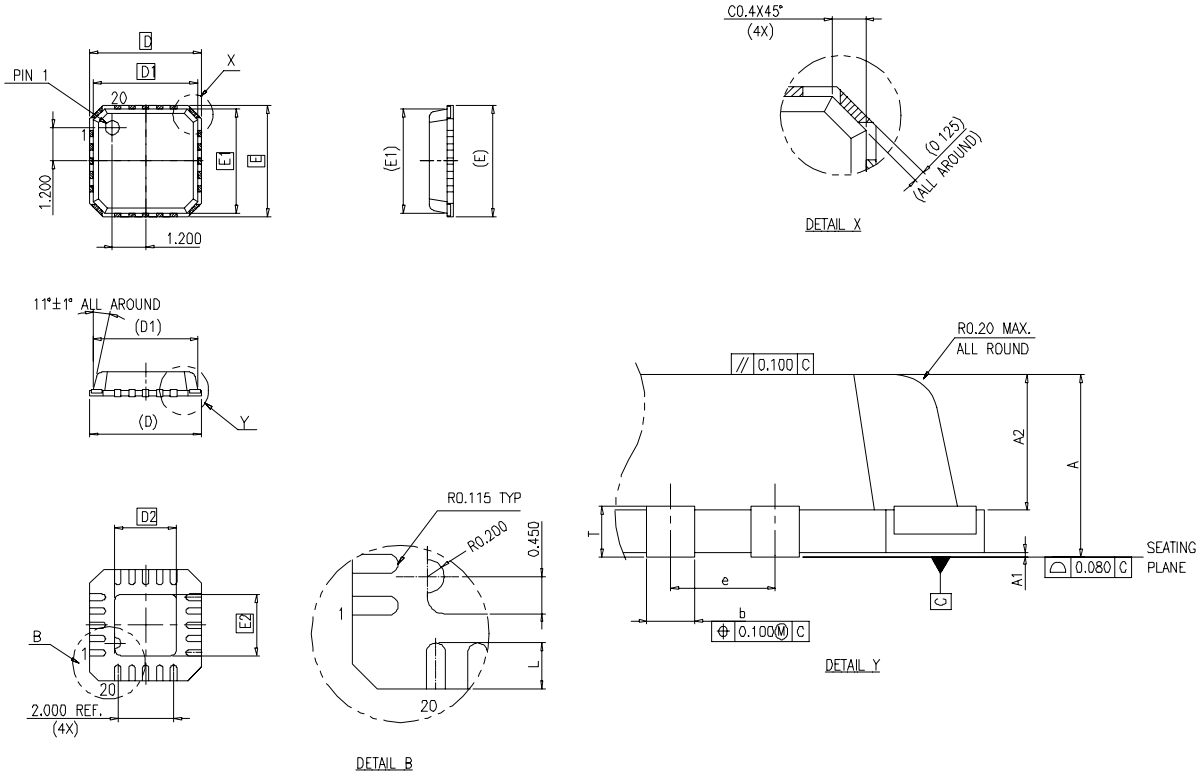

Figure 23: Package Dimensions Drawing (the actual package has 16 pins)

Package type		A	A1	A2	D	D1	D2	E	E1	E2	L	T	b	e
QLP 16 (4x4)	Min	0.75	0.005	0.55	3.90	3.65		3.90	3.65		0.45	0.190	0.23	
	Typ.	0.85	0.025	0.65	4.00	3.75	2.30	4.00	3.75	2.30	0.55		0.28	0.65
	Max	0.95	0.045	0.75	4.10	3.85		4.10	3.85		0.65	0.245	0.35	

Table 27: Package Dimensions

29.1 Recommended PCB Layout for Package (QLP 16)

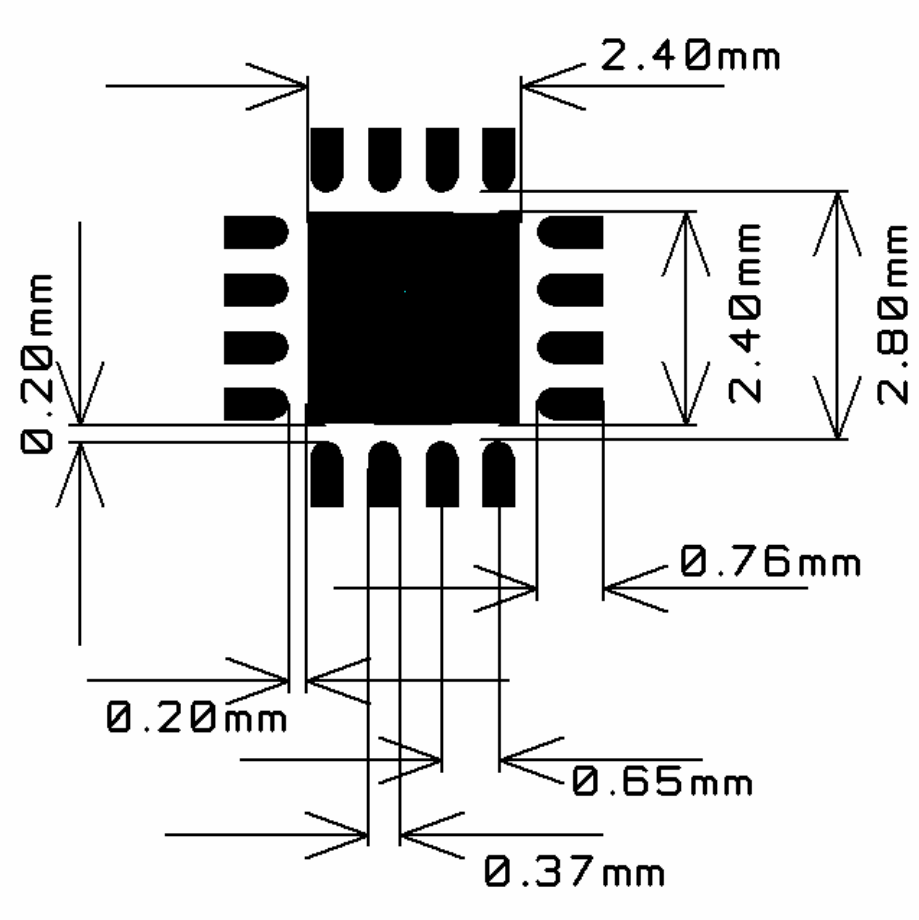

Figure 24: Recommended PCB layout for QLP 16 package

Note: The figure is an illustration only and not to scale. There are five 10 mil diameter via holes distributed symmetrically in the ground pad under the package. See also the CC2550EM reference design [3].

29.2 Package Thermal Properties

Thermal Resistance	
Air velocity [m/s]	0
Rth,j-a [K/W]	40.1

Table 28: Thermal Properties of QLP 16 Package

29.3 Soldering Information

The recommendations for lead-free reflow in IPC/JEDEC J-STD-020D should be followed.

29.4 Tray Specification

CC2550 can be delivered in standard QLP 4x4 mm shipping trays.

Tray Specification				
Package	Tray Width	Tray Height	Tray Length	Units per Tray
QLP 16	135.9 mm	7.62 mm	322.6 mm	490

Table 29: Tray Specification

29.5 Carrier Tape and Reel Specification

Carrier tape and reel is in accordance with EIA Specification 481.

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QLP 16	12 mm	8 mm	4 mm	13 inches	2500

Table 30: Carrier Tape and Reel Specification

30 Ordering Information

Part Number	Description	Minimum Order Quantity (MOQ)
CC2550RTK	*CC2550* QLP16 RoHS Pb-free 490/tray	490 (tray)
CC2550RTKR	*CC2550* QLP16 RoHS Pb-free 2500/T&R	2500 (tape and reel)
CC2500-CC2550DK	*CC2500_CC2550* Development Kit	1
CC2550EMK	*CC2500* Evaluation Module Kit	1

Table 31: Ordering Information

31 References

[1] CC2550 Errata Notes (swrz011.pdf)

[2] AN032 2.4 GHz Regulations (swra060.pdf)

[3] CC2550EM Reference Design 1.0 (swrr015.zip)

[4] SmartRF® Studio (swrc046.zip)

[5] CC1100 CC2500 Examples Libraries (swrc021.zip)

[6] CC1100/CC1150DK & CC2500/CC2550DK Development Kit Examples & Libraries User Manual (swru109.pdf)

[7] CC25XX Folded Dipole Reference Design (swrc065.zip)

[8] DN004 Folded Dipole Antenna for CCC25xx (swra118.pdf)

[9] CC2500 Data Sheet (cc2500.pdf)

32 General Information

32.1 Document History

Revision	Date	Description/Changes
SWRS039B	2007-09-30	kbps replaced by kBaud throughout the document. Some of the sections hav been re-written to be easier to read without having any new info added. Absolute maximum supply voltage rating increased from 3.6 V to 3.9 V. FSK changed to 2-FSK throughout the document. Updates to the Abbreviation table. Updates to the Electrical Specifications section. Added ACP and OBW performance. Added info about TX latency in serial mode. Added info about default values after reset versus optimum register settings in the Configuration Software section. Changes to the SPI Interface Timing Requirements. Info added about $t_{sp,pd}$ The following figures have been changed: Configuration Registers Write and Read Operations, SRES Command Strobe, and Register Access Types. In the Register Access section, the address range is changed. Changes to PATABLE Access section. In the Packet Format section, preamble pattern is changed to 10101010 and info about bug related to turning off the transmitter in infinite packet length mode is added. Added info about the initial value of the PN9 sequence in the Data Whitening section. Added info about TX FIFO underflow state in the Packet Handling in Transmit Mode section. Added section Packet Handling in Firmware. Removed all references to the voltage regulator in relation with the CHP_RDYn signal, as this signal is only related to the crystal. Removed references to the voltage regulator in the figures: Power-On Reset and Power-On Reset with SRES. Changes to the SI line in the Power-On Reset with SRES figure. Added info on the three automatic calibration options. The Output Power Programming section has been changed. Only 1 PATABLE entry used for 2-FSK/GFSK/MSK and 2 PATABLE entries used for OOK. Added info about PATABLE when entering SLEEP mode. New PA_POWER and PATABLE figure. Added section on PCB Layout Recommendations. In section General Purpose / Test Output Control Pins: Added info on GDO pins in SLEEP state. Asynchronous transparent mode is called asynchronous serial mode throughout the document. Removed comments about having to use NRZ coding in synchronous serial mode. Added info that Manchester encoding cannot be used in asynchronous serial mode. Changed field name and/or description of the following registers: MCSM0, FSCAL3, FSCAL2, FSCAL1 and TEST0. Added references.
1.2 SWRS039A	2006-06-28	Added figures to table on SPI interface timing requirements. Added information about SPI read. Updates to text and included new figure in section on arbitrary length configuration. Added information that RF frequencies at n/2·crystal frequency (n is an integer number) should not be used due to spurious signals at these frequencies . Updates to text and included new figures in section on power-on start-up sequence. Added information about how to check for PLL lock in section on VCO. Better explanation of some of the signals in table of GDO signal selection. Added section on wideband modulation not using spread spectrum under section on system considerations and guidelines. Added more detailed information on PO_TIMEOUT in register MCSM0. Changes to ordering information.
1.1	2005-06-27	Updated TEST1 register default value. 26-27 MHz crystal range. Added matching information. Added information about using a reference signal instead of a crystal.
1.0	2005-01-24	First preliminary data sheet release.

Table 32: Document History

32.2 Product Status Definitions

Data Sheet Identification	Product Status	Definition
Advance Information	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and Pre-Production Prototypes	This data sheet contains preliminary data, and supplementary data will be published at a later date. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. The product is not yet fully qualified at this point.
No Identification Noted	Full Production	This data sheet contains the final specifications. Chipcon reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by Chipcon. The data sheet is printed for reference information only.

Table 33: Product Status Definitions

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	Indonesia	001-803-8861-1006
	Korea	080-551-2804
	Malaysia	1-800-80-3973
	New Zealand	0800-446-934
	Philippines	1-800-765-7404
	Singapore	800-886-1028
	Taiwan	0800-006800
	Thailand	001-800-886-0010
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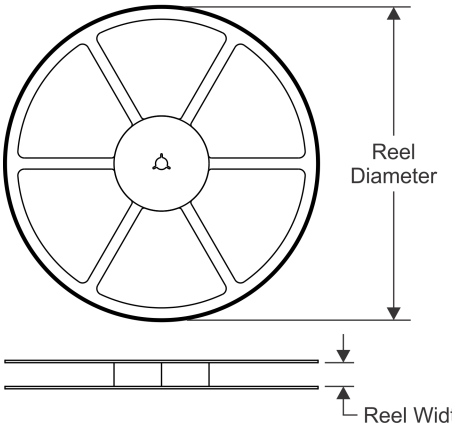
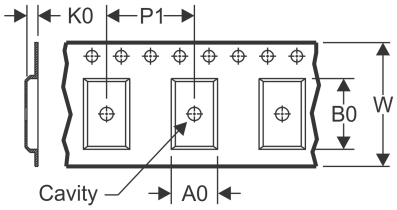
Email		tiasia@ti.com or ti-china@ti.com
Internet		support.ti.com/sc/pic/asia.htm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

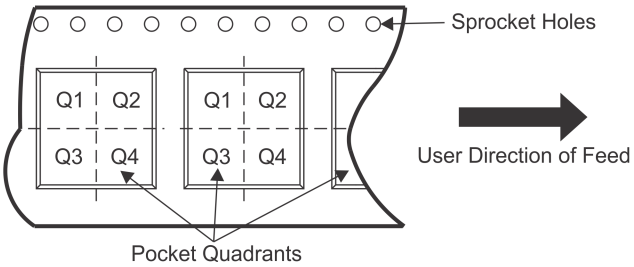


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

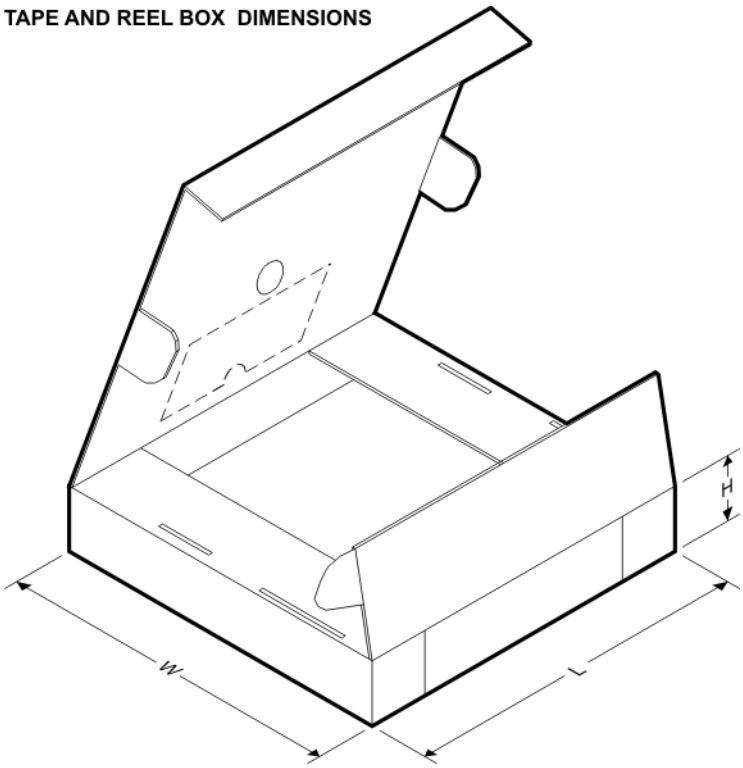
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC2550RSTR	VQFN	RST	16	2500	330.0	12.4	4.25	4.25	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC2550RSTR	VQFN	RST	16	2500	378.0	70.0	346.0

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