DR80390

High Performance 8-bit Microcontroller ver 3.10

OVERVIEW

DR80390 is a **high performance, area optimized** soft core of a single-chip 8-bit embedded controller dedicated for operation with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern about **low power consumption**. Additionally an advanced power management unit makes DR80390 core **perfect for portable equipment** where low power consumption is mandatory.

DR80390 soft core is 100% binary-compatible with the industry standard 80C390 8-bit microcontroller. There are two configurations of DR80390: **Harward** where external data and program buses are separated, and **von Neumann** with common program and external data bus. DR80390 has RISC architecture **6.7 times faster** compared to standard architecture and executes **65-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications where the core can be clocked up to seven times more slowly than the original implementation for no performance penalty.

DR80390 is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- 100% software compatible with industry standard 80390
  - *LARGE mode – 8051 instruction set*
  - *FLAT mode – 80390 instruction set*
- RISC architecture enables to execute instructions 6.7 times faster compared to standard 8051
- 12 times faster multiplication
- 9.6 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- **Up to 16M bytes of contiguous Program Memory**
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- De-multiplexed Address/Data bus to allow easy connection to memory
- Interface for additional Special Function Registers

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- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready
- **1.3 GHz virtual** clock frequency in a 0.35u technological process

PERIPHERALS

- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Internal (direct) Data Memory*
    - *Special Function Registers (SFRs)*
    - *External Data Memory*
  - *Hardware breakpoints activated at a certain*
    - *Program address (PC)*
    - *Address by any write into memory*
    - *Address by any read from memory*
    - *Address by write into memory a required data*
    - *Address by read from memory a required data*
  - *Three wire communication interface*
- Power Management Unit
  - *Power management mode*
  - *Switchback feature*
  - *Stop mode*
- Interrupt Controller
  - *2 priority levels*
  - *2 external interrupt sources*
  - *3 interrupt sources from peripherals*
- Four 8-bit I/O Ports
  - *Bit addressable data direction for each line*
  - *Read/write of single line and 8-bit group*
- Two 16-bit timer/counters
  - *Timers clocked by internal source*
  - *Auto reload 8-bit timers*
  - *Externally gated event counters*
- Full-duplex serial port
  - *Synchronous mode, fixed baud rate*
  - *8-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, fixed baud rate*
  - *9-bit asynchronous mode, variable baud rate*

CONFIGURATION

The following parameters of the DR80390 core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• Memory style	- Harward - von Neumann
• Program Memory type	- synchronous - asynchronous
• Program Memory wait-states	- used (0-7) - unused
• Program Memory writes	- used - unused
• Internal Data Memory type	- synchronous - asynchronous
• External Data Memory wait-states	- used (0-7) - unused
• Interrupts	- subroutines location
• Power Management Mode	- used - unused
• Stop mode	- used - unused
• DoCD™ debug unit	- used - unused

Besides mentioned above parameters all available peripherals and external interrupts can be excluded from the core by changing appropriate constants in package file.

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DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

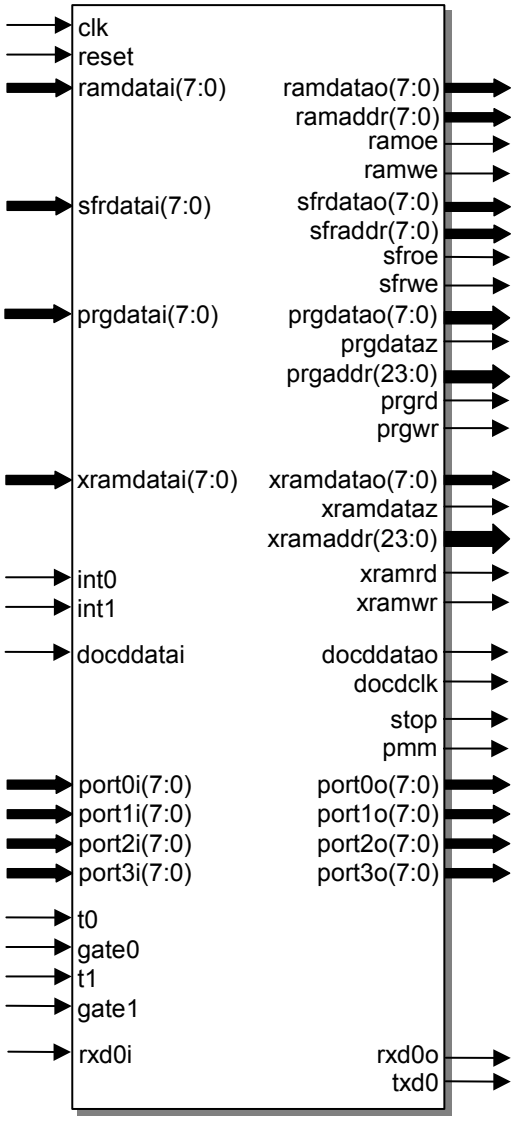
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL

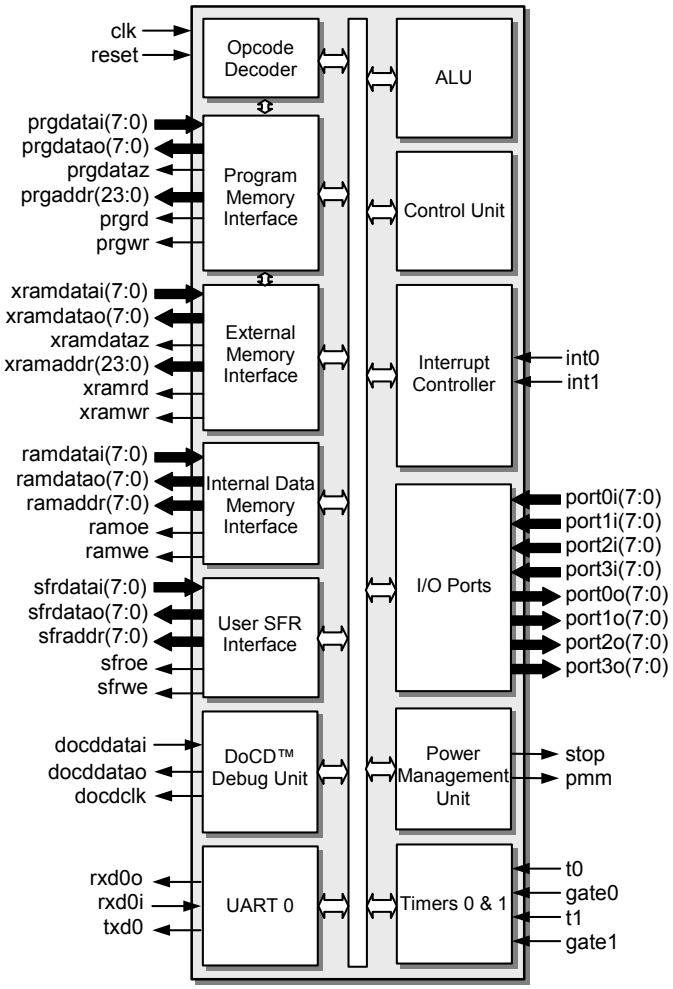


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BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global synchronous reset
ramdatai[7:0]	input	Data bus from Internal Data Memory
sfrdatai[7:0]	input	Data bus from user SFRs
prgdatai[7:0]	input	Input data bus from Program Memory
xramdatai[7:0]	input	Data bus from External Data Memory
int0	input	External interrupt 0 line
int1	input	External interrupt 1 line
docddatai	input	DoCD™ data input
port0i[7:0]	input	Port 0 input
port1i[7:0]	input	Port 1 input
port2i[7:0]	input	Port 2 input
port3i[7:0]	input	Port 3 input
t0	input	Timer 0 clock line
gate0	input	Timer 0 clock line gate control
t1	input	Timer 1 clock line
gate1	input	Timer 1 clock line gate control
rxd0i	input	Serial receiver input 0
ramdatao[7:0]	output	Data bus for Internal Data Memory
ramaddr[7:0]	output	Internal Data Memory address bus
ramoe	output	Internal Data Memory output enable
ramwe	output	Internal Data Memory write enable
sfrdatao[7:0]	output	Data bus for user SFRs
sfraddr[7:0]	output	User SFRs address bus
sfroe	output	User SFRs output enable
sfrwe	output	User SFRs write enable
prgaddr[23:0]	output	Program Memory address bus
prgdatao[7:0]	output	Output data bus for Program Memory
prgdataz	output	PRGDATA tri-state buffers control line
prgrd	output	Program Memory read
prgwr	output	Program Memory write
xramdatao[7:0]	output	Data bus for External Data Memory
xramdataz	output	XDATA tri-state buffers control line
xramaddr[23:0]	output	External Data Memory address bus
xramrd	output	External Data Memory read
xramwr	output	External Data Memory write
docddatao	output	DoCD™ data output
docdclk	output	DoCD™ clock line
pmm	output	Power management mode indicator
stop	output	Stop mode indicator
port0o[7:0]	output	Port 0 output
port1o[7:0]	output	Port 1 output
port2o[7:0]	output	Port 2 output
port3o[7:0]	output	Port 3 output
rxd0o	output	Serial receiver output 0
txd0	output	Serial transmitter line 0
rxd1o	output	Serial receiver output 1
txd1	output	Serial transmitter line 1

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic such as arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.

Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader loading new

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program into RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module. Program fetch cycle length can be programmed by user. This feature is called Program Memory Wait States, and allows core to work with different speed program memories.

External Memory Interface – Contains memory access related registers such as Data Pointer High (DPH0), Data Pointer Low (DPL0), Data Page Pointer (DPP0), MOVX @Ri address register (MXAX) and STRETCH registers. It performs the memory addressing and data transfers. Allows applications software to access up to 16 MB of external data memory. The DPP0 register is used for segments swapping. STRETCH register allows flexible timing management while accessing different speed system devices by programming XRAMWR and XRAMRD pulse width between 1 – 8 clock periods.

Internal Data Memory Interface – Internal Data Memory interface controls access into the internal 256 bytes memory. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system for the external and internal interrupt sources. It contains interrupt related registers such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.

I/O Ports – Block contains 8051's general purpose I/O ports. Each of port's pin can be read/write as a single bit or as an 8-bit bus called P0, P1, P2, P3.

Power Management Unit – Block contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode) to significantly reduce power consumption. Switchback feature allows UARTs, and interrupts to be processed in full speed mode if enabled. It is very desired when microcontroller is planned to use in portable and power critical applications.

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods when appropriate timer is enabled. In the counter mode the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.

UART0 – Universal Asynchronous Receiver & Transmitter module is full duplex, meaning it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register, and reading SBUF0 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1.

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PERFORMANCE

The following tables give a survey about the Core area and performance in ASICs Devices (CPU features and peripherals have been included):

Device	Optimization	F_{max}
0.25u typical	area	100 MHz
0.25u typical	speed	250 MHz

Core performance in ASIC devices

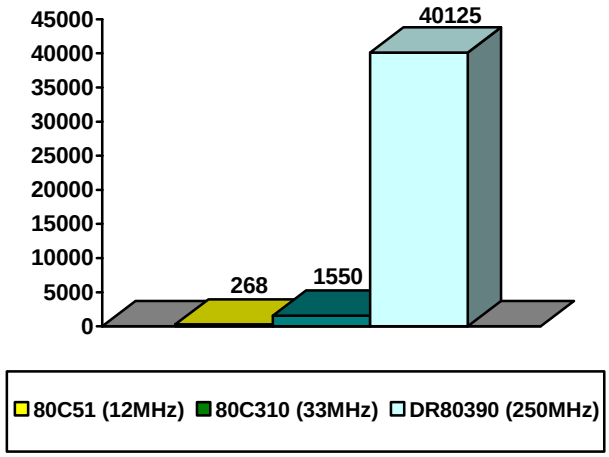
For a user the most important is application speed improvement. The most commonly used arithmetic functions and their improvements are shown in table below. An improvement was computed as {80C51 clock periods} divided by {DR80390 clock periods} required to execute an identical function. More details are available in core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**7,20**
8-bit addition (*direct addressing*)	**6,00**
8-bit addition (*indirect addressing*)	**6,00**
8-bit addition (*register addressing*)	**7,20**
8-bit subtraction (*immediate data*)	**7,20**
8-bit subtraction (*direct addressing*)	**6,00**
8-bit subtraction (*indirect addressing*)	**6,00**
8-bit subtraction (*register addressing*)	**7,20**
8-bit multiplication	**10,67**
8-bit division	**9,60**
16-bit addition	**7,20**
16-bit subtraction	**7,64**
16-bit multiplication	**9,75**
32-bit addition	**7,20**
32-bit subtraction	**7,43**
32-bit multiplication	**9,04**
Average speed improvement:	**7,58**

Dhrystone Benchmark Version 2.1 was used to measure Core performance. The following table gives a survey about the DR80390 performance in terms of Dhrystone/sec and VAX MIPS rating.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	-	12 MHz	268 (0.153)
80C310	-	33 MHz	1550 (0.882)
DR80390	0.25u	250 MHz	40125 (22.837)

Core performance in terms of Dhrystones



Area utilized by the each unit of DR80390 core in vendor specific technologies is summarized in table below.

Component	Area [Gates]	Area [FFs]
CPU*	5500	250
Interrupt Controller	450	40
Power Management Unit	50	5
I/O ports	400	35
Timers	550	50
UART0	650	60
Total area	7600	430

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization

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The main features of each DR80390 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space	Stack space size	Internal Data Memory space	External Data Memory space	External Data Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	IO Ports	Program Memory Wait States	Compare/Capture	Watchdog	Master I^2C Bus Controller	Slave I^2C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
DR80390CPU	6.7	16M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-
DR80390	6.7	16M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-
DR80390XP	6.7	16M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓

DR80390 family of High Performance Microcontroller Cores

The main features of each DR8051 family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space	Stack space size	Internal Data Memory space	External Data Memory space	External Data Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	IO Ports	Program Memory Wait States	Compare/Capture	Watchdog	Master I^2C Bus Controller	Slave I^2C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
DR8051CPU	6.7	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-	-
DR8051	6.7	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-	-
DR8051XP	6.7	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓	✓

DR8051 family of High Performance Microcontroller Cores

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