

MECL PLL COMPONENTS $\div 64/65$, $\div 128/129$
SEMICONDUCTOR TECHNICAL DATA

Legacy Device: Motorola MC12054A

The ML12054A is a super low power dual modulus prescaler used in phase-locked loop applications with low power dissipation of 5.4 mW at a minimum supply voltage of 2.7 V.

The ML12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx or Lansdale's ML145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- The ML12054A is Pin and Functionally Compatible with the Motorola MC12031
- Low Supply Current 2.0 mA Typical
- 2.6mA Maximum, $V_{CC} = 2.7$ to 5.5 Vdc
- Short Setup Time (T_{set}) 10ns Maximum @ 2.0 GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5 Vdc
- Operating Temperature Range $T_A = -40$ to 85°C


FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

NOTES: 1. SW: H = V_{CC} , L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to V_{CC} , L = GND to 0.8 V.

MAXIMUM RATINGS

Characteristic	Symbol	Range	Unit
Power Supply Voltage, Pin 2	V_{CC}	-0.5 to 7.0	Vdc
Operating Temperature Range	T_A	-40 to 85	°C
Storage Temperature Range	T_{stg}	-65 to 150	°C
Modulus Control Input, Pin 6	MC	-0.5 to 6.5	Vdc

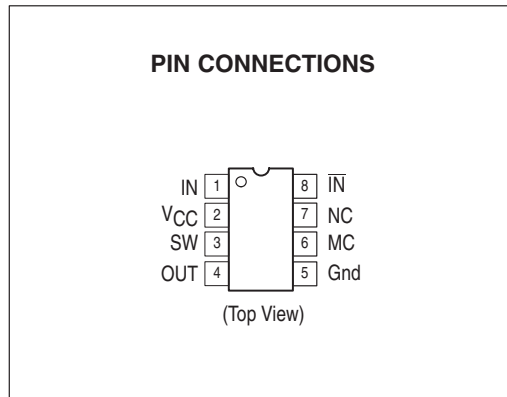


SO 8 -5P
PLASTIC PACKAGE
CASE 751
(SO-8)

PACKAGE	MOTOROLA	LANSDALE
SO 8	MC12054AD	ML12054A-5P

CROSS REFERENCE/ORDERING INFORMATION

Note: Lansdale lead free (Pb) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.



ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7$ to 5.5 Vdc, $T_A = -40$ to 85°C , unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Toggle Frequency (Sine Wave Input)	f_t	0.1	2.5	2.0	GHz
Supply Current (Pin 2)	I_{CC}	–	2.0	2.6	mA
Modulus Control Input High (MC)	V_{IH1}	2.0	–	$V_{CC} + 0.5$ V	V
Modulus Control Input Low (MC)	V_{IL1}	Gnd	–	0.8	V
Divide Ratio Control Input High (SW)	V_{IH2}	$V_{CC} - 0.5$ V	V_{CC}	$V_{CC} + 0.5$ V	VDC
Divide Ratio Control Input Low (SW)	V_{IL2}	Open	Open	Open	–
Output Voltage Swing (Note 2) ($C_L = 8.0$ pF, $R_L = 1.65$ k Ω)	V_{out}	0.8	1.1	–	V_{pp}
Modulus Setup Time MC to Out @ 2000 MHz	t_{set}	–	8.0	10	ns
Input Voltage Sensitivity 250–2000 MHz 100–250 MHz	V_{in}	100 400	– –	1000 1000	mVpp
Output Current (Note 1) $V_{CC} = 2.7$ V, $C_L = 8.0$ pF, $R_L = 1.65$ k Ω $V_{CC} = 5.0$ V, $C_L = 8.0$ pF, $R_L = 3.6$ k Ω	I_O	– –	1.0 1.0	4.0 4.0	mA

NOTES: 1. Divide ratio of +64/65 @ 2.0 GHz
2. Valid over voltage range 2.7 to 5.5 V; $R_L = 1.65$ k Ω @ $V_{CC} = 2.7$ V; $R_L = 3.6$ k Ω @ $V_{CC} = 5.0$ V

Figure 1. Logic Diagram (ML12054A)

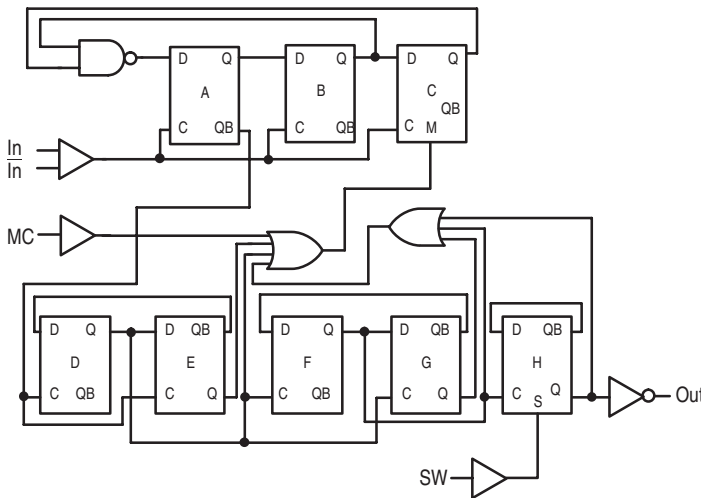


Figure 2. Modulus Setup Time

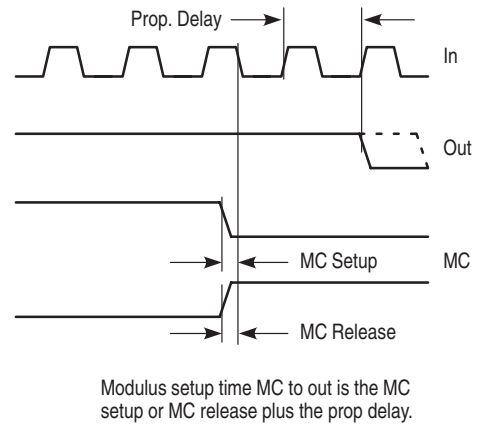


Figure 3. AC Test Circuit

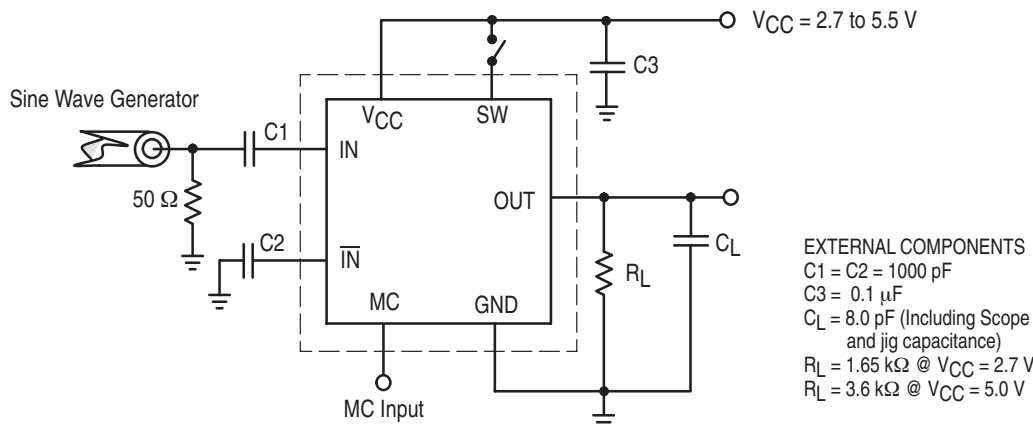


Figure 4. Generic block diagram showing prescaler connection to PLL device

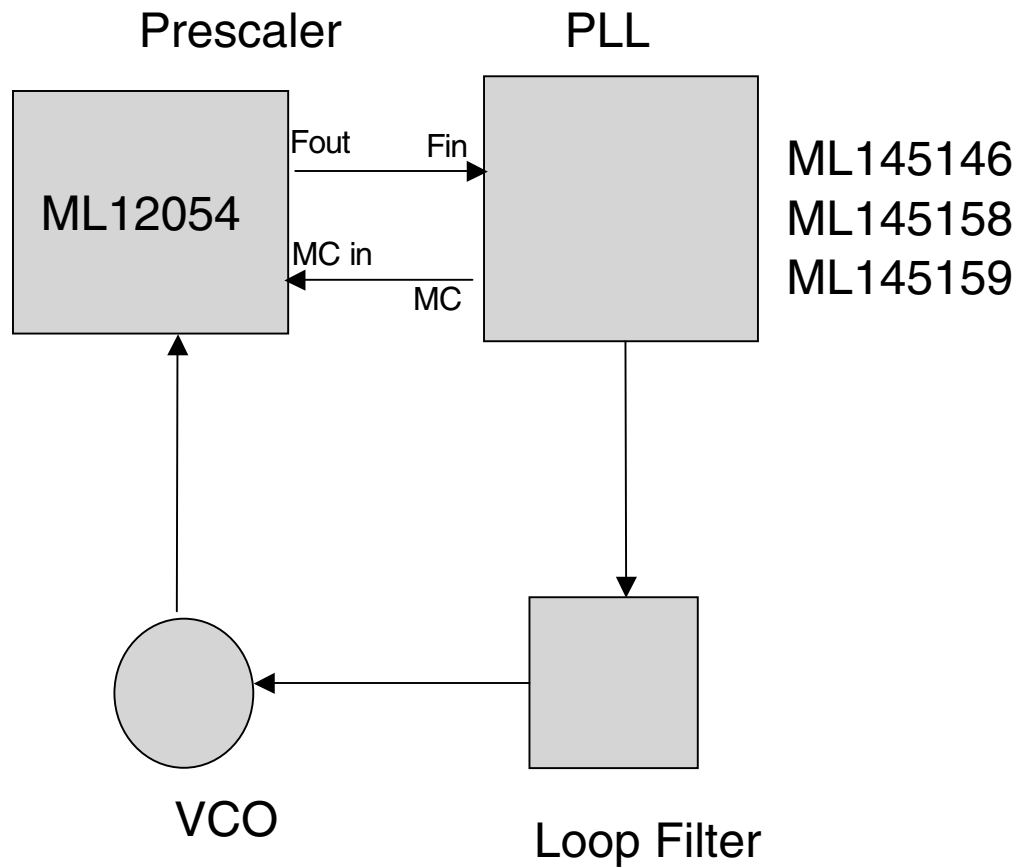
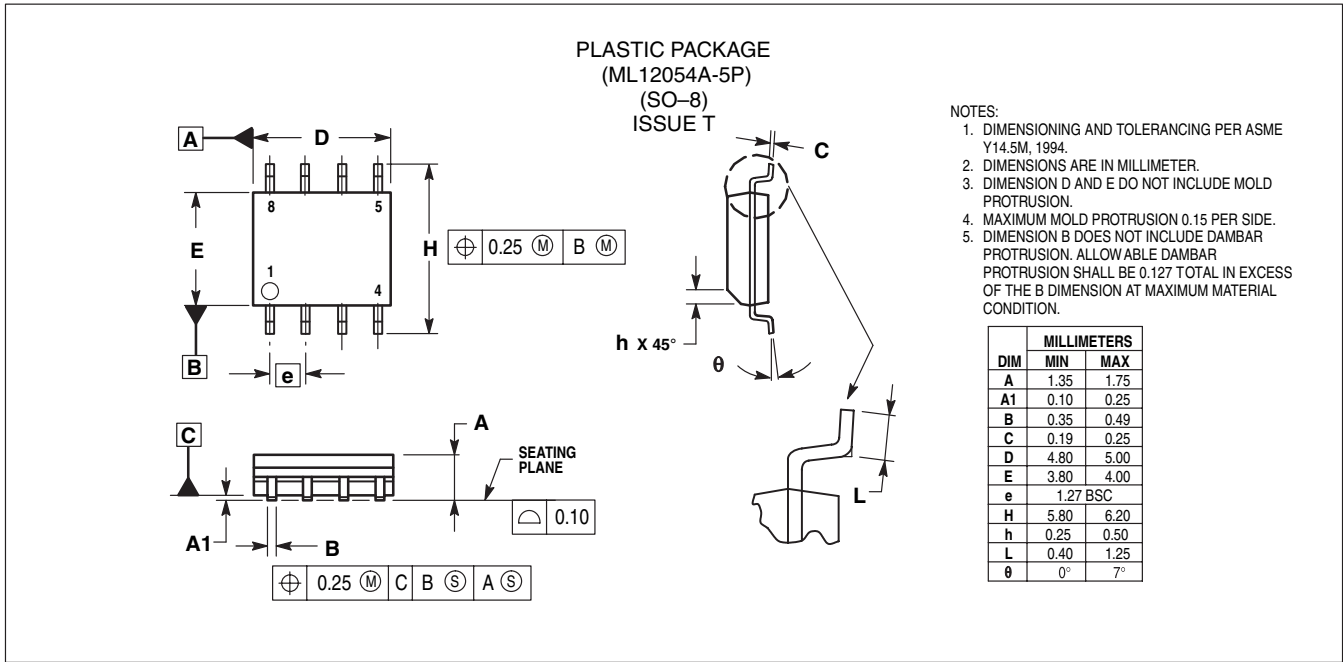


Figure 4 shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 describes using a two-modulus prescaler technique. By using prescaler higher frequencies can be achieved than by a single CMOS PLL device.

OUTLINE DIMENSIONS



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