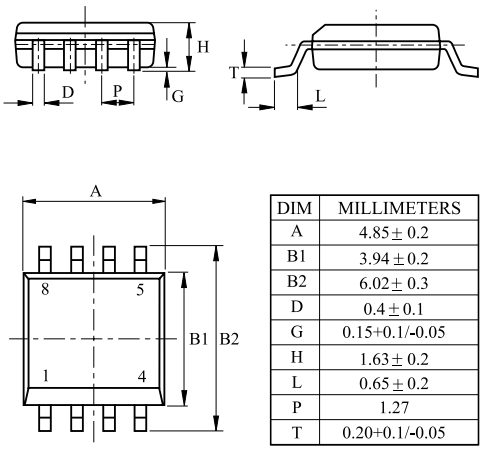
General Description

Switching regulator and DC-DC Converter applications.
It's mainly suitable for Back-light Inverter.



DIM	MILLIMETERS
A	4.85 ± 0.2
B1	3.94 ± 0.2
B2	6.02 ± 0.3
D	0.4 ± 0.1
G	0.15+0.1/-0.05
H	1.63 ± 0.2
L	0.65 ± 0.2
P	1.27
T	0.20+0.1/-0.05

FLP-8

FEATURES

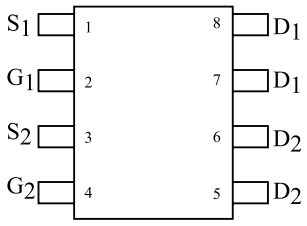
- N-Channel
  - : V_{DSS}=30V, I_D=7A.
  - : $R_{DS(ON)}$=23.5mΩ(Max.) @ V_{GS}=10V
  - : $R_{DS(ON)}$=39mΩ(Max.) @ V_{GS}=4.5V
- P-Channel
  - : V_{DSS}=-30V, I_D=-5A.
  - : $R_{DS(ON)}$=45.5mΩ(Max.) @ V_{GS}=-10V
  - : $R_{DS(ON)}$=80mΩ(Max.) @ V_{GS}=-4.5V
- Super High Dense Cell Design.
- Reliable and rugged.

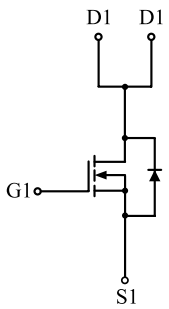
MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D*	7	-5	A
	Pulsed (note1)	I_{DP}	29	-20	
Source-Drain Diode Current		I_S	1.7	-1.7	A
Drain Power Dissipation		P_D*	2		W
Maximum Junction Temperature		T_j	150		℃
Storage Temperature Range		T_{stg}	-55 150		℃
Thermal Resistance, Junction to Ambient		R_{thJA}*	62.5		℃/W

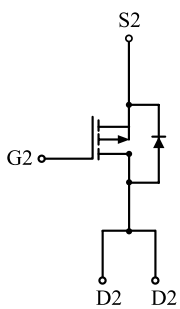
Note : *Sorface Mounted on FR4 Board

PIN CONNECTION (TOP VIEW)





N-Channel MOSFET



P-Channel MOSFET

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250 μA, V_{GS}=0V,	N-Ch	30	-	-	V
		I_D=-250 μA, V_{GS}=0V,	P-Ch	-30	-	-	
Drain Cut-off Current	I_{DSS}	V_{GS}=0V, V_{DS}=24V	N-Ch	-	-	1	μA
		V_{GS}=0V, V_{DS}=-24V	P-Ch	-	-	-1	
Gate Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	N-Ch	-	-	±100	nA
			P-Ch	-	-	±100	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250 μA	N-Ch	1.0	-	3	V
		V_{DS}=V_{GS}, I_D=-250 μA	P-Ch	-1.0	-	-3	
Drain-Source ON Resistance	$R_{DS(ON)}$*	V_{GS}=10V, I_D=7A	N-Ch	-	18	23.5	mΩ
		V_{GS}=-10V, I_D=-5A	P-Ch	-	35	45.5	
		V_{GS}=4.5V, I_D=6A	N-Ch	-	30	39	
		V_{GS}=-4.5V, I_D=-4A	P-Ch	-	62	80	
ON State Drain Current	$I_{D(ON)}$*	V_{GS}=4.5V, V_{DS}=5V	N-Ch	20	-	-	A
		V_{GS}=-10V, V_{DS}=-5V	P-Ch	-20	-	-	
Forward Transconductance	g_{fs}*	V_{DS}=5V, I_D=6.6A	N-Ch	-	10	-	S
		V_{DS}=-5V, I_D=-5A	P-Ch	-	9	-	
Source-Drain Diode Forward Voltage	V_{SD}*	I_S=1.7A, V_{GS}=0V	N-Ch	-	0.7	1.2	V
		I_S=-1.7A, V_{GS}=0V	P-Ch	-	-0.8	-1.2	

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Dynamic							
Total Gate Charge	Q_g	**N-Ch** : V_{DS}=15V, I_D=6.6A, V_{GS}=10V (Fig.1) **P-Ch** : V_{DS}=-15V, I_D=-5A, V_{GS}=-10V (Fig.3)	N-Ch	-	16.4	20.5	nC
			P-Ch	-	13	16	
		N-Ch : V_{DS}=15V, I_D=6.6A, V_{GS}=4.5V (Fig.1) **P-Ch** : V_{DS}=-15V, I_D=-5A, V_{GS}=-4.5V (Fig.3)	N-Ch	-	7.2	9	
			P-Ch	-	6.25	7.8	
Gate-Source Charge	Q_{gs}	**N-Ch** : V_{DS}=15V, I_D=6.6A, V_{GS}=10V (Fig.1) **P-Ch** : V_{DS}=-15V, I_D=-5A, V_{GS}=-10V (Fig.3)	N-Ch	-	4	-	
			P-Ch	-	2.6	-	
Gate-Drain Charge	Q_{gd}		N-Ch	-	2.6	-	
			P-Ch	-	2.9	-	
Turn-on Delay time	$t_{d(on)}$	**N-Ch** : V_{DD}=15V, I_D=6.6A, V_{GS}=10V, R_G=3Ω (Fig.2) **P-Ch** : V_{DD}=-15V, V_{GS}=-10V, R_G=3Ω, R_L=2.7Ω (Fig.4)	N-Ch	-	7.4	-	ns
			P-Ch	-	4.7	-	
Turn-on Rise time	t_r		N-Ch	-	27.7	-	
			P-Ch	-	7.8	-	
Turn-off Delay time	$t_{d(off)}$		N-Ch	-	12.2	-	
			P-Ch	-	47.2	-	
Turn-off Fall time	t_f		N-Ch	-	7.6	-	
			P-Ch	-	22.6	-	
Input Capacitance	C_{iss}	**N-Ch** : V_{DS}=15V, V_{GS}=0V, f=1.0MHz **P-Ch** : V_{DS}=-15V, V_{GS}=0V, f=1.0MHz	N-Ch	-	742	-	pF
			P-Ch	-	820	-	
Output Capacitance	C_{oss}		N-Ch	-	126	-	
			P-Ch	-	137	-	
Reverse transfer Capacitance	C_{rss}		N-Ch	-	76	-	
			P-Ch	-	89	-	

Note 1>* Pulse test : Pulse width≤300μs, Duty Cycle≤2%.

N-Channel

Fig1. I_D - V_{DS}

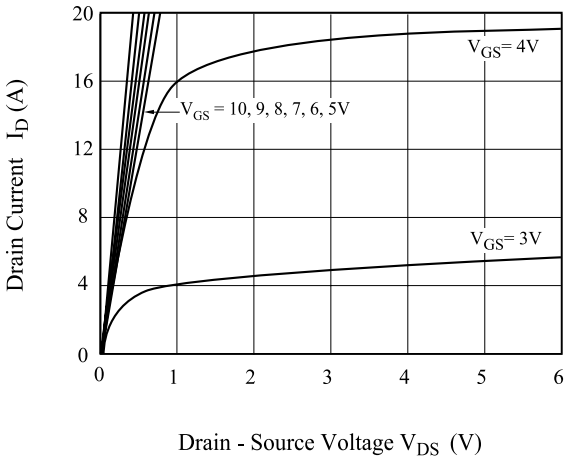


Fig2. I_D - V_{GS}

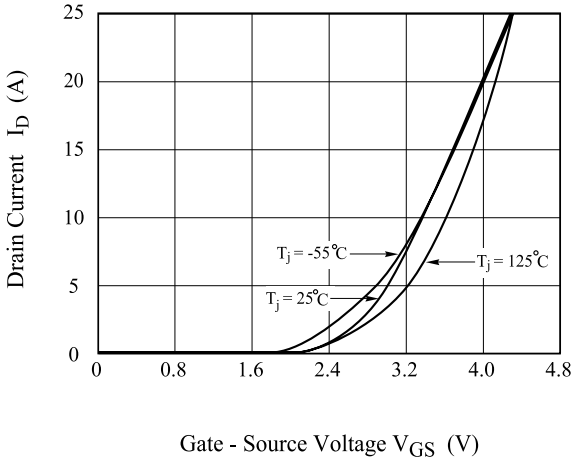


Fig3. V_{th} - T_j

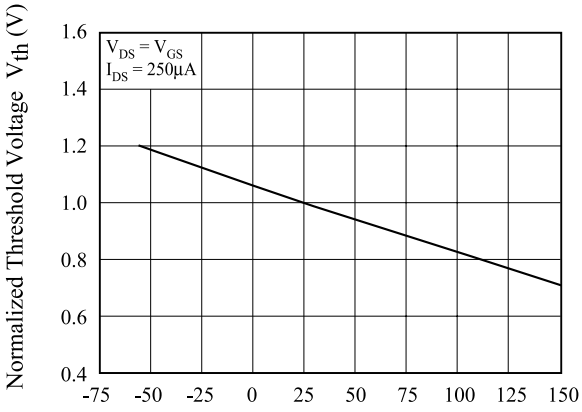


Fig4. I_{DR} - V_{SD}

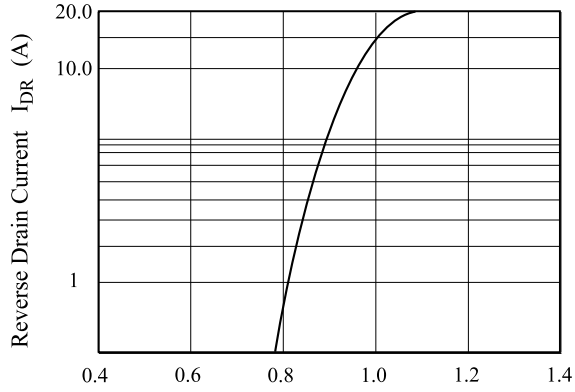


Fig5. $R_{DS(ON)}$ - T_j

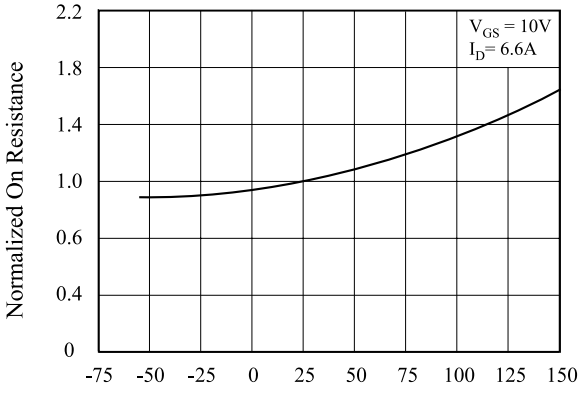


Fig6. C - V_{DS}

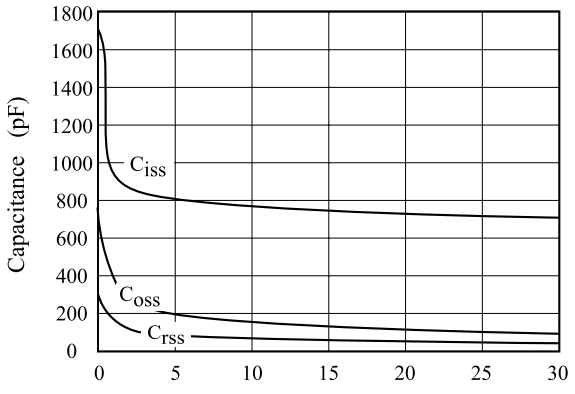


Fig7. Q_g - V_{GS}

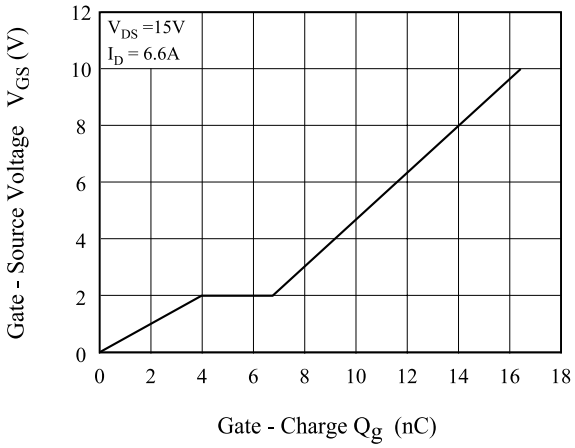


Fig8. Safe Operation Area

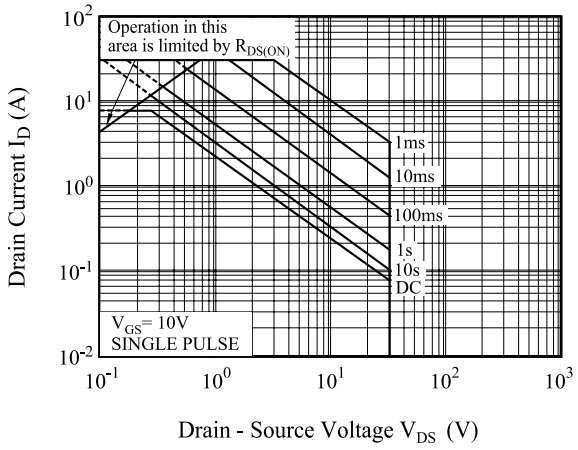
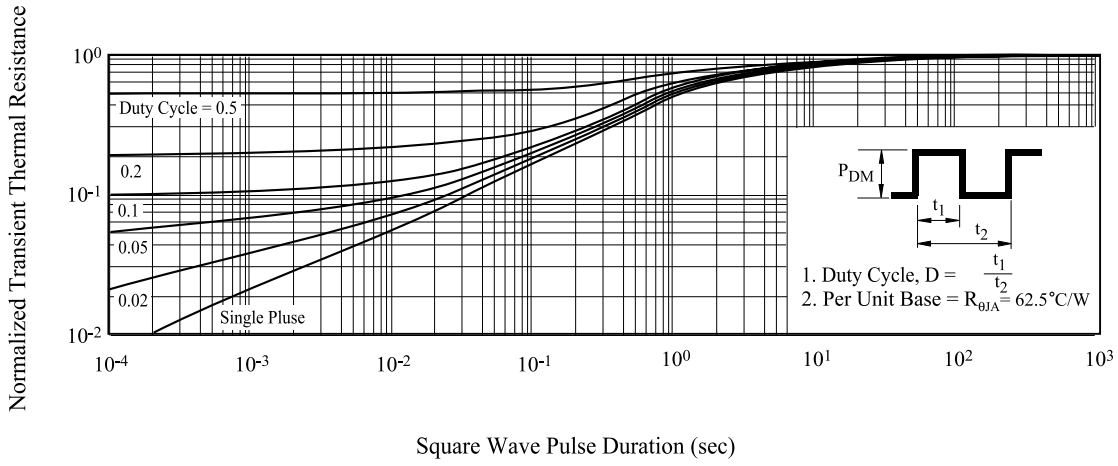


Fig9. Transient Thermal Response Curve



P-Channel

Fig1. I_D - V_{DS}

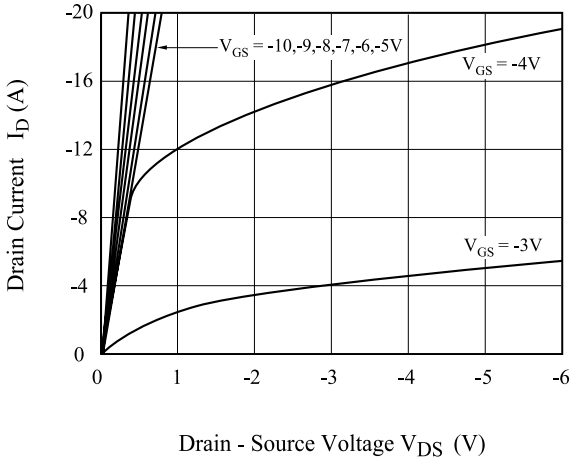


Fig2. I_D - V_{GS}

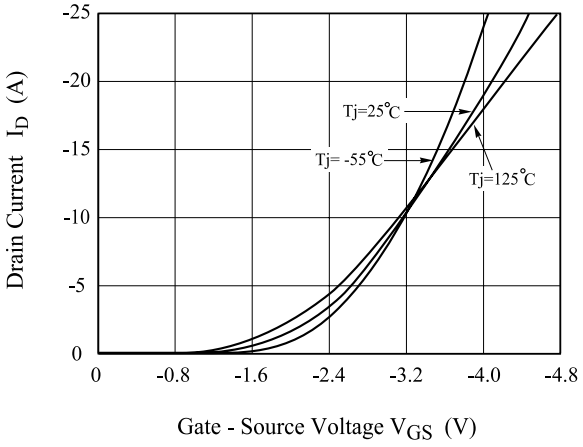


Fig3. V_{th} - T_j

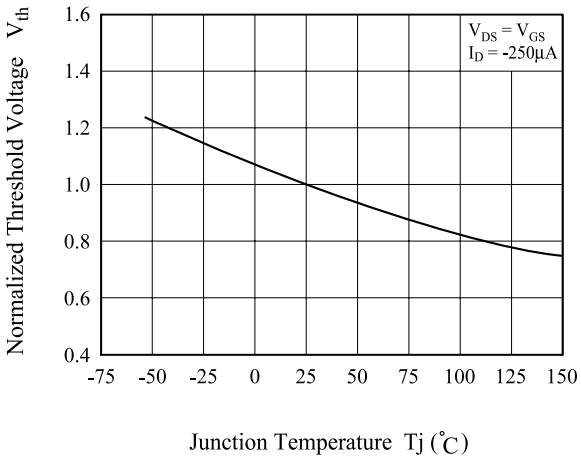


Fig4. I_{DR} - V_{SD}

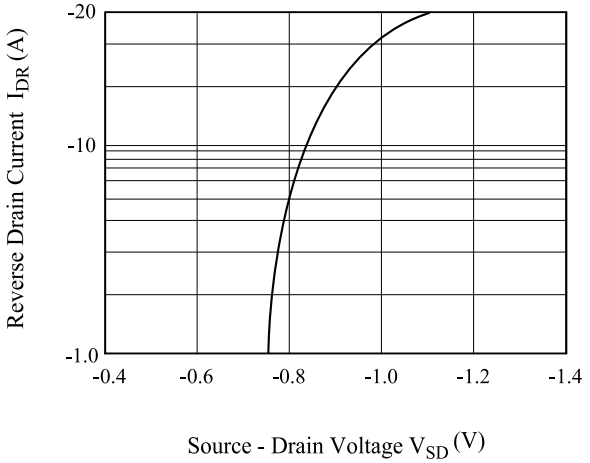


Fig5. $R_{DS(ON)}$ - T_j

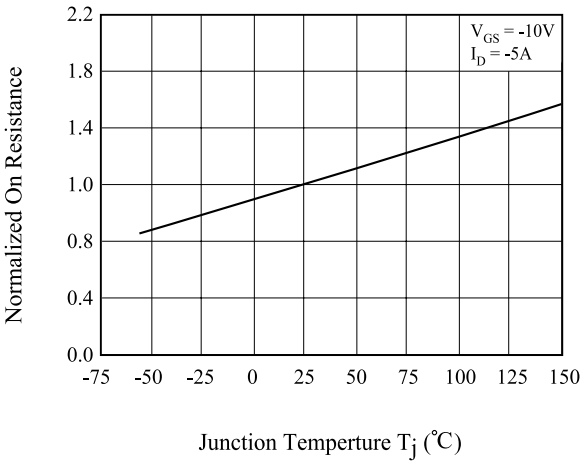


Fig6. C - V_{DS}

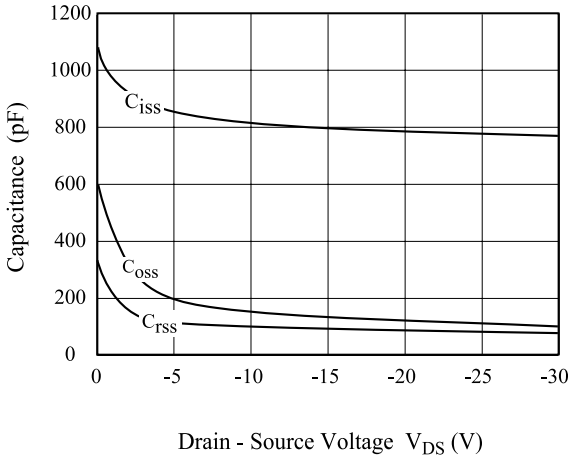


Fig7. Q_g - V_{GS}

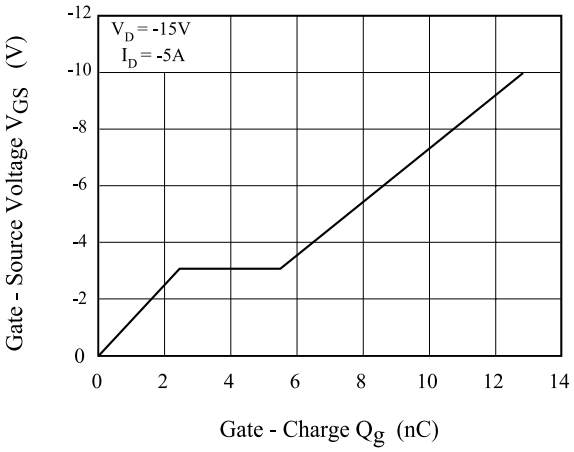


Fig8. Safe Operation Area

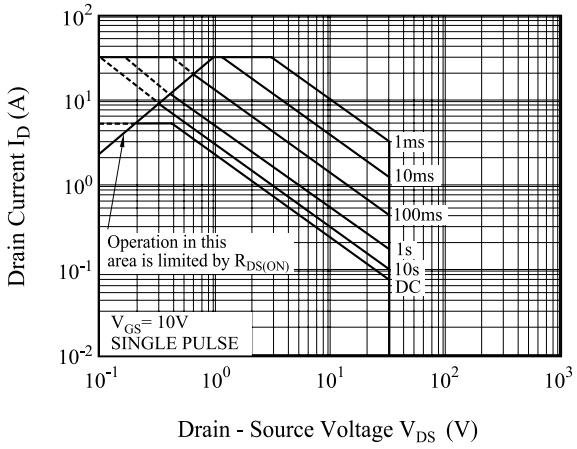
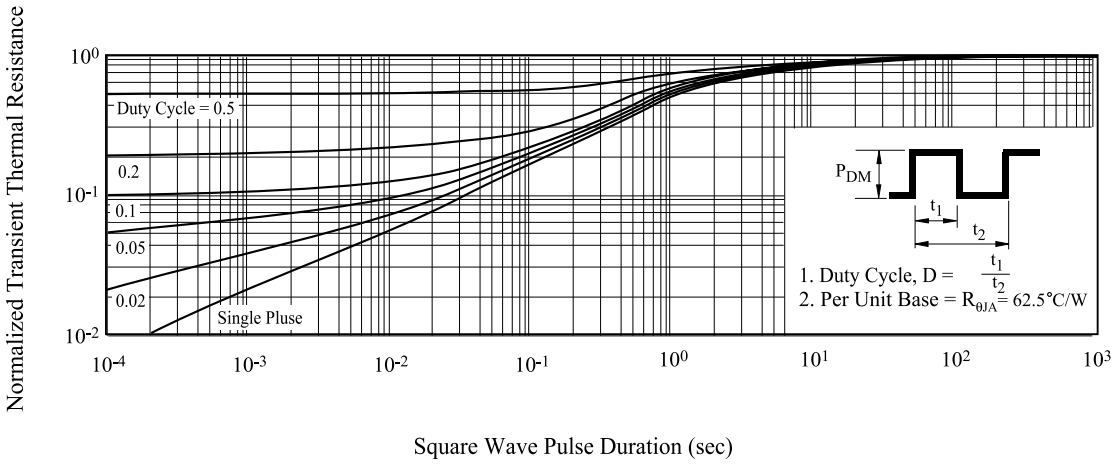
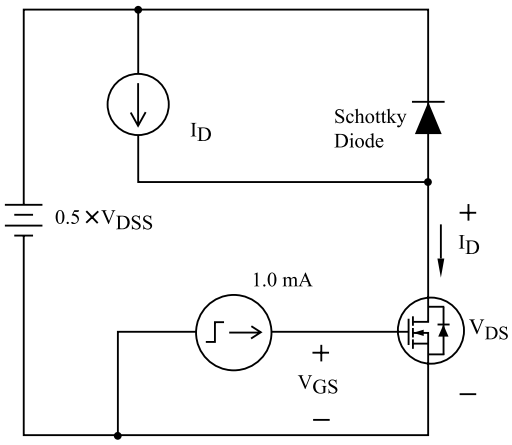


Fig9. Transient Thermal Response Curve



N-Channel

Fig. 1 Gate Charge



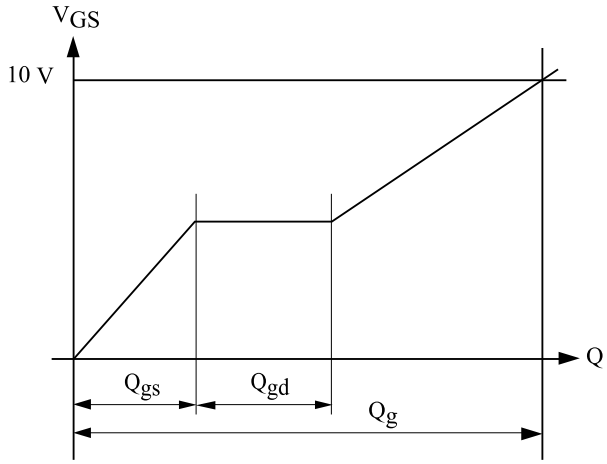
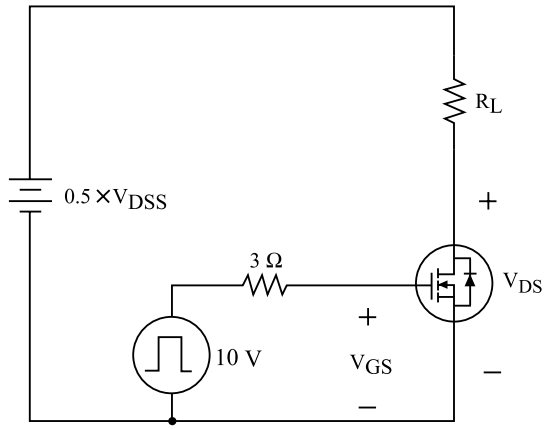
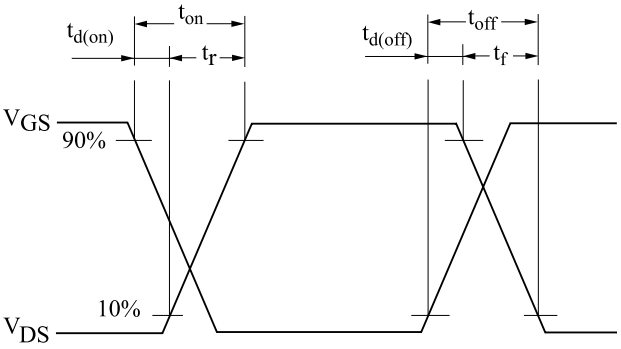


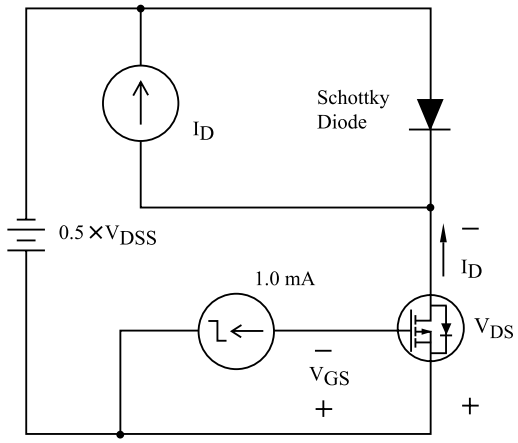
Fig. 2 Resistive Load Switching

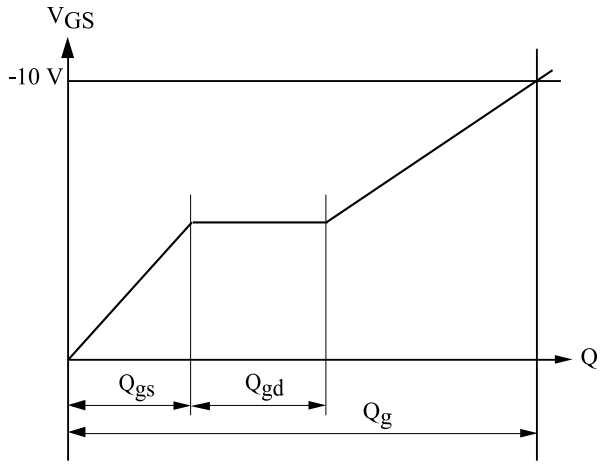




P-Channel

Fig. 1 Gate Charge





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