M65817AFP

Digital Amplifier Processor of S-Master* Technology

DESCRIPTION

The M65817AFP is a S-Master technique processor for digital amplifier enable to convert from multi liner-PCM digital input signal to high precise switching-pulse digital output without analog signal.The M65817AFP has built-in 24bit sampling rate converter and digital-gain-controller.
The M65817AFP enables to realize high precise (X`tal oscillation precision) full digital amplifier systems combining with power driver IC.

FEATURES

- Built-in 24bit Sampling Rate Converter.
  Input Signal Sampling Rate
  from 32KHz to 192KHz(24bit Maximum).
  4 kinds of Digital Input Format.
- Built-in L/R Independent Digital Gain Control.
- Built-in Soft Mute Function with Exponential Approximate-Curve.
- Correspondence for SACD signal (64Fs 1bit,Fs=44.1KHz).
- Output from Sampling Rate Converter.
- 3.3V and 5.0V Power Supply Operation at Output Clock, Input Data, and Control Signal Port

MAIN SPECIFICATION

- Master Clock
  Primary Clock: 256Fs/512Fs Secondary Clock: 1024Fs/512Fs
- Input Signal Format:
  MSB First Right Justified(16/20/24bit),MSB First Left Justified(24bit)
  LSB First Right Justified(24bit),I²S(24bit)
- Input Signal Sampling Rate from 32kHz to 192kHz.
- 8Fs Input Mode:Correspondence for External Digital Filter,Rate Converter Outputs.
- Gain Control Function:
  +30dB to -∞dB(0.1dB Step until -96dB, -136dB Minimum)
- Third Order ΔΣ(16Fs:6bit/5bit)
- Sampling Rate Converter Output :Left MSB First /LRch Independent/32BCK

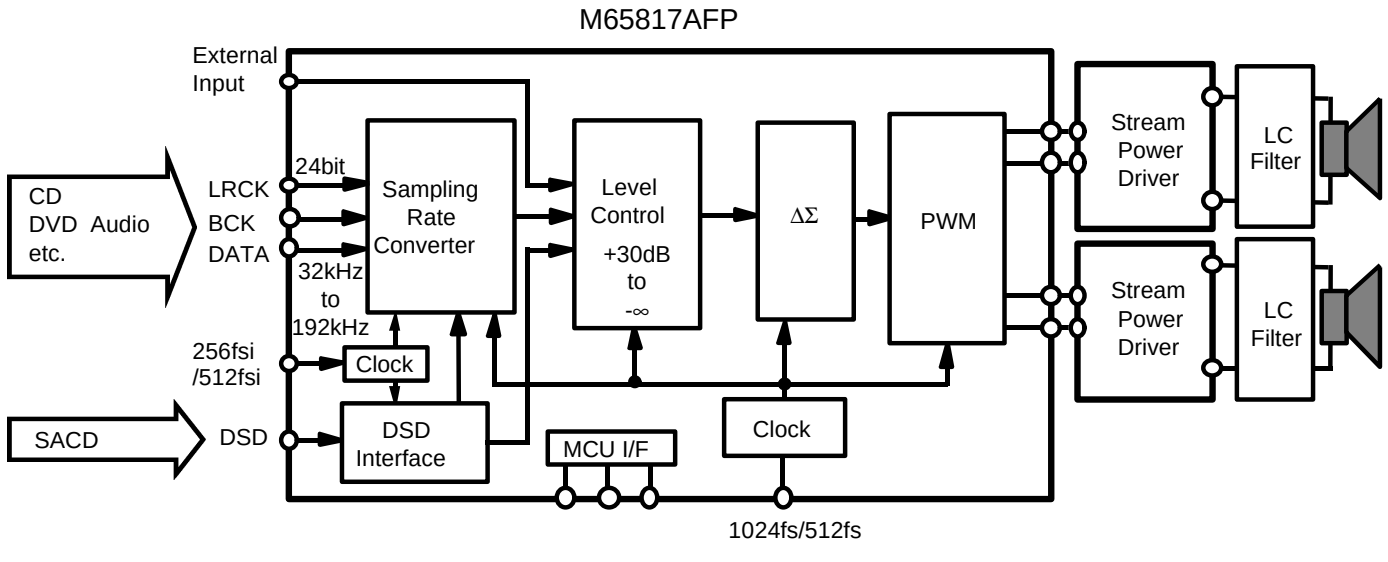
APPLICATION

DVD Receiver, AV Amplifier

RECOMMENDED OPERATING CONDITIONS

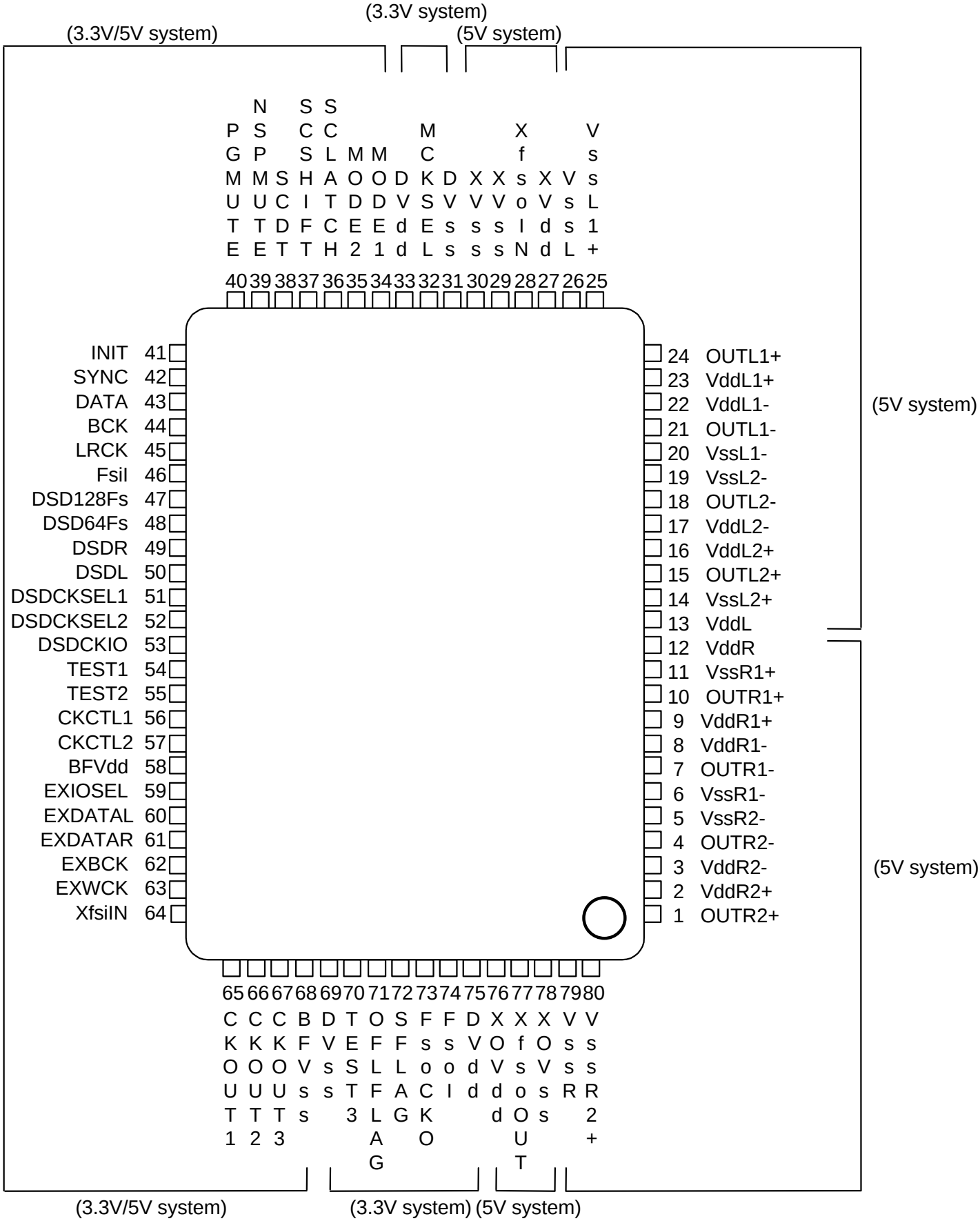
Logic Block:3.3V±10%,PWM Buffer Block :5.0V±10%

SYSTEM BLOCK DIAGRAM)

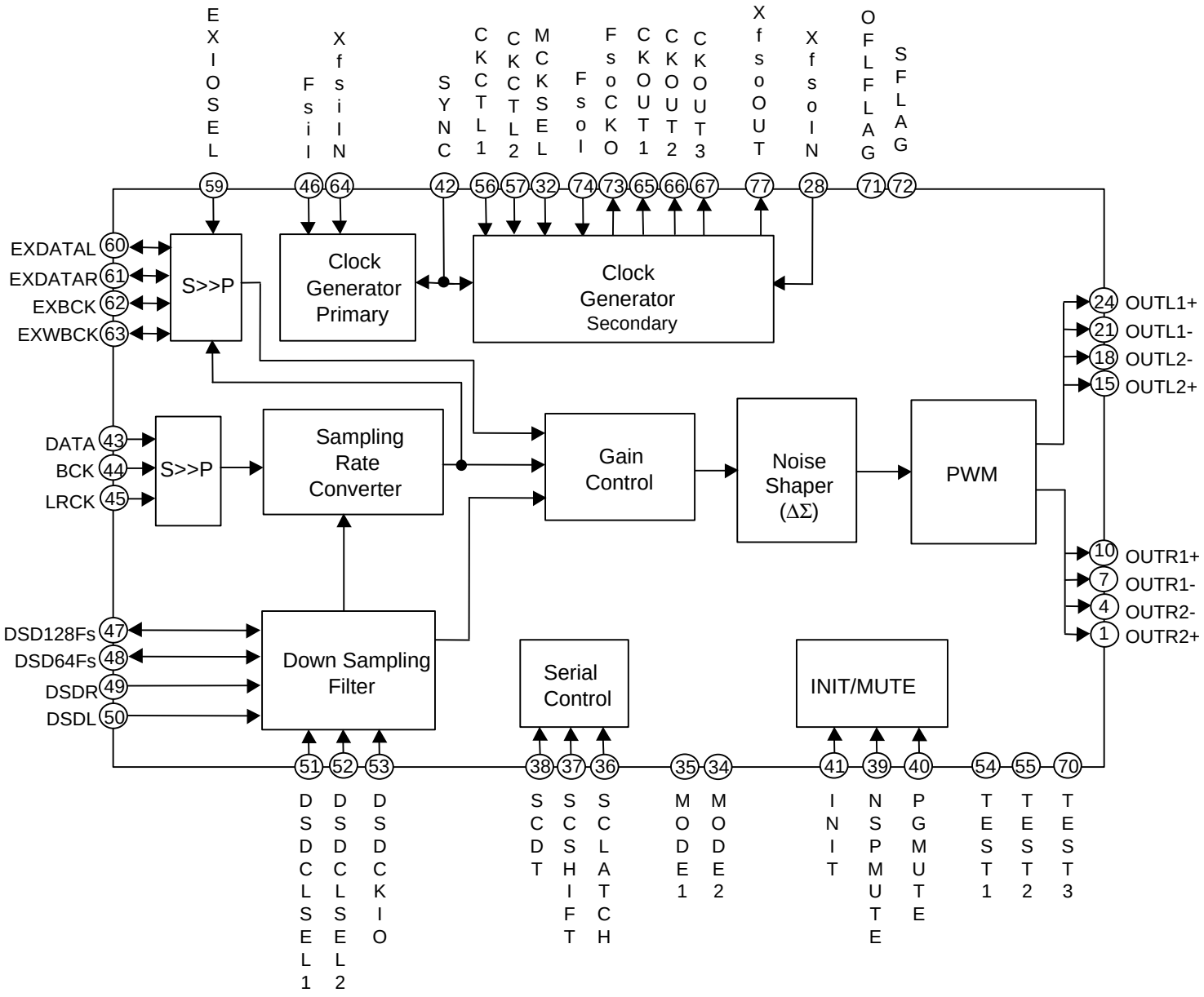


* "S-Master" is the digital amplifier technology developed by Sony Corporation. "S-Master" is a trademark of Sony Corporation.

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Supply Voltage	PWMVdd	XVdd, XOVdd, and Vdd (PWM).	-0.3	-	6.0	V
	BFVdd		-0.3	-	6.0	V
	DVdd		-0.3	-	4.2	V
Input Voltage Range	Vi (5.0V)		-0.3	-	Vdd+0.3V	V
	Vi (3.3V)		-0.3	-	Vdd+0.3V	V
Power Dissipation	Pd	Ta=60ºC		600		mW
Storage Temperature	Tstg		-40	-	125	ºC

RECOMMENDED OPERATING CONDITIONS

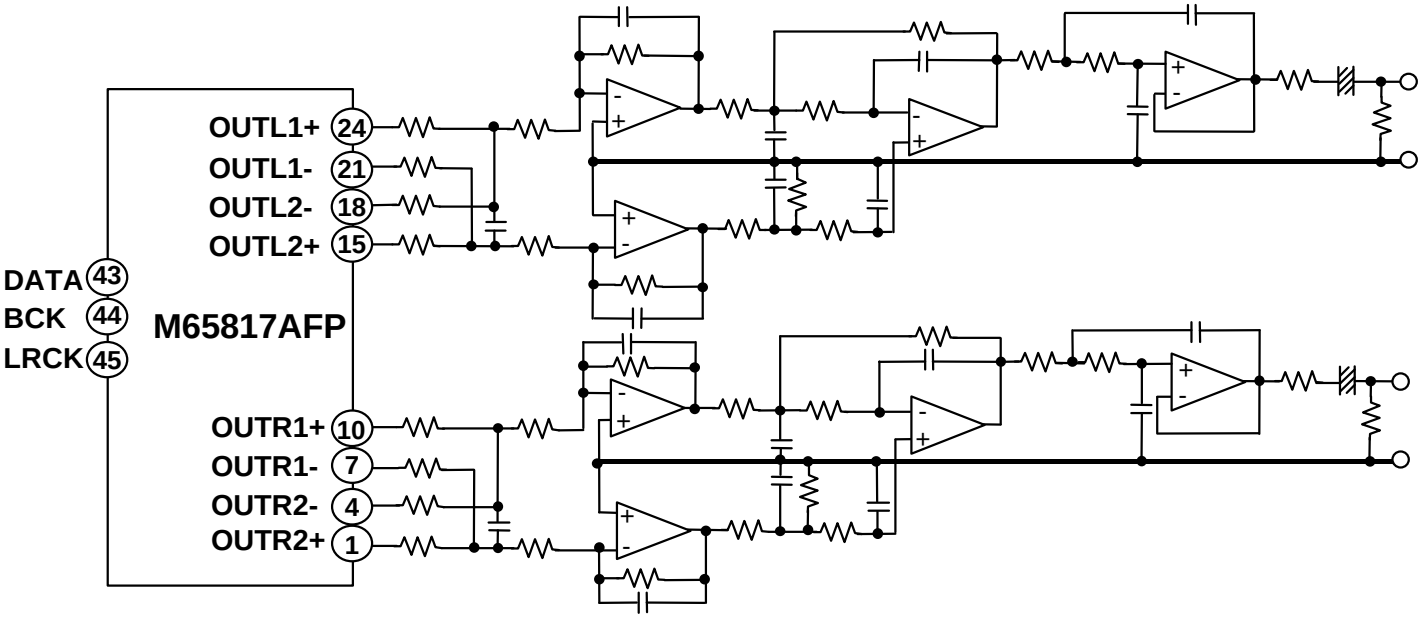
Parameter	Symbol	Conditions	Min.	Typ.	Max	Unit
Supply Voltage	PWMVdd	5V XVdd, XOVdd, and Vdd (PWM).	4.5	5.0	5.5	V
	BFVdd	5V function	4.5	5.0	5.5	V
		3.3V function	3.0	3.3	3.6	V
	DVdd		3.0	3.3	3.6	V
Operating Temperature	Ta		-10	-	60	ºC
Operating Frequency	XFsoIN		16	-	50	MHz
	XFsiIN		8	-	25	MHz

ELECTRICAL CHARACTERISTICS

(Ta=25ºC,PWMVdd=5V, DVdd=3.3V: Unless otherwise specified.)

Parameter		Symbol	Conditions	Min.	Typ.	Max	Unit
H Level Input Voltage		VIH5	BFVdd=4.5~5.5V	0.75Vdd	-	-	V
		VIH3	BFVdd=3.0~3.6V	0.75Vdd	-	-	V
L Level Input Voltage		VIL5	BFVdd=4.5~5.5V	-	-	0.25Vdd	V
		VIL3	BFVdd=3.0~3.6V	-	-	0.25Vdd	V
Input Leak Current		Ileak		-	-	10	µA
H Level Output Voltage	DSD128Fs DSD64Fs EXDATAL	VOH5	BFVdd=4.5~5.5V IOH5=-2.0mA	Vdd-0.5	-	-	V
	EXDATAR EXBCK EXWCK	VOH3	BFVdd=3.0~3.6V IOH3=-1.5mA	Vdd-0.5	-	-	V
	CKOUT1 CKOUT2	VOH5	BFVdd=4.5~5.5V IOH5=-4.0mA	Vdd-0.5	-	-	V
	CKOUT3	VOH3	BFVdd=3.0~3.6V IOH3=-3.0mA	Vdd-0.5	-	-	V
	XfsoOUT	VOH5	BFVdd=4.5~5.5V IOH5=-2.0mA	Vdd-0.5	-	-	V
	OFLFAG SFLAG FsoCKO	VOH3	BFVdd=3.0~3.6V IOH3=-2.0mA	Vdd-0.5	-	-	V
L Level Output Voltage	DSD128Fs DSD64Fs EXDATAL	VOL5	BFVdd=4.5~5.5V IOH5=2.0mA	-	-	0.5	V
	EXDATAR EXBCK EXWCK	VOL3	BFVdd=3.0~3.6V IOH3=1.5mA	-	-	0.5	V
	CKOUT1 CKOUT2	VOL5	BFVdd=4.5~5.5V IOH5=4.0mA	-	-	0.5	V
	CKOUT3	VOL3	BFVdd=3.0~3.6V IOH3=3.0mA	-	-	0.5	V
	XfsoOUT	VOL5	BFVdd=4.5~5.5V IOH5=2.0mA	-	-	0.5	V
	OFLFAG SFLAG FsoCKO	VOL3	BFVdd=3.0~3.6V IOH3=2.0mA	-	-	0.5	V
Power Supply Current		Idd	BFVdd=5V		33		mA

Characteristics Evaluation Circuit



Reference Characteristic		Conditions
S/N	103dB(typ)	•Input:1kHz sine wave •Fs:Primary, Secondary 48kHz •AC dithering E •DC dithering:0.1% •Gain Data Setting:(Index)10000b/(Mantissa)10000000b •THD+N:Filter 20kHz LPF S/N:Filter 22kHz LPF+JIS-A
THD+N	0.0015%(typ)	

PIN DESCRIPTION

Pin No.	Name	I/O	Description	Input Type	Output Current 5V/3.3V	Signal Level
1	OUTR2+	O	Rch PWM2(+) Output	-		5V
2	VddR2+		Power Supply for Rch PWM2(+) (5V)	-	-	-
3	VddR2-		Power Supply for Rch PWM2(-) (5V)	-	-	-
4	OUTR2-	O	Rch PWM2 (-) Output	-		5V
5	VssR2-		GND for Rch PWM2(-)	-	-	-
6	VssR1-		GND for Rch PWM1(-)	-	-	-
7	OUTR1-	O	Rch PWM1 (-) Output	-		5V
8	VddR1-		Power Supply for Rch PWM1(-) (5V)	-	-	-
9	VddR1+		Power Supply for Rch PWM1(+) (5V)	-	-	-
10	OUTR1+	O	Rch PWM1 (+) Output	-		5V
11	VssR1+		GND for Rch PWM1(+)	-	-	-
12	VddR		Power Supply for Rch PWM (5V)	-	-	-
13	VddL		Power Supply for Lch PWM (5V)	-	-	-
14	VssL2+		GND for Lch PWM2(+)	-	-	-
15	OUTL2+	O	Lch PWM2 (+) Output	-		5V
16	VddL2+		Power Supply for Lch PWM2(+) (5V)	-	-	-
17	VddL2-		Power Supply for Lch PWM2(-) (5V)	-	-	-
18	OUTL2-	O	Lch PWM2 (-) Output	-		5V
19	VssL2-		GND for Lch PWM2(-)	-	-	-
20	VssL1-		GND for Lch PWM1(-)	-	-	-
21	OUTL1-	O	Lch PWM1 (-) Output	-		5V
22	VddL1-		Power Supply for Lch PWM1(-) (5V)	-	-	-
23	VddL1+		Power Supply for Lch PWM1(+) (5V)	-	-	-
24	OUTL1+	O	Lch PWM1 (+) Output	-		5V
25	VssL1+		GND for Lch PWM1(+)	-	-	-
26	VssL		GND for Lch PWM	-	-	-
27	XVdd		Power Supply for Master Clock Buffer	-	-	-
28	XfsoIN	I	Secondary Master Clock Input:1024Fso/512Fso	Normal	-	5V
29	XVss		GND for Master Clock Buffer	-	-	-
30	XVss		GND for Master Clock Buffer	-	-	-
31	DVss		GND for Digital Block	-	-	-
32	MCKSEL	I	Secondary Master Clock Selection; L:1024Fso, H:512Fso	Normal	-	3.3V
33	DVdd		Power Supply for Digital Block (3.3V)	-	-	-
34	MODE1	I	Input Mode Selection 1	Schmitt	-	5V/3.3V
35	MODE2	I	Input Mode Selection 2	Schmitt	-	5V/3.3V
36	SCLATCH	I	Serial Control•Latch Signal Input	Schmitt	-	5V/3.3V
37	SCSHIFT	I	Serial Control•Shift Clock Input	Schmitt	-	5V/3.3V
38	SCDT	I	Serial Control•Data Input	Schmitt	-	5V/3.3V
39	NSPMUTE	I	PWM Duty 50% Mute (L :Active)	Schmitt	-	5V/3.3V
40	PGMUTE	I	PWM G-MUTE(L :Active)	Schmitt	-	5V/3.3V

Pin No.	Name	I/O	Description	Input Type	Output Current 5V/3.3V	Signal Level
41	INIT	I	Initialize Input(Power Supply Reset): ; L:Reset, H:Release	Schmitt	-	5V/3.3V
42	SYNC	I	Synchronous Set of System Clock (at Rising Edge)	Schmitt	-	5V/3.3V
43	DATA	I	DATA Input (CD/MD / DVD audio mode)	Normal	-	5V/3.3V
44	BCK	I	BCK Input (CD/MD / DVD audio mode)	Schmitt	-	5V/3.3V
45	LRCK	I	LRCK Input (CD/MD / DVD audio mode)	Schmitt	-	5V/3.3V
46	FsiI	I	Primary Fsi Clock Input (SACD mode)	Schmitt	-	5V/3.3V
47	DSD128Fs	I/O	SACD Interface Clock(128Fs)	Schmitt	2mA/1.5mA	5V/3.3V
48	DSD64Fs	I/O	SACD Interface Clock(64Fs)	Schmitt	2mA/1.5mA	5V/3.3V
49	DSDR	I	SACD Rch Data Input	Normal	-	5V/3.3V
50	DSDL	I	SACD Lch Data Input	Normal	-	5V/3.3V
51	DSDCKSEL1	I	SACD Interface Selection 1	Normal	-	5V/3.3V
52	DSDCKSEL2	I	SACD Interface Selection 2	Normal	-	5V/3.3V
53	DSDCKIO	I	I/O Selection for SACD(64Fs,128Fs)Clock L:input,H:output	Normal	-	5V/3.3V
54	TEST1	I	TEST1 must be connected to GND.	Normal	-	5V/3.3V
55	TEST2	I	TEST2 must be connected to GND.	Normal	-	5V/3.3V
56	CKCTL1	I	fso System Clock(CKOUT1,2,3) Output Selection 1	Normal	-	5V/3.3V
57	CKCTL2	I	fso System Clock(CKOUT1,2,3) Output Selection 2	Normal	-	5V/3.3V
58	BFVdd		Power Supply for Input/Output (3.3V/5V)Buffer	-	-	-
59	EXIOSEL	I	8Fs Data Input/Output Selection L:Input H:Output	Normal	-	5V/3.3V
60	EXDATAL	I/O	8Fs Data Lch	Normal	2mA/1.5mA	5V/3.3V
61	EXDATAR	I/O	8Fs Data Rch	Normal	2mA/1.5mA	5V/3.3V
62	EXBCK	I/O	BCK for 8fs Data (32BCK=1WCK)	Schmitt	2mA/1.5mA	5V/3.3V
63	EXWCK	I/O	Word Clock for 8fs Data (1WCK=32BCK)	Schmitt	2mA/1.5mA	5V/3.3V
64	XfsiIN	I	Primary Master Clock Input (256fsi/512fsi/256fso/512fso)	Normal	-	5V/3.3V
65	CKOUT1	O	fso System Clock Output 1	-	4mA/3mA	5V/3.3V
66	CKOUT2	O	fso System Clock Output 2	-	4mA/3mA	5V/3.3V
67	CKOUT3	O	fso System Clock Output 3	-	4mA/3mA	5V/3.3V
68	BFVss		GND for Digital Block Input/Output Buffer	-	-	-
69	DVss		GND for Digital Block	-	-	-
70	TEST3	I	TEST3 must be connected to GND.	Normal	-	3.3V
71	OFLFLAG	O	Overflow Detector Flag of Digital Operation (H :Active)	-	2mA	3.3V
72	SFLAG	O	Asynchronous Flag (H :Active)	-	2mA	3.3V
73	FsoCKO	O	Secondary Fso Clock Output	-	4mA	3.3V
74	FsoI	I	Secondary Fso Clock Input	Schmitt	-	3.3V
75	DVdd		Power Supply for Digital Block(3.3V)	-	-	-
76	XOVdd		Power Supply for Secondary Master Clock Buffer(5V)	-	-	-
77	XfsoOUT	O	Buffered Output of Secondary Master Clock (1024/512fso)	-	2mA	5V
78	XOVss		GND for Secondary Master Clock Buffer(1024/512fso)	-	-	-
79	VssR		GND for Rch PWM	-	-	-
80	VssR2+		GND for Rch PWM2(+)	-	-	-

EXPLANATION OF OPERATION

1. Pin Setting.

1-1. MODE1, MODE2 (34) (35)

The states of **MODE1** and **MODE2** pins select input signal mode.

MODE1 and **MODE2** are control pins for input signal mode (Normal/SACD/External Rate Converter 8fs Input).

These are selectable as follows.

Pin	Name \ Mode	*Normal*	*External Rate Converter 8fs*	*SACD-fsi*	*SACD-fso*
34	MOD	L	L	H	H
35	MOD	L	H	L	H

♦*Normal* mode

The *Normal* is data input mode from CD,MD,DVD etc.

Input pins are **DATA, BCK** and **LRCK** .

♦*External Rate Converter 8fs* mode

The *External Rate Converter 8fs* is data input mode from external source without using Rate Converter Block. Input pins are **EXBCK**, **EXWCK**, **EXDATAL** and **EXDATAR** .

♦*SACD-fsi* mode

The *SACD-fsi* is data input mode on SACD format with synchronized primary clock.

Input pins are **DSDL, DSDR, DSD128Fs** and **DSD64Fs** .

♦*SACD-fso* mode

The *SACD-fso* is data input mode on SACD format with synchronized secondary clock.

Input pins are **DSDL, DSDR, DSD128Fs** and **DSD64Fs** .

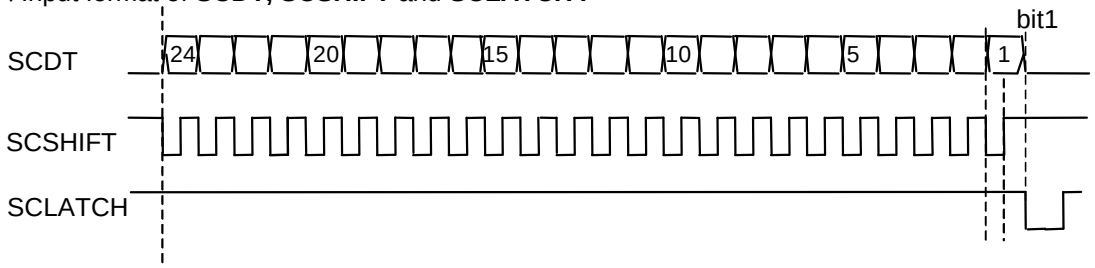
* primary clock: This clock means input side clock system of rate converter.
secondary clock: This clock means output side clock system of rate converter. This clock makes to operate after Rate Converter Block(Gain Control Block, ΔΣ Block and PWM Block).

1-2. SCDT,SCSHIFT,SCLATCH (38) (37) (36)

SCDT,SCSHIFT, and **SCLATCH** are input pins for setting M65817AFP's operation.

Input format of **SCDT, SCSHIFT** and **SCLATCH** is shown below.

♦Input format of **SCDT, SCSHIFT** and **SCLATCH .**



♦Description of Operation Mode

Operating Mode are classified in four and assigned by bit1and bit2. These four functions are shown below.

(bit1 and bit2) = : (L and L) Gain Control Mode: Gain control.
(bit1 and bit2) = : (L and H) System1 Mode: Primary block initialization, etc.
(bit1 and bit2) = : (H and L) System2 Mode: Secondary block initialization, etc.
(bit1 and bit2) = : (H and H) Test Mode(setting prohibition)

These four detail functions are shown in Page17.

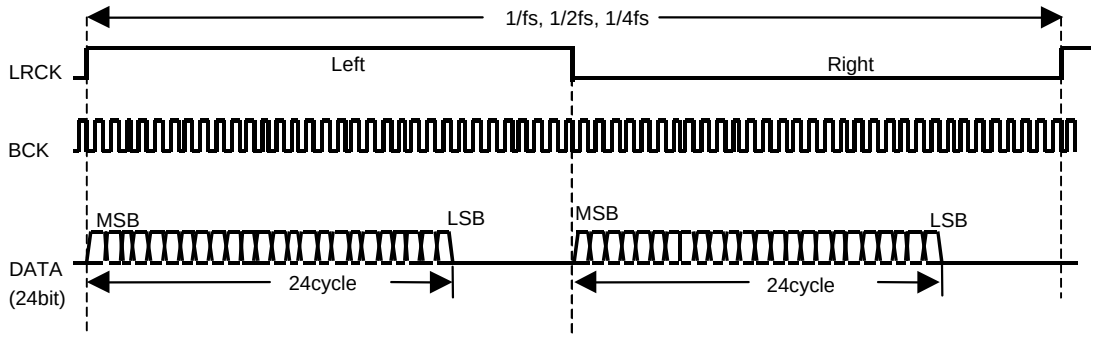
1-3. DATA,BCK,LRCK 43 44 45

DATA, BCK and **LRCK** are input pins under condition of ` *Normal* ` mode.
Input formats are supported by following 4 ways, and are set by Serial Control, "System1 Mode, bit3 and bit4". Input data length are selectable in a case of "MSB First Right Justified" (Serial Control "System1 Mode,bit5 and bit6").

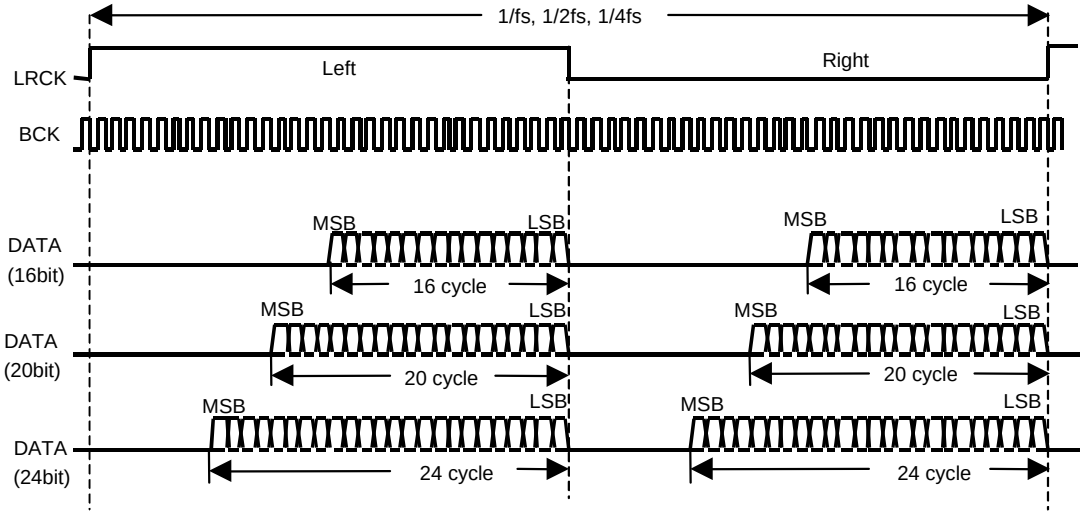
Input formats are shown in following figures.

♦Input Formats of **DATA, BCK** and **LRCK**

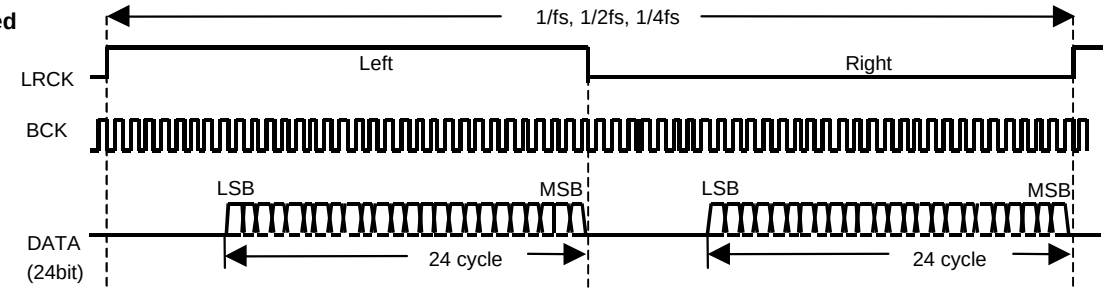
MSB first left justified (24bit)



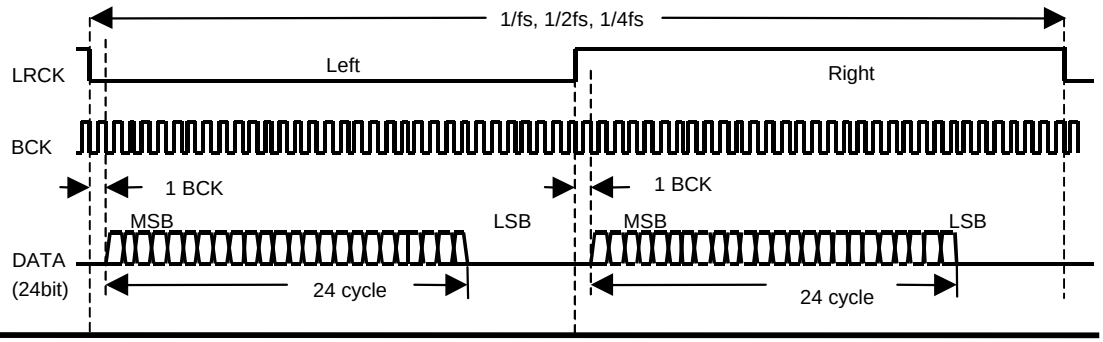
MSB first right justified (16bit, 20bit, 24bit)



LSB first right justified (24bit)



I²S(24bit)



1-4. EXBCK,EXWCK,EXDATAL,EXDATAR,EXIOSEL (62) (63) (60) (61) (59)

These are Input pins on "External sampling rate converter 8fs mode". In case of no usage , from **59** pin to **63** pin should be tied to "low" .
But when EXIOSEL is set the condition to "H" on no usage mode,
EXDATAL,EXDATAR are changed to output terminals for sampling rate converter.
This function's detail explanation is shown in Page14 .

1-5. DSDL,DSDR,DSD128Fs,DSD64Fs,DSDCKSEL1,DSDCKSEL2,DSDCKIO (50) (49) (47) (48) (51) (52) (53)

These are Input pins used on **SACD-fsi Mode** or **SACD-fso Mode.**
In case of no usage,from 47 pin to 53 pin should be tied to "low".

This function's detail explanation is shown in Page15 .

1-6. MCKCEL,XfsoIN,XfsoOUT (32) (28) (77)

XfsoIN pin is secondary master clock input.
The state of **MCKSEL** pin selects secondary master clock.

MCKSEL	XfsoIN
L	1024fs
H	512fs

XfsoOUT pin is buffered-output from **XfsoIN** pin's input clock.

1-7. XfsiIN (64)

XfsiIN pin is primary master clock input.
Frequency of primary master clock must be selected by the serial control "System2 Mode,bit3".
The state of **IMCKSEL** pin selects primary master clock.

bit3(IMCKSEL)	XfsiIN
H	512fs
L	256fs

1-8. CKCTL1,CKCTL2,CKOUT1,CKOUT2,CKOUT3 (56) (57) (65) (66) (67)

CKOUT1, CKOUT2 and **CKOUT3** pins are divided-clock output from secondary clock.
At power on, these frequency is free-running.
The states of CKCTL1 and CKCTL2 pins selects clock frequency of CKOUT1,CKOUT2 and CKOUT3 pins.

The setting table of **CKCTL1** and **CKCTL2** pins is shown below.

CKCTL1	CKCTL2	CKOUT1	CKOUT2	CKOUT3
L	L	L	L	L
L	H	256Fso	16Fso	8Fso
H	L	512Fso	256Fso	16Fso
H	H	512Fso	256Fso	8Fso

1-9. FsoCKO (73)

FsoCKO is clock output pin of 1Fs frequency. The output is divided-clock of **XfsoIN**, and frequency is free-running at power on. **FsoCKO** pin's clock is utilized for a synchronization in case that have used plural M65817AFP,take a synchronization between M65817AFP and other external devices.
Detail explanation is shown in next paragraph, "**SYNC** ".

1-10. SYNC,FsoI,FsiI,SFLAG

42 74 46 72

SYNC pin is input for resynchronization. **FsoI** and **FsiI** pins are clock input for synchronized operation.
SFLAG pin is output for Asynchronous Flag. It is necessary of synchronized operation between M65817AFP and other input-source-devices. Therefore the M65817AFP is operated by the synchronized clocks,Fsol(1fs), Fsil(1fs),and LRCK(1/2/4fs).The M65817AFP detects rise edge of these synchronized-clocks in normal operation, and the M65817AFP does a treatment of resynchronization in case that the cycle has changed. In addition, the M65817AFP re-synchronizes for a synchronized clock, in case that the M65817AFP detects **SYNC** pin's rise edge ,too. This rise edge detective function is effective for stable operation in case of power-on and change of input source, this '**SYNC**' function is able to do at Serial Control(System2 mode, bit6:Page17 in detail),too. For a period of resynchronization, **SFLAG** pin output "**H**" and output signal is muted ,The synchronization clock is differed by input signal mode.
These relations are shown in following table.

Input Signal Mode	`Synchronization detection` clock	
	Primary Side	Secondary Side
Normal	**LRCK**	**FsoI**
External Rate Converter 8fs	———	**FsoI**
SACD-fsi	**FsiI**	**FsoI**
SACD-fso	———	**FsoI**

In case of using Multiplex(for multi channel application) and Single(for 2ch application) , detail explanation is shown below.(Input signal mode is "Normal")

♦*Normal* Mode (34 pin="L",35 pin="L")

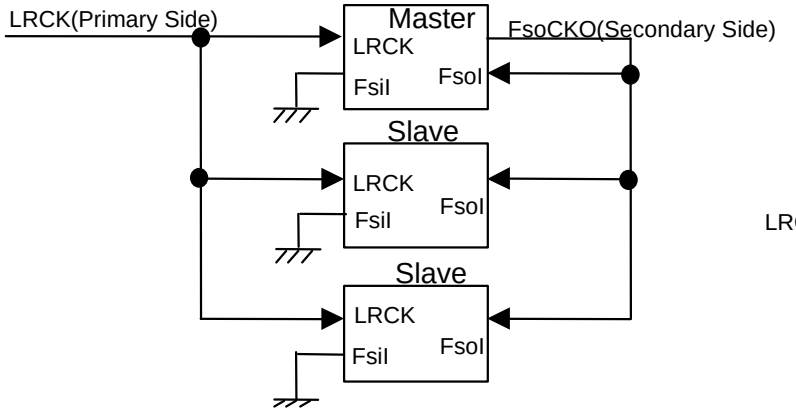
Multiplex use

The primary clock must be entered into each **LRCK** pins of M65817AFP, therefore primary clock side of plural M65817AFP is done with synchronization.
The secondary clock must be generated from arbitrary one master-M65817AFP`s **FsoCKO** pin and be entered each **FsoI** pins of slave-M65817AFP(inclusive master-M65817AFP) with synchronization.

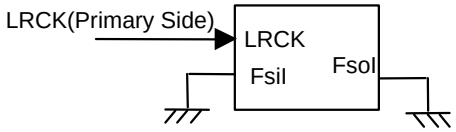
Single use

The primary clock must be entered into **LRCK** pin of M65817AFP, therefore primary clock side of M65817AFP is done with synchronization.
The secondary clock can be entered from FsoCKO pin into FsoI pin with synchronization.
As the other way, the secondary clock may not be entered into **FsoI** pin,
however in this case, the ASYNCEN2 register flag in System Control must be set `disable`, secondary-asynchronous-detection.

Under `*Normal*` mode, M65817AFP always treats synchronous detection between **LRCK** pin's clock and primary clock in M65817AFP.This detection has a priority rather than Serial Control:ASYNCEN1, therefore the synchronous detection does as ` forced-enable`, regardless of ASYNCEN value.



Multiplex use (6ch)



Single use (2ch)

*Refer to Page14 and Page15 about circuit examples in case that input signal modes are `*External Rate Converter 8fs*`, `*SACD-fsi*`, and `*SACD-fso*`.

1-11. OFLFLAG (71)

OFLFLAG pin is output for the 'over flow flag' in the operation. **OFLFLAG** pin outputs "H" level by detection of over flow from Gain Control Block and others. The "H" level width is over 0.6msec, so detection result is held.

1-12. NSPMUTE (39)

NSPMUTE pin is input to make for PWM output to 50% duty mute.

"L": PWM output 50% duty Mute. '"H": Mute release.

1-13. PGMUTE (40)

PGMUTE pin is input to make PWM output to absolute zero mute.

"L": PWM output mute.

OUTL1 (+), OUTL2 (+), OUTR1 (+), OUTR2 (+) : "L" fixed

OUTL1 (-), OUTL2 (-), OUTR1 (-), OUTR2 (-) : "H" fixed

"H": MUTE release.

1-14. INIT (41)

INIT pin is input for reset to all the function of M65817AFP.

"L" level : (1). Clear of data memory. (2). Initialization of Serial Control. (3). PWM output Duty 50 %.

"L" period needs more than 5 msec.

"H" level : usual operation.

"L">"H" rise edge: Resynchronization treatment, which is same at SYNC function.

1-15. TEST1,TEST2,TEST3

TEST1,TEST2, and **TEST3** pins are test input for factory shipping test of M65817AFP.

TEST1,TEST2, and **TEST3** pins must be tied to "L" level on usual operation.

1-16. Power Supply and GND

Power supply and GND routes have 5 isolated lines.

(1) **VddL1+, VssL1+, VddL1-, VssL1-, VddL2+, VssL2+, VddL2,-, VssL2 - ,VddR1+, VssR1+, VddR1-, VssR1-, VddR2+, VssR2+, VddR2, -, VssR2 - ,VssL, VddL, VssR, VddR**

These pins are Power supply and GND for PWM output buffer block.

Power Supply voltage must be fixed at 5.0V.

(2) **XVdd, XVss**(29pin) **,XVss**(30pin) (27) (29) (30)

These pins are Power supply and GND for XfsoIN clock input block.

Power Supply voltage must be fixed at 5.0V.

(3) **XOVdd, XOVss** (76) (78)

These pins are Power supply and GND for XfsoOUT clock output block.

Power Supply voltage must be fixed at 5.0V.

(4) **DVdd, DVss** (33) (31) (75) (69)

These pins are Power supply and GND for digital block and fixed input/output buffer only for 3.3V (32,70-74 pins).Power Supply voltage must be fixed at 3.3V

(5) **BFVdd, BFVss** (58) (68)

These pins are Power supply and GND for input/output buffer (3.3V/5V). In a case that **BFVdd** pin is applied at 5.0V, input/output voltage level of 34-67pins becomes 5.0V signal level. In another case that **BFVdd** pin is supplied at 3.3V, input/output pins (34-67 pins) becomes 3.3V signal level.

1-17. OUTL1+,OUTL1-,OUTL2+,OUTL2-,OUTR1+,OUTR1-,OUTR2+,OUTR2-

OUTL1+,OUTL1-,OUTL2+,OUTL2-,OUTR1+,OUTR1-,OUTR2+ and **OUTR2-** pins are pulse output converted $\Delta\Sigma$ output signal to PWM data.

These pins are connected to external Power Driver ICs.

2. Setting on `External Rate Converter 8fs` Mode

2-1. EXBCK,EXWCK,EXDATAL,EXDATAR,EXIOSEL

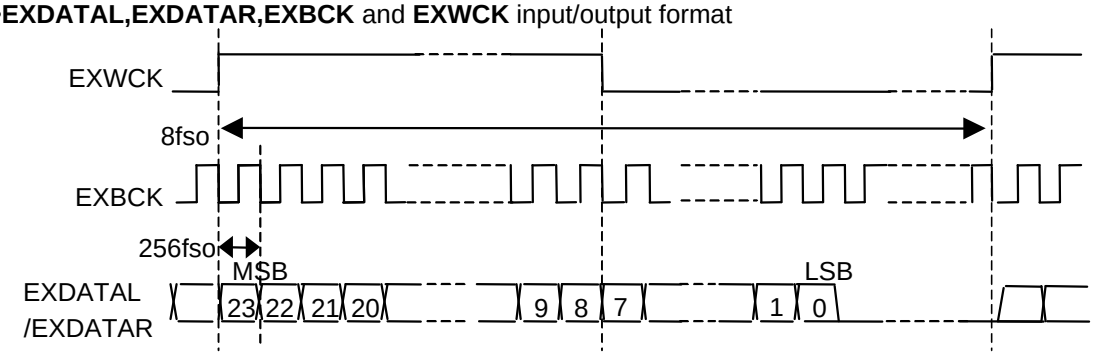
EXDATAL and **EXDATAR**are data input pins under condition of `*External Sampling Rate Converter 8fs*` mode. **EXDATAL** and **EXDATAR** are changed to output pins for Sampling Rate Converter except condition of `External Rate Converter 8fs` mode and **EXIOSEL** ="H".

In case of un-using `External sampling rate converter 8fs` mode, **EXIOSEL**="L" and **EXBCK, EXWCK, EXDATAL** and **EXDATAR** must be tied to low position.

EXDATAL, EXDATAR, EXBCK and **EXWCK** pin's input/output format is following figure.

Input Signal Mode	**EIOSEL**	**EXWCK,EXBCK,EXDATAL,EXDATAR** input/ output
`*External Rate Converter 8fs*` mode (MODE1,2=L,H)	L	input
	H	input
Except `*External Rate Converter 8fs*` mode (Except MODE1,2=L,H)	L	input
	H	output

•**EXDATAL,EXDATAR,EXBCK** and **EXWCK** input/output format



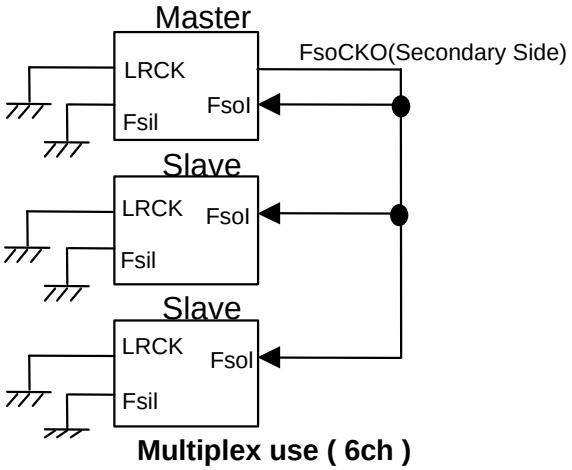
MSB first left justified (24bit)

2-2. SYNC,Fsol,Fsil,SFLAG

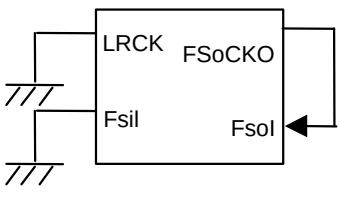
Multiplex and Single use

The primary clock side is not operated with synchronization, because internal Sampling Rate Converter is not used. Under `*External Rate Converter 8fs*` mode, the primary clock side asynchronous detection operates as `forced-disable`. The secondary clock side is operated with synchronization by **FsoCKO** pin.

Then, M65817AFP needs that rising edge of FsoCKO connected from M65817AFP to external sampling rate converter and rising edge of **EXWCK** connected from external rate converter to M65817AFP are in synchronized phase.



Multiplex use (6ch)



Single use (2ch)

3. Setting on `*SACD*` Mode

3-1. DSDL,DSDR,DSD128Fs,DSD64Fs,DSDCKSEL1,DSDCKSEL2,DSDCKIO

DSDL and **DSDR** are data input pins under `*SACD-fsi*` or `SACD-fso` mode.

Under `*SACD-fsi* ` mode, SACD data must be synchronized for primary clock.

Under `*SACD-fso* ` mode, SACD data must be synchronized for secondary clock.

DSDCKIO pin selects pin-type of **DSD128Fs** and **DSD64Fs** pins as input or output clock for data fetch.

The states of DSDCKSEL1 and DSDCKDEL2 pins select 4 "SACD" operating mode.

The relations of **DSDCKSEL1**, **DSDCKSEL2** pins and SACD input format mode setting are following figures.

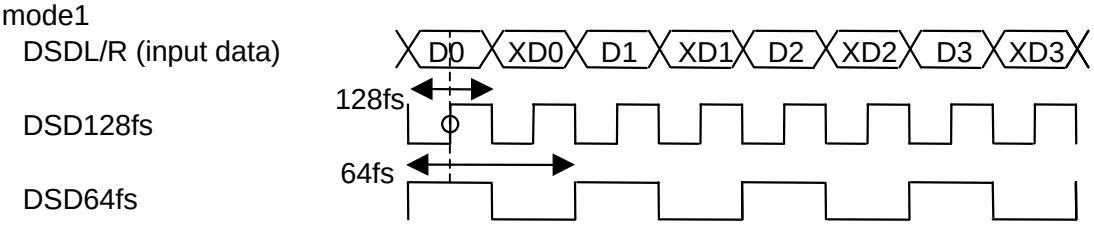
DSDCKSEL1	DSDCKSEL2	SACD operating timing mode
L	L	mode1
L	H	mode2
H	L	mode3
H	H	mode4

Setting of **DSDCKIO** is following table.

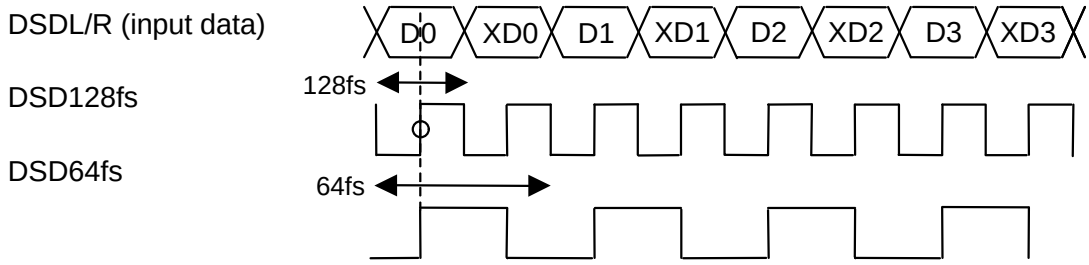
DSDCKIO	Selection of DSD64fs and DSD128fs I/O
L	Input
H	Output

SACD operating mode

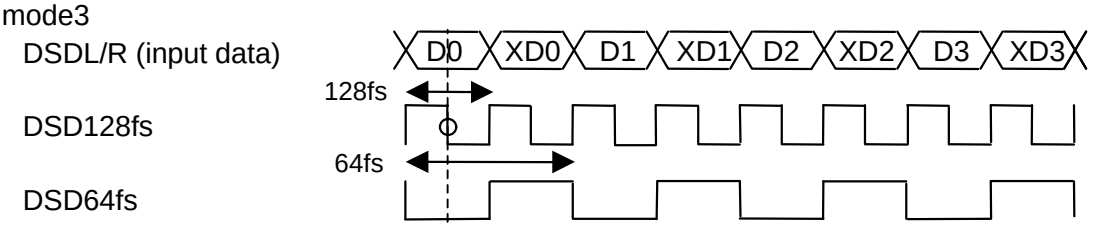
♦ mode1



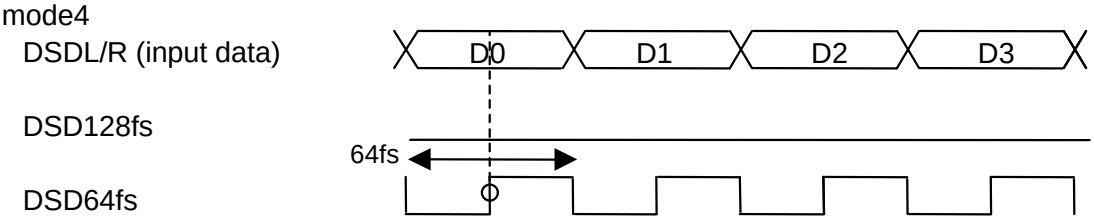
♦ mode2



♦ mode3



♦ mode4



* D0:Positive phase data, XD0:Negative phase data (reversal)

Positive phase data are fetched at the timing of "O" marks in upper figure.

3-2. SYNC,FsoI,FsiI,SFLAG

♦ *SACD-fsi* Mode

Multiplex Use

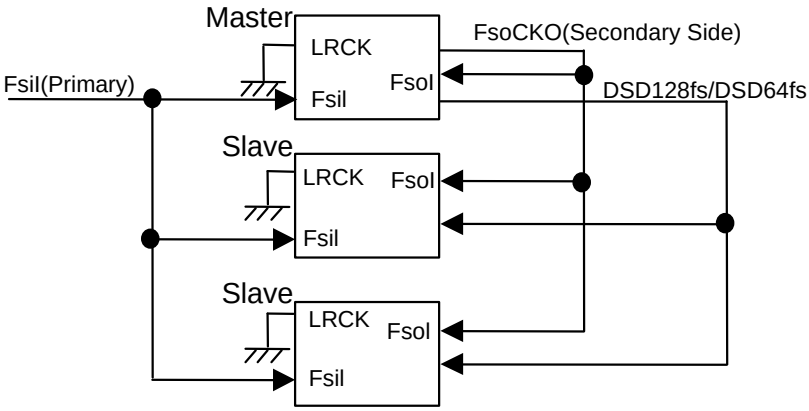
In the primary clock side,M65817AFP are operated with synchronization by FsiI pin's clock. In secondary clock side, M65817AFP must be generated from arbitrary one master-M65817AFP's FsoCKO pin and be entered each FsoI pins of slave-M65817AFP(inclusive master) with synchronization.

Additionally, the master-M65817AFPoutputs clock from **DSD64fs** and **DSD128fs** pins(DSDCKIO ="H"), and these clock are entered DSD64fs and DSD128fs pins (DSDCKIO="L") of slave-M65817AFP.

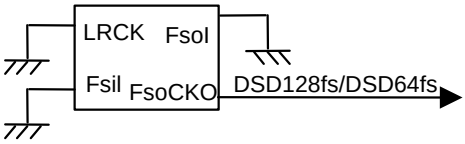
By these conditions, multiple M65817AFP are operated with synchronization each other for SACD input.

Single Use

The primary clock must be entered to FsiI pin, and the secondary clock must be entered to **FsoI** pin. In the other way, the primary and secondary clocks can not be entered at **FsiI** and **FsoI** pins, however in this case, the asynchronous-detection register flags (ASYNCEN1 and ASYNCEN2 in System Control) must be `disable`.



Multiplex use (6ch)



Single use (2ch)

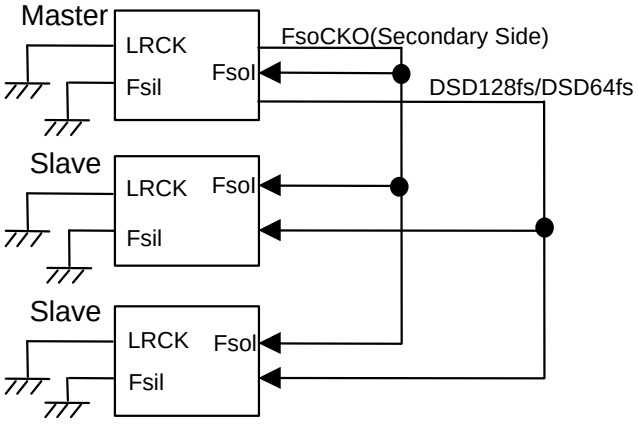
♦ *SACD-fso Mode*

Multiplex use (6ch)

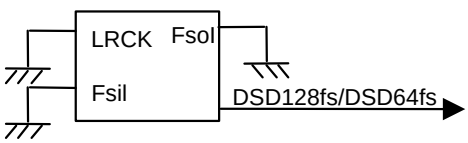
The primary clock side is not done with synchronization, because internal Sampling Rate Converter is not used. In `*SACD-fso*` mode, the primary side asynchronous detection operates as forced-`disable`. The secondary clock must be generated from arbitrary one master-M65817AFP's**FsoCKO** pin and be entered each **FsoI** pins of slave-M65817AFP(inclusive master) with synchronization. Additionally, the master-M65817AFP outputs clock wave from **DSD64fs** and **DSD128fs** pins (in this condition, **DSDCKIO** pin's input level of master-M65817AFP must be "H"), and these clock are entered **DSD64fs** and **DSD128fs** pins of slave-M65817AFP(in this condition, **DSDCKIO** pin's input level of slave-M65817AFP must be “L”). By these conditions, plural M65817AFP are operated with synchronization each other for SACD input.

Single Case (2ch)

The primary clock side is not operated with synchronization, because internal Sampling Rate Converter is not used. In `*SACD-fso*` mode, the primary side asynchronous detection operates as forced-`disable`. The secondary clock can be input at **FsoI** pin. As the another way, the secondary clock can not be entered at **FsoI** pin, however in this case, the asynchronous-detection flag register (ASYNCEN2 in System Control) must be `disable`.



Multiplex use (6ch)



Single use (2ch)

SERIAL CONTROL

1. Gain Control Mode

No setting bits means "Don't care".

bit	Flag Name	Functional Explanation	H	L	INIT
1	*MODE1*	Mode Setting 1		"L" fixed	-
2	*MODE2*	Mode Setting 2		"L" fixed	-
3	*TEST1*	Test Mode 1		"L" fixed	L
4	*TEST2*	Test Mode 2		"L" fixed	L
5	*NSLMT1*	Output Limit 1	Refer to Table 1-1.		L
6	*NSLMT2*	Output Limit 1			L
7	*GCONT1*	Channel selection for Gain Control Block 1	L/R independence	L/R common	L
8	*GCONT2*	Channel selection for Gain Control Block 2	Lch	Rch	L
9					-
10					-
11					-
12	*GAIN0*	Gain Data Index (MSB)			H
13	*GAIN1*	Gain Data Index			L
14	*GAIN2*	Gain Data Index			L
15	*GAIN3*	Gain Data Index			L
16	*GAIN4*	Gain Data Index (LSB)			L
17	*GAIN5*	Gain Data Mantissa (MSB)			H
18	*GAIN6*	Gain Data Mantissa			L
19	*GAIN7*	Gain Data Mantissa			L
20	*GAIN8*	Gain Data Mantissa			L
21	*GAIN9*	Gain Data Mantissa			L
22	*GAIN10*	Gain Data Mantissa			L
23	*GAIN11*	Gain Data Mantissa			L
24	*GAIN12*	Gain Data Mantissa (LSB)			L

•Output Limit (bit5,bit6:*NSLMT1* , *NSLMT2*)

The M65817AFP has Over Flow Limit function.

Over Flow Limit detects of input signal level and limits gain level.

Limit value is set by Gain Control Mode :bit5,bit6 " *NSLMT1,NSLMT2*" and System2 Mode:bit17"*NSOBIT*".

•The limit value setting of Gain control block and PWM output.

Table (1-1a). Limit Value [In Case of 6bit mode, system2 mode bit17(NSOBIT)="L"]

NSLMT1	*NSLMT2*	Gain Block	PWM Output(Limit Value from DS Block)
L	L	±0.9375	63 values (±31)
H	L	±0.90625	61 values (±30)
L	H	±0.875	59 values (±29)
H	H	±0.84375	57 values (±28)

Table (1-1b). Limit Value [In Case of 5bit mode system 2 mode bit17(NSOBIT)="H"]

NSLMT1	*NSLMT2*	Limit Value of Gain	PWM Output Value(Limit Value from ΔΣ Block)
L	L	±0.90625	31 values (±15)
H	L	±0.875	31 values (±15)
L	H	±0.84375	29 values (±14)
H	H	±0.8125	29 values (±14)

•Channel Selection for Gain Control Block (bit7,bit8:*GCONT1*, *GCONT2*)

These bits select L/R common or L/Rch independence operation.

GCONT1:"L"…L/Rch common(INIT),"H"…L/Rch independence.

GCONT2:"L"…Rch only, "H"…Lch only.

Bit8 is effective only the case of `bit7 = "H"`.

• The index and Mantissa part of Gain Data. (bit12 -bit24,:*GAIN0 -GAIN12*)

The Gain value is set from bit12 to bit24.

Index part: bit12 (MSB) -bit16(LSB)

Mantissa part: bit17 (MSB) -bit24 (LSB)

The Gain Data is assigned 13bits, composed of Index part 5bits and of Mantissa part 8bits,

The range of Index parts is following statements.

Index part: 10100b(16.0) - 10000b(1.0) - 00000b(2^{-16})

The range of mantissa part is following as statement.

Index part; 10100b -00001b: Mantissa part; 11111111b -10000000b (128 step/1 Index).

Index part;00000b: Mantissa part; 11111111b -00000000b (256 step).

Initial value :Index part: 10000b Mantissa part:10000000b

infinity zero:Index part: 00000b Mantissa part:00000000b

For instance 10000b (1.0) / 10000000b (0.5) means 0.5 (0dB).

Notice of GAIN value Setting continuously

In the case of GAIN value Setting continuously, for example of Setting L/Rch independently, please take the interval time (pulse interval time of SCLATCH signal) more than 1/fsc.For example, in the case of fso=48kHz, please take the interval time more than 21µsec.

• The Gain Data and Audio Output Level.

Table (6-1-2). The Gain Data and Output Level

The Gain Data	Polarity	Absolute Output	Output Level
10100/11111111		15.937	+30.069dB
|		|	|
10001/10000000		1.	+6.021dB
|		|	|
10000/10000000		0.	0dB
01111/11111111	+	0.49804687	–0.0340dB
|		|	|
00000/10000000		$0.5*2^{-16}$	–96.330dB
|		|	|
00000/00000001		$0.00390625*2^{-16}$	–138.474dB
00000/00000000		infinity zero	–∞ dB

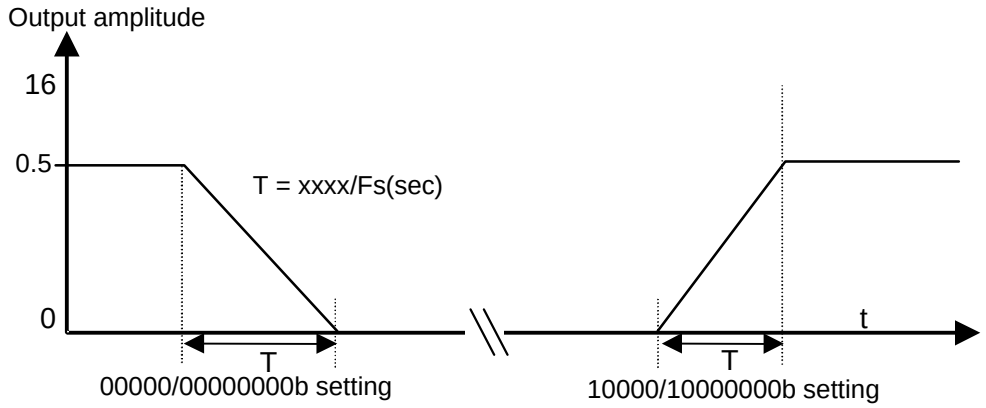
• Calculation method of Gain value.

The way to calculation of Gain value from Gain Data is following equation.

$$\text{Gain value} = 20\log\left[\, 2^{(\text{Index data(decimal value)}-16)} \times \frac{\text{Mantissa data(decimal value)}}{128} \,\right] \text{dB}$$

♦Soft Mute.

The Soft Mute function is executed by setting of Gain Data as 00000/00000000b
("/" :means dividing point between index part and mantissa part).
The release from Soft Mute function must be executed by setting the gain data before soft mute.
The Soft Mute function and release from Soft Mute function don't have linear curve but
have characteristics of approximate exponential curve.



Characteristics of Soft Mute function

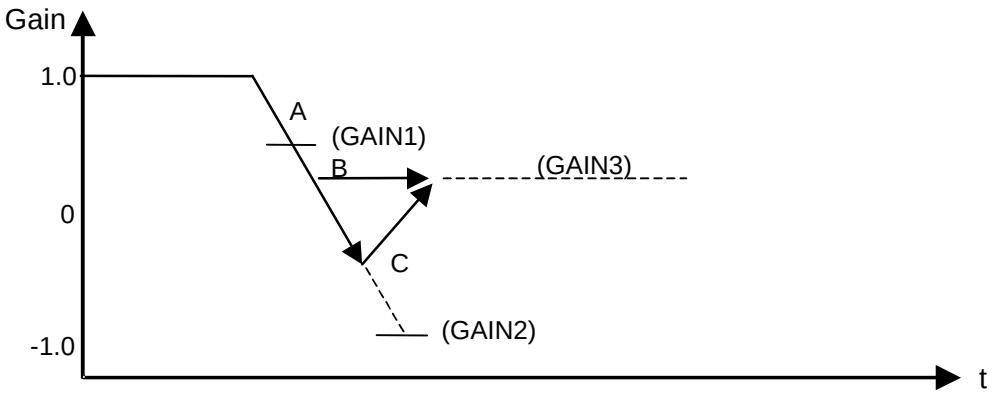
♦Operating time of Soft Mute

Total steps from MAX value(10100b/11111111b) to MIN value(00000b/00000000b) are
(128steps/1index) × (20 indexes(10100b-10000b)) + 256steps =2816steps.
The transition term of up and down depend on 2fso clock.
Therefore, in case of fso=48kHz, T=1/2fso=10.416µsec/step, transition term are following.

From MAX value (10100b/11111111b) to MIN value (00000b/00000000b) : 2816T=29.333msec.
From 0dB value(10100b/11111111b) to MIN value(00000b/00000000b) : 2304T=24.000msec.
6dB transition term (when over 00000b/10000000b(=-96dB) values): 128T=1.333msec.

♦Soft Attenuate.

Transition from older Gain Attenuation to newer Gain Attenuation always operates with Soft Mute function.
For example, in case of Gain1 > GAIN3 > GAIN2, transition process is shown below.
First, GAIN1 is operated, then second, GAIN2 is operated.
In case that GAIN2 is operated faster than GAIN1of transition completion("A" situation in figure),
GAIN1 is ignored and data approaches at GAIN2 .
Further, GAIN3 is operated faster than GAIN2 of transition completion("B" or "C" situation in figure),
GAIN2 is ignored and data approaches at GAIN3 .



Soft Attenuate

2. System1 Mode (Primary side).

bit	Flag Name	Functional Explanation	H	L	INIT
1	*MODE1*	Mode Setting 1		"L" fixed	-
2	*MODE2*	Mode Setting 2	"H" fixed		-
3	*IFMT0*	Input Format Selection	Refer to Table 2-1.		L
4	*IFMT1*				L
5	*IBIT0*	Setting for Input Word Length	Refer to Table 2-2.		L
6	*IBIT1*				L
7	*ISF0*	Input Sampling Rate Selection	Refer to Table 2-3.		L
8	*ISF1*				L
9	*EMPFS1*	Fs selection for De-emphasis Filter	Refer to Table 2-4.		L
10	*EMPFS2*				L
11	*DF1IMUTE*	Zero Mute of DATA input	Active	Non-active	L
12	*DF2IMUTE*	Zero Mute at rate converter input	Active	Non-active	L
13			don't care		-
14			don't care		-
15			don't care		-
16	*ASYNCEN1*	Asynchronous Detection Flag for Primary Side	enable	disable	L
17					
18					
19					
20					
21					
22					
23					
24					

Table 2-1. Input Format

bit	Flag Name	MSB First Left Justified	MSB First Right Justified	LSB First Right Justified	I^2S
3	*IFMT0*	L	H	L	H
4	*IFMT1*	L	L	H	H

Table 2-2. Setting for Input Data Word Length

bit	Flag Name	16bit	20bit	24bit	Don't use
5	*IBIT0*	L	L	H	H
6	*IBIT1*	L	H	L	H

Table 2-3. Input Sampling Rate Selection (Fs:32k-48kHz, 2Fs:64k-96kHz, and 4Fs:128k-192kHz)

bit	Flag Name	Fs	2Fs	4Fs	Don`t use
7	*ISF0*	L	H	L	H
8	*ISF1*	L	L	H	H

Table 2-4. Fs Selection for De-emphasis filter (De-emphasis is "ON" except for bit9=L and bit10=L)

bit	Flag Name	32.0K	44.1K	48.0K	OFF
9	*EMPFS1*	H	L	H	L
10	*EMPFS2*	H	H	L	L

♦Input Format Selection (bit3,bit4:*IFMT0,IFMT1*).

Input Format Selection function is effective only condition of `*Normal*` mode.

Otherwise, Input Format Selection function is ineffective under conditions of `*External Rate Converter 8fs* ` and `*SACD*` modes(Interlocked with **MODE1** and **MODE2** pins).

Detail setting of `*External Rate Converter 8fs*` and `*SACD*` modes are shown in Page14 and Page15 .

♦Setting of Input Word Length (bit5,bit6:*IBIT0,IBIT1*).

Refer to Table 2-2.

Setting of Input Data Word Length is effective only MSB First Right Justified.

♦Input Sampling Rate Selection (bit7,bit8:*ISF0,ISF1*).

Refer to Table 2-3.

♦Fs Selection for De-emphasis Filter on/off (bit9, bit10 : *EMPFS1, EMPFS2*).

Refer to Table 2-4.

(bit9,bit10): (L,L)… De-emphasis Filter is "off".

except (L,L)…De-emphasis Filter on (Fs setting).

♦Zero Mute at data input (bit11: *DF1IMUTE*).

DF1IMUTE : "L"…Mute release.

"H"…Mute.

The input data from DATA pin in normal mode is muted in this setting.

♦Zero Mute at Sampling Rate Converter Input (bit12: *DF2IMUTE*).

DF2IMUTE : "L"…Mute release.

"H"…Mute.

DF2IMUTE is effective for rate converter input data.

DF2IMUTE executes zero mute of input data from **DATA** pin under condition of `*Normal*` mode and from **DSDL** /**DSDR** pins under condition of `*SACD-fsi*` mode.

♦"Enable" of Primary Side Asynchronous Detection Flag (bit16: *ASYNCEN1*).

Bit16 controls "enable"/"disable" of primary-side-asynchronous-detection-circuit.

ASYNCEN1 : "L"…disable.

"H"…enable.

Under condition of ASYNCEN1="L", primary side asynchronous detection is ineffective whether the clock is not inputted to FsiI pin, thereby M65817AFP does not operate function under asynchronization, for instance mute operation. However, Primary Side Asynchronous Detection is effective only condition of `*SACD-Fsi* ` mode.

3. System2 Mode (Secondary side).

bit	Flag name	Functional Explanation	H	L	INIT
1	*MODE1*	Mode setting1	"H" fixed		-
2	*MODE2*	Mode setting2		"L" fixed	-
3	*IMCKSEL*	Input Master Clock Selection	512Fs	256Fs	L
4	*DSDFCO0*	Filter Coefficient of Down Sampling	Refer to Table 6-3-1.		L
5	*DSDFCO1*				L
6	*SYNC*	Resynchronization	L->H : Resynchronization.		L
7	*XFsoOEN*	**XfsoOUT** pin output "enable"	disable	enable	L
8	*ASYNCEN2*	Asyncronous Detection Flag for secondary Side	enable	disable	L
9	*CHSEL*	L / R inversion of PWM output	active	non-active	L
10	*DRPOL*	ΔΣ Block: Rch Input Phase	Negative-phase	Positive-phase	L
11	*SRCRST*	Sampling Rate Converter Reset	Active	Non-active	L
12			don't care		-
13	*GIMUTE*	Zero Mute at Gain Control Input Clock	Active	Non-active	L
14	*NSPMUTE*	Duty 50 percent Mute of PWM Output	Active	Non-active	L
15	*PGMUTE*	G_MUTE of PWM Output Data	Active	Non-active	L
16	*NSSPEED*	ΔΣ Block: Operation Speed		"L" fixed	L
17	*NSOBIT*	ΔΣ Block: Setting of Output Bit Number	5 bits (31 value)	6 bits (63 value)	L
18	*DCDRPOL*	ΔΣ Block: Rch Phase of DC dithering	Negative-phase	Positive-phase	L
19	*DCDSEL0*	ΔΣ Block: DC dithering Selection	Refer to 6-3-2		L
20	*DSDSEL1*				L
21	*ACDRPOL*	ΔΣ Block: Rch Phase of AC dithering	Negative-phase	Positive-phase	L
22	*ACDSEL0*	ΔΣ Block: AC dithering selection	Refer to 6-3-3		L
23	*ACDSEL1*				L
24	*ACDSEL2*				L

Table 3-1 Setting of Down Sampling Filter Coefficient

bit	Flag Name	ROM1	ROM2	ROM3	ROM4
4	*DSDFCO0*	L	H	L	H
5	*DSDFCO1*	L	L	H	H

Table 3-2 DC dithering Selection at DS Block

bit	Flag Name	Non-dithering	DC dithering	DC dithering	DC
19	*DCDSEL0*	L	H	L	H
20	*DCDSEL1*	L	L	H	H

Table 3-3 AC dithering Selection at DS Block

bit	Flag Name	Non-dithering	AC dithering A	AC dithering C	AC dithering E
22	*ACDSEL0*	don't care	L	L	L
23	*ACDSEL1*	L	H	L	H
24	*ACDSEL2*	L	L	H	H

•Input Master Clock Selection (bit3:*IMCKSEL*).

"L":256Fs

"H":512Fs

•Selection of of Down Sampling Filter Coefficient for SACD input (bi4,bit5: DSDFCO0,DSDFCO1) .

Refer to Table 6-3-1.

•Resynchronization (bit6: *SYNC*).

Resynchronization function is same at **SYNC** pin's function. Refer to Operation Explanation, Chapter 5-1.10 .

Resynchronization process starts by SYNC rise edge,

therefore SYNC level must be fixed to "L"just before SYNC operation .

•"Enable" of **XfsoOUT** pin Output(bit7: *XfsoOEN*).

"L": Clock Output (enable), "H": L fixed (disable)

•Flag to "Enable" Asynchronous Detection for Secondary Block (bit8: *ASYNCEN2*).
ASYNCEN2 : "L"…disable.
"H"…enable.
Under condition of ASYNCEN2="L", secondary side asynchronous detection is ineffective whether FsiI Clock is not inputted, there by M65817AFP does not operate function under asynchronous position, for instance mute operation.

•PWM Output Pins L/R Reverse.(bit9: *CHSEL*).
"L": L/R no reverse, "H": L/R reverse.

•ΔΣ: Rch Input Phase (bit10: *DRPOL*).
"L": Positive Phase(Through).
"H": This setting makes ΔΣ Rch input in reverse, further makes PWM block input phase reverse, ultimately phase becomes Positive Phase(Input pin and output pin's phase is same).

•Rate Converter Block Reset (Initialize function) (bit11: *SRCRST*).
SRCRST: "L"…normal operation .
"H”>>"L" edge…Reset(initialize function).

•Zero Mute of Gain Control Input (bit13: *GIMUTE*).
GIMUTE: "L"…Mute release, "H"…Mute.

•Duty 50% Mute of PWM Output (bit14: *NSPMUTE*).
NSPMUTE: "L"…Mute release.
"H"…PWM output duty 50 % mute.
This function is able to do NSPMUTE pin (39 pin), too. (This Mute function can be set either NSPMUTE register or NSPMUTE pin.)

•PWM Output Data G_MUTE. (bit15: *PGMUTE*).
Under condition of G_MUTE flag ="H", each PWM outputs are fixed below.
OUTL1+ and **OUTR1+** = "L", **OUTL2+** and **OUTR2+** = "L”
OUTL1- and **OUTR1-** = "H", **OUTL2-** and **OUTR2-** = "H"
"L"…Mute release, "H"…Mute.
PGMUTE function exists at **PGMUTE** pin (39 pin), too(PGMUTE function and **PGMUTE** pin are same function. This Mute function can be set either NSPMUTE function or **NSPMUTE** pin.)

•ΔΣ Block : Operation RATE (bit16: *NSSPEED*).
NSSPEED: "L” fixed
NSSPEED function becomes 16Fs fixed.

• ΔΣ Block : Output Bit Number Setting (bit17: *NSOBIT*).
Bit17 selects bit numbers of ΔΣ Block .
NSOBIT: "L"…6bits(63 values).
"H"…5bits(31values).
(At MCKSEL="H", bit numbers of ΔΣ Block become 5bits(31values) fixed.

•ΔΣ Block: DC dithering Rch Phase (bit18: *DCDRPOL*).
DCDRPOL: "L"…In phase (toward the left channel).
"H"…Out of phase.

•ΔΣ Block: DC dithering Selection (bit19,bit20: *DCDSEL0,DCDSEL1*).
Refer to Table 3-2.

•ΔΣ Block: AC dithering Rch Phase (bit21: *ACDRPOL*).
ACDRPOL: "L"…In phase (toward the left channel).
"H"…Out of phase.

•ΔΣ Block: AC dithering Selection (bit22,bit23,bit24: *ACDSEL0,ACDSEL1,ACDSEL2*).
Refer to Table 3-3.

TIMING CHARACTERISTIC

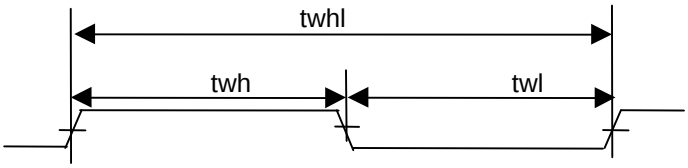
1. AC Characteristics Lists.

(Ta=25ºC, PWM Vdd=5V, DVdd=3.3V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
XfsoIN duty ratio	duty(XfsoIN)		40	50	60	%
XfsiIN duty ratio	duty(XfsiIN)	512fs	30	50	70	%
		256fs	40	50	60	%
SCSHIFT pulse time	tw(SCSHIFT)		160			nsec
SCDT setup time	tsu(SCDT)		80			nsec
SCDT hold time	th(SCDT)		80			nsec
SCLATCH pulse width	tw(SCLATCH)		160			nsec
SCLATCH setup time	tsu(SCLATCH)		160			nsec
SCLATCH hold time	th(SCLATCH)		160			nsec
BCK pulse width	tw(BCK)		35			nsec
DATA setup time	tsu(DATA)		20			nsec
DATA hold time	th(DATA)		20			nsec
LRCK setup time	tsu(LRCK)		20			nsec
LRCK hold time	th(LRCK)		20			nsec
EXBCK pulse time	tw(EXBCK)		35			nsec
EXWCK setup time	tsu(EXWCK)		20			nsec
EXWCK hold time	th(EXWCK)		20			nsec
EXDATA L / R setup time	tsu(EXDATA)		20			nsec
EXDATA L / R hold time	th(EXDATA)		20			nsec
EXDATA L / R output delay time	tpd(EXDATA)	Output load capacity 10 [pF]		1.0		nsec
EXWCK output delay time	tpd(EXWCK)	Output load capacity 10 [pF]		1.0		nsec
DSD128fs pulse width	tw(DSDCK)		70			nsec
DSD64fs pulse width	tw(DSDCK)		140			nsec
DSD L / R setup time	tsu(DATA)	mode 1, 2, 3 and 4	40			nsec
DSD L / R hold time	th(DATA)	mode 1, 2, 3 and 4	40			nsec
SYNC pulse width	tw(SYNC)		160			nsec

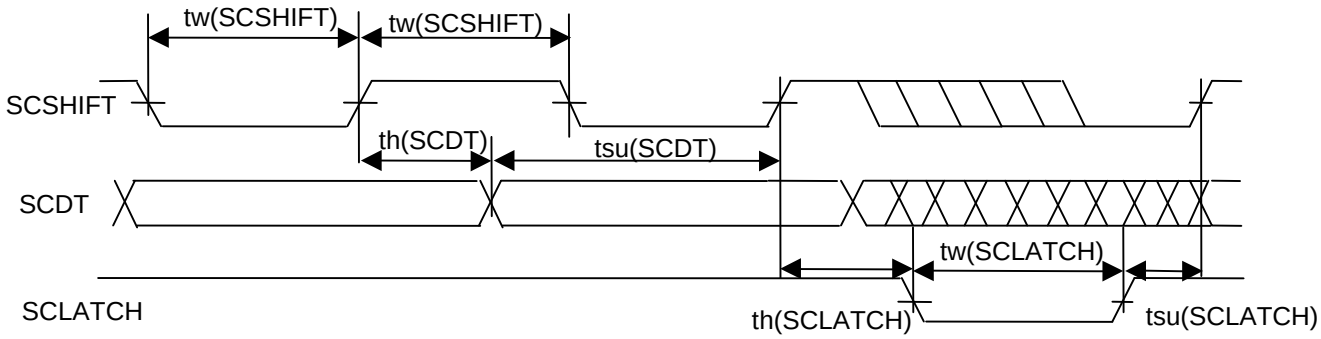
2. AC Characteristics Timing Chart.

(1) XfsoIN, XfsiIN Duty Ratio

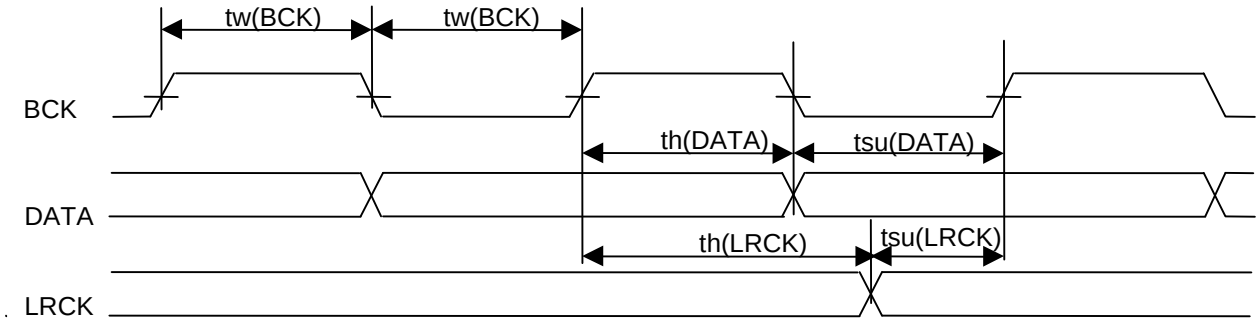


$$\text{duty (XfsoIN,XfiIN)} = \frac{twh}{twhl}$$

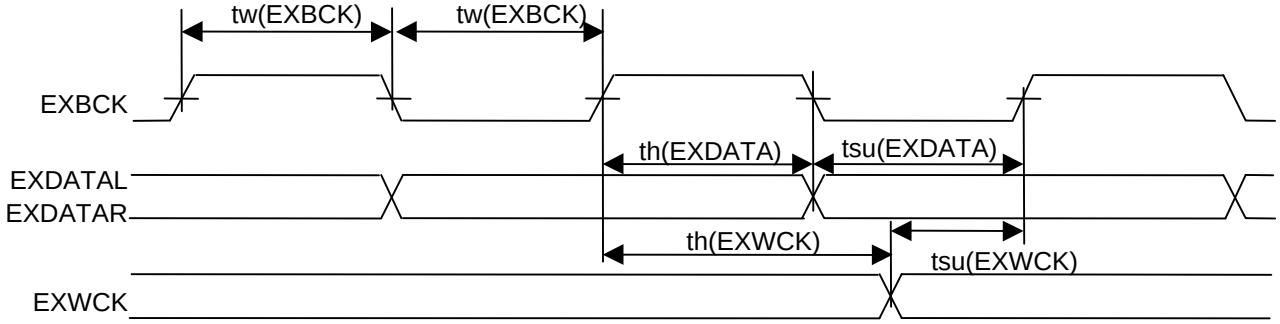
(2) SCSHIFT, SCDT, SCLATCH input timing



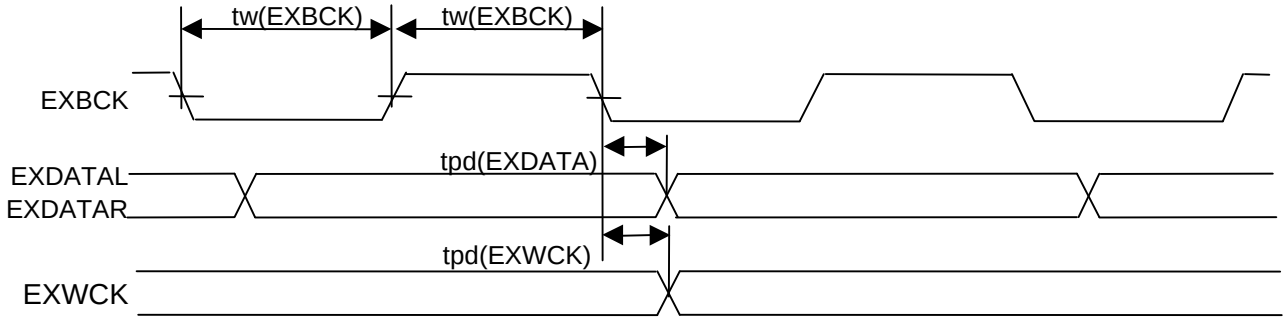
(3) BCK, DATA, and LRCK Input timing



(4) EXBCK, EXDATAL, EXDATAR, EXWCK input timing

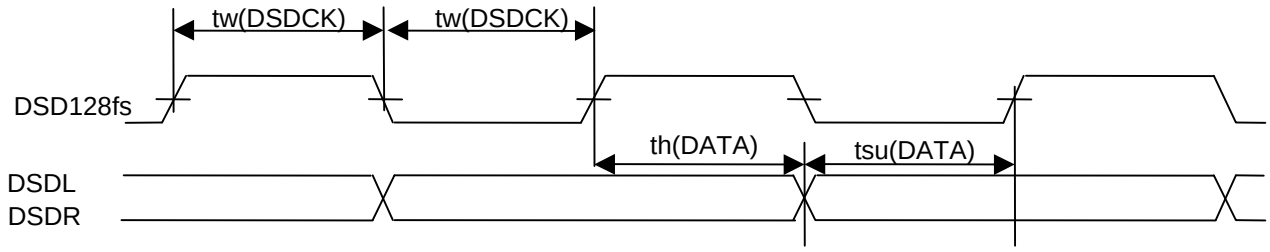


(5) EXBCK, EXDATAL, EXDATAR, EXWCK output timing

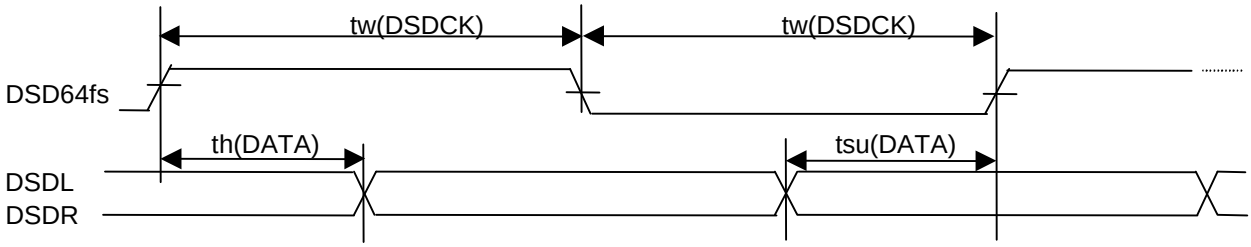


(6) DSD64fs, DSD128fs, DSDL, DSDR input timing

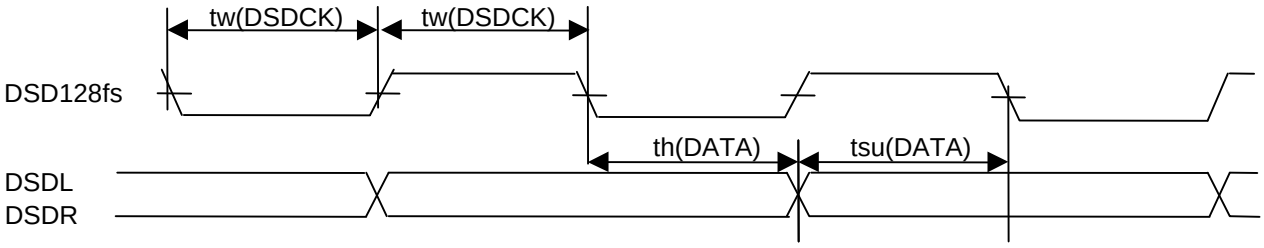
♦mode1



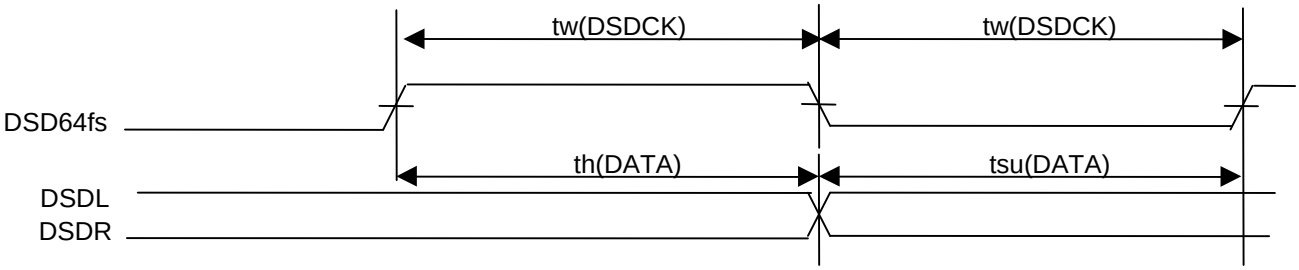
♦mode2



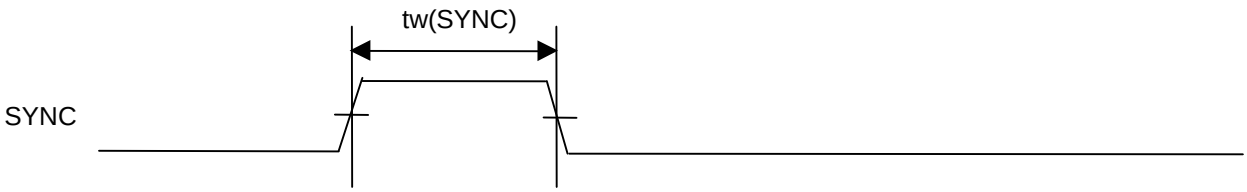
♦mode3



♦mode4



(7) SYNC input timing

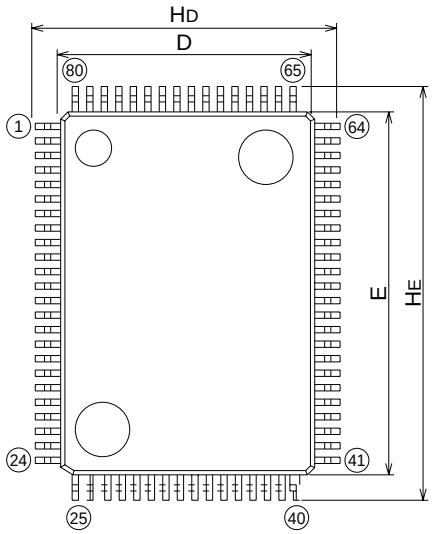


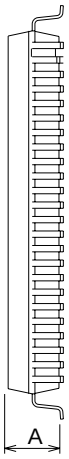
DETAILED DIAGRAM OF PACKAGE OUTLINE

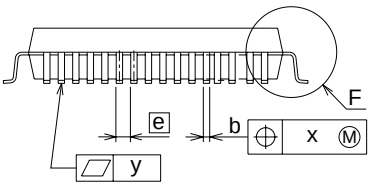
80P6N-A (MMP)

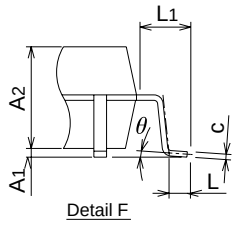
Plastic 80pin 14×20mm body QFP

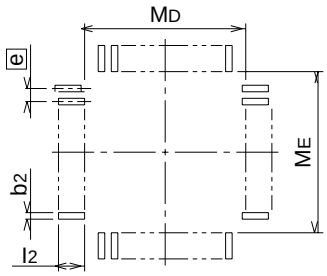
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	–	1.58	Alloy 42











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A_1	0	0.1	0.2
A_2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.8	–
H_D	16.5	16.8	17.1
H_E	22.5	22.8	23.1
L	0.4	0.6	0.8
L_1	–	1.4	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b_2	–	0.5	–
I_2	1.3	–	–
M_D	–	14.6	–
M_E	–	20.6	–

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