OPAX607 50-MHz, Low-Power, Gain of 6-V/V Stable, Rail-to-Rail Output CMOS Operational Amplifier

1 Features

- Low I_Q: 900 µA (typical)
- Input Offset Drift: 1.5 µV/°C (maximum)
- Offset voltage: 100 µV (typical)
- Gain bandwidth product: 50 MHz
- Broadband noise: 3.8 nV/√Hz
- Input bias current: 20 pA (maximum)
- Rail-to-rail output (RRO)
- Decompensated, gain ≥ 6 V/V (stable)
- Shutdown current: 1 µA (maximum)
- Supply range: 2.2 V to 5.5 V

2 Applications

- Current-sensing
- Fish finders and sonar
- Ultrasonic flow meters
- Printers
- Light curtains and safety guards
- Optical modules
- Handheld test equipment
- PM2.5 and PM10 particle sensors

3 Description

The OPAX607 is a decompensated (gain = 6 V/V stable), general-purpose complementary metal oxide semiconductor (CMOS) operational amplifier (op amp) that provides low noise of 3.8 nV/√Hz and a wide gain bandwidth of 50 MHz. The low noise and wide bandwidth of the OPAX607 make the device attractive for general-purpose applications that require a good balance between cost and performance. The high-impedance CMOS inputs make the OPAX607 an ideal amplifier to interface with sensors with large output impedance (for example, piezoelectric transducers).

The OPA607 features a power-down mode with a maximum quiescent current of less than 1 µA, making the device suitable for use in portable battery-powered applications. The rail-to-rail output (RRO) of the OPA607 can swing up to 10 mV from the supply rails, enabling maximum dynamic range.

This op amp is optimized for low-voltage operation as low as 2.2 V (±1.1 V) and up to 5.5 V (±2.75 V), and is specified over the temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA607	SC70 (6)	2.00 mm × 1.25 mm
	SOT23 (5)	2.90 mm × 1.60 mm
OPA2607	SOIC (8) (2)	4.90 mm × 3.91 mm
	VSSOP (8) (2)	3.00 mm × 3.00 mm
	X2QFN (10) (2)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Preview package.

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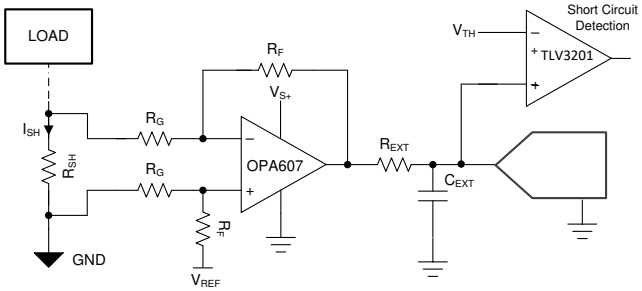
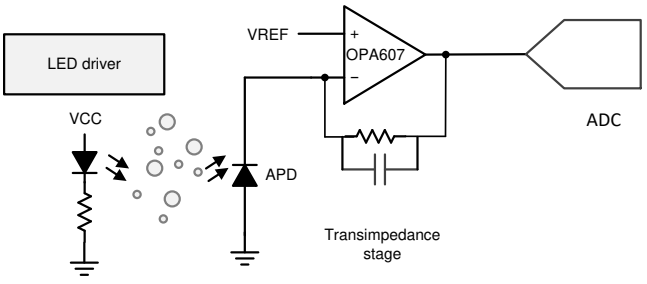
OPA607 as a Difference Amplifier for a Current-Sensing Application



OPA607 as a Low-Speed TIA



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2019) to Revision A **Page**

- Added OPA2607 D, DGK (Preview) and OPA2607 RUG Package (Preview) pinout drawings to the *Pin Configuration and Functions* section ... 4
- Updated the OPA607 amplifiers specifications in the *Rail-to-Rail Output and Driving Capacitive Loads* section ... 9

Changes from Revision A (February 2020) to Revision B **Page**

- Updated *OPA607 as a Low-Speed TIA* key graphic ... 1

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5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS				
		SOIC D(1)	X2QFN(1) RUG	VSSOP(1) DGK	SC-70 DCK	SOT-23 DBV
OPA607	1	—	—	—	—	5
OPA607 (Shutdown)		—	—	—	6	—
OPA2607	2	8	—	8	—	—
OPA2607 (Shutdown)		—	10	—	—	—

(1) Package is preview only.

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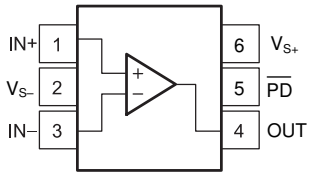
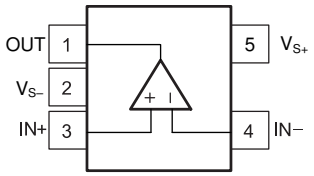
6 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



DBV Package
5-Pin SOT-23
Top View

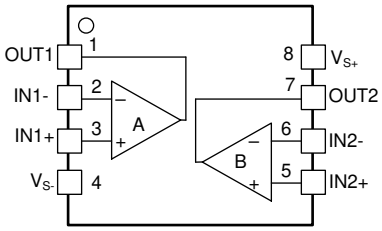


Pin Functions - Single Channel

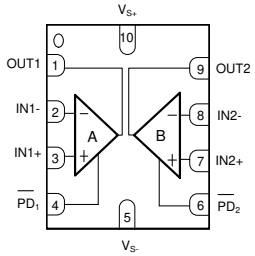
PIN			I/O(1)	DESCRIPTION
NAME	DBV	DCK		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
$\overline{PD}$	—	5	I	Low = amplifier disabled, high = amplifier enabled; see the *Power-Down Mode* section for more information.
$V_{S–}$	2	2	P	Negative supply or ground (for single-supply operation)
V_{S+}	5	5	P	Positive supply

(1) I = input, O = output, and P = power.

OPA2607 D, DGK (Preview)
8-Pin SOIC, VSSOP,
Top View



OPA2607 RUG Package (Preview)
10-Pin X2QFN
Top View



Pin Functions - Dual Channel

PIN			I/O	DESCRIPTION
NAME	D, DGK	RUG		
IN1–	2	2	I	Inverting input, channel 1
IN1+	3	3	I	Noninverting input, channel 1
IN2–	6	8	I	Inverting input, channel 2
IN2+	5	7	I	Noninverting input, channel 2
OUT1	1	1	O	Output, channel 1
OUT2	7	9	O	Output, channel 2
$V_{S–}$	4	5	—	Negative (lowest) supply or ground (for single-supply operation)
V_{S+}	8	10	—	Positive (highest) supply
$\overline{PD1}$	—	4	I	Low = amplifier 1 disabled, high = amplifier 1 enabled; see the *Power-Down Mode* section for more information.
$\overline{PD2}$	—	6	I	Low = amplifier 2 disabled, high = amplifier 2 enabled; see the *Power-Down Mode* section for more information.

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$(V_{S+}) – (V_{S–})$	Supply voltage, V_S		6	V
V_{IN+}, $V_{IN–}$	Input voltage(1)	$(V_{S–}) – 0.5$	$(V_{S+}) + 0.5$	V
V_{ID}	Differential input voltage(1)		±5	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±20	mA
	Continuous power dissipation		See *Thermal Information*	
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage $(V_{S+}) – (V_{S–})$	2.2		5.5	V
		±1.1		±2.75	
T_A	Ambient operating temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA607 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	219.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	182.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	105.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	87	°C/W
ψ_{JB}	Junction-to-board characterization parameter	105.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V[1], R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V and PD connected to (V_{S+}) (unless otherwise noted)[2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–0.5	0.1	0.5	mV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–0.6	0.1	0.6	mV
dV_{OS}/dT	Input offset voltage drift[3]	T_A = –40°C to +125°C		±0.3	±1.5	µV/°C
PSRR	Power-supply rejection ratio		98	120		dB
PSRR	Power supply rejection ratio	V_S = 2.2 V to 5.5 V, V_{CM} = (V_S/2) - 0.5 V, T_A = -40 to 125℃	98	130		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		($V_{S–}$)		(V_{S+}) – 1.1	V
CMRR	Common-mode rejection ratio	($V_{S–}$) < V_{CM} < (V_{S+}) – 1.1 V	94	100		dB
INPUT BIAS CURRENT						
I_B	Input bias current[3]			2	20	pA
I_{OS}	Input offset current[3]			2	20	
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		1.6		μV_{PP}
e_N	Input voltage noise density	f = 10 kHz, 1/f corner at 1 kHz		3.8		$nV/\sqrt{Hz}$
i_N	Input current noise density	f = 1 kHz		47		$fA/\sqrt{Hz}$
INPUT IMPEDANCE						
C_{IN}	Differential			11.5		pF
	Common-mode			5.5		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 400 mV < V_O < (V+) – 400 mV	120	140		dB
	Phase margin			65		Degrees
AC Characteristics (V_S = 5 V)						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mVpp		9		MHz
GBW	Gain-bandwidth product	G = 20		50		
SR	Slew rate	3-V output step (10-90%), V_{OCM} = mid-supply		24		V/µs
t_S	Settling time	To 0.1%, 3-V step, G = 40, V_{OCM} = mid-supply		0.75		µs
		To 0.01%, 3-V step, G = 40, V_{OCM} = mid-supply		1.75		
	Overdrive recovery time	V_{IN+} × Gain > V_S		0.2		µs
THD + N	Total Harmonic Distortion Plus Noise[4]	V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 10 kΩ		-103		dB
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 10 kΩ		-91.5		
		V_{OUT} = 2 V_{PP}, f = 1 kHz , R_L = 1 kΩ		-96		
		V_{OUT} = 2 V_{PP}, f = 20 kHz , R_L = 1 kΩ		-72.8		
HD2	Second-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-105		dBc
HD3	Third-order harmonic distortion	V_{OUT} = 2 V_{PP} f = 20 kHz		-95		
OUTPUT						
	Output Voltage swing from supply rails			8	10	mV
I_{SC}	Short-circuit current			55		mA
Z_O	Open-loop output impedance	f = 1 MHz		500		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		900	1000	µA
POWER DOWN (Device Enabled When Floating)						

(1) All Gains (G) mentioned are in V/V unless otherwise noted.
(2) Parameters with minimum or maximum specification limits are 100% production tested at 25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(3) Specified by design and characterization; not production tested.
(4) Lowpass-filter bandwidth is 92kHz for f = 20 kHz and 20 kHz for f = 1 kHz.

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Electrical Characteristics (continued)

at T_A = 25°C, V_S = 2.2 V to 5.5 V, G = 6 V/V(1), R_F = 5 kΩ, C_F = 2.5 pF, V_{CM} = (V_S / 2) – 0.5 V, C_L = 10 pF, R_L = 10 kΩ connected to (V_S / 2) – 0.5 V and PD connected to (V_{S+}) (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{QPD}	Power-down quiescent current	$\overline{PD}$ = V_{S-}		750	1000	nA
I_{PDB}	Power-down pin bias current(5)	$\overline{PD}$ = V_{S-}		800	900	
	Enable voltage threshold	Logic-high threshold			0.7 x V_S	V
	Disable voltage threshold	Logic-low threshold	0.2 x V_S			
t_{ON}	Turn-on time delay			15		µs
t_{OFF}	Turn-off time delay			0.5		

(5) In Power-Down Mode , I_{QPD} = I_{PDB} + Leakage current drawn by the op amp circuit. Total current in Power-Down mode = I_{QPD} only and not the sum of I_{QPD} and I_{PDB}.

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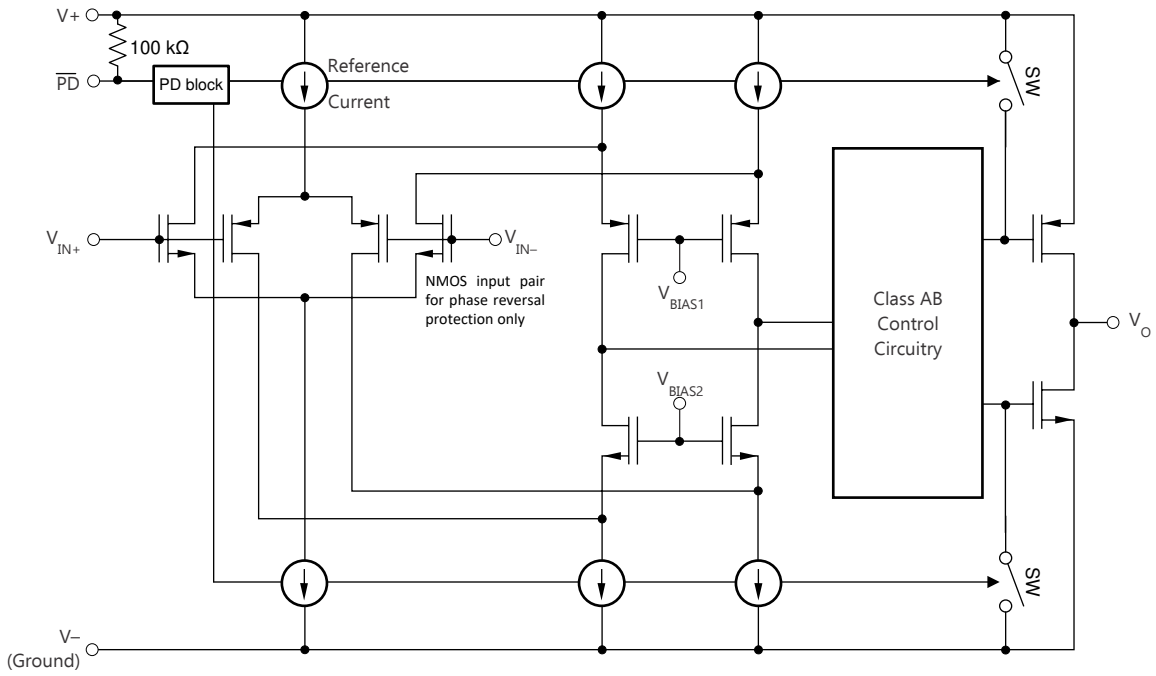
8 Detailed Description

8.1 Overview

The OPAX607 is a low-noise, rail-to-rail output (RRO) operational amplifier (op amp). The device operates from a supply voltage of 2.2 V to 5.5 V. The input common-mode voltage range also extends down to the negative rail allowing the OPAX607 op amp to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply, voltage-range applications, which results in complete usage of the full-scale range of the consecutive analog-to-digital converters (ADCs). The decompensated architecture allows for a favorable tradeoff of low-quiescent current for a very-high gain-bandwidth product (GBW) and low-distortion performance in high-gain applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAX607 operational amplifier is fully specified and assured for operation from 2.2 V to 5.5 V, applicable from –40°C to +125°C. The OPAX607 is completely operational with asymmetric voltages applied across the supply pins. The total voltage (that is, $(V_{S+}) – (V_{S–})$) must be less than the supply voltage mentioned in the *Absolute Maximum Ratings* table.

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Feature Description (continued)

8.3.2 Rail-to-Rail Output and Driving Capacitive Loads

Designed as a low-power, low-voltage operational amplifier, the OPAX607 delivers a robust output drive capability. For resistive loads of 10 kΩ, the output swings to within a few millivolts of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails. The OPAX607 drives up to a nominal capacitive load of 47 pF on the output with no special consideration and without the need of a series isolation resistor R_O while still being able to achieve 45º of phase margin. When driving capacitive loads greater than 47 pF, TI recommends using R_O as shown in Figure 1 in series with the output as close to the device as possible. Without R_O, the external capacitance (C_L) interacts with the output impedance (Z_O) of the amplifier, resulting in stability issues. Inserting R_O isolates C_L from Z_O and restores the phase margin. Figure 1 shows the test circuit.

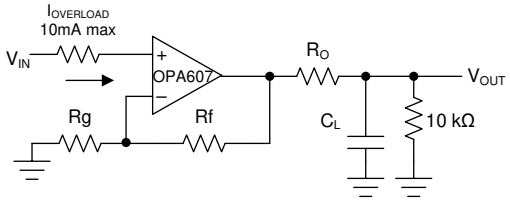

Figure 1. Input Current Protection and Driving Capacitive Loads

8.3.3 Input and ESD Protection

When the primary design goal is a linear amplifier with high CMRR, do not exceed the op amp input common-mode voltage range (V_{CM}). This CMRR is used to set the common-mode input range specifications in the *Electrical Characteristics* table. The typical specifications for the OPAX607 are from the negative rail to 1.1 V below the positive rail. Assuming the op amp is in linear operation, the voltage difference between the input pins is small (ideally 0 V) and the input common-mode voltage can be analyzed at either input pin; the other input pin is assumed to be at the same potential. The voltage at V_{IN+} is easy to evaluate. In a noninverting configuration (Figure 1) the input signal, V_{IN+}, must not exceed the V_{CM} rating. However, in an inverting amplifier configuration, V_{IN+} must be connected to the voltage within V_{CM}. The input signal applied at V_{IN-} can be any voltage, such that the output voltage swings with a headroom of 10mV from either of the supply rails.

The input voltage limits have fixed headroom to the power rails and track the power-supply voltages. For single 5-V supply, the linear input voltage range is 0 V to 3.9 V and with a 2.2-V supply this range is 0 V to 1.1 V. The headroom to each power-supply rail is the same in either case: 0 V and 1.1 V.

The OPAX607 also incorporates internal electrostatic discharge (ESD) protection circuits on all pins. For the input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide input overdrive protection, as long as the current is limited with a series resistor to 10 mA, as stated in the *Absolute Maximum Ratings* table. Figure 1 shows a series input resistor can be added to the driven input to limit the input current. The series input resistor also serves to cancel input offset voltage resulting from bias current, as detailed in the *Device Functional Modes* section of the OPA2834 data sheet.

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Feature Description (continued)

8.3.4 Decompensated Architecture With Wide Gain-Bandwidth Product

Amplifiers such as the OPAX607 that are not unity-gain stable are referred to as *decompensated amplifiers*. The decompensated architecture typically allows for higher GBW, higher slew rate, and lower noise compared to a unity-gain stable amplifier with similar quiescent current. The increased available bandwidth reduces the rise time and the settling time of the op amp, allowing for sampling at faster rates in an ADC-based signal chain.

As shown in Figure 2, the dominant pole f_d is moved to the frequency f_1 in the case of a decompensated op amp. The solid A_{OL} plot is the open-loop gain plot of a traditional unity-gain stable op amp. The change in internal compensation in a decompensated amp such as the OPAX607 increases the bandwidth for the same amount of power. That is, the decompensated op amp has an increased bandwidth to power ratio when compared to a unity-gain stable op amp of equivalent architecture. Besides the advantages in the above mentioned parameters, an increased slew rate and a better distortion (HD2 and HD3) value is achieved because of the higher available loop-gain, compared to its unity-gain counterpart. The most important factor to be considered is to ensure the op amp is in a noise gain (NG) greater than G_{min}. A value of NG lower than G_{min} results in instability, as shown in Figure 2 because the 1/ß curve intersects the A_{OL} curve at 40 dB/decade. This method of analyzing stability is called the *rate of closure method*. See the precision lab training videos from TI for a better understanding on stability and for different techniques of ensuring stability.

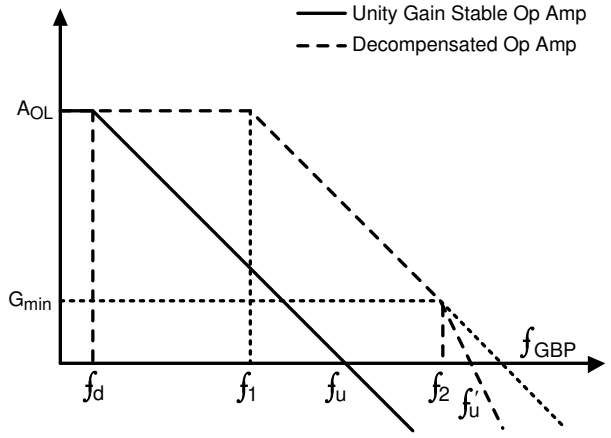

Figure 2. Gain vs Frequency Characteristics for a Unity-Gain Stable Op Amp and a Decompensated Op Amp

The OPAX607 is stable in a noise gain of 6 V/V (15.56 dB) or higher in conventional gain circuits; see Figure 3. The device has 9 MHz of small-signal bandwidth (SSBW) in this gain configuration with approximately 65° of phase margin. The high GBW and low voltage noise of the OPAX607 make the device suitable for general-purpose, high-gain applications.

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8.4 Device Functional Modes

The OPAX607 has two functional modes: normal operating mode and power-down ($\overline{PD}$) mode.

8.4.1 Normal Operating Mode

The OPAX607 is operational when the power-supply voltage is between 2.2 V (±1.1 V) and 5.5 V (±2.75 V). Most newer systems use a single power supply to improve efficiency and simplify the power tree design. The OPAX607 can be used with a single-supply power (V_{S-} connected to GND) with no change in performance from split supply, as long as the input and output pins are biased within the linear operating region of the device. The valid input and output voltage ranges are given in the *Electrical Characteristics* table. The outputs nominally swing rail-to-rail with approximately 10-mV headroom required for linear operation. The inputs can typically swing up to the negative rail (typically ground) and to within 1.1 V from the positive supply. Figure 3 shows changing from a ±2.5-V split supply to a 5-V single-supply.

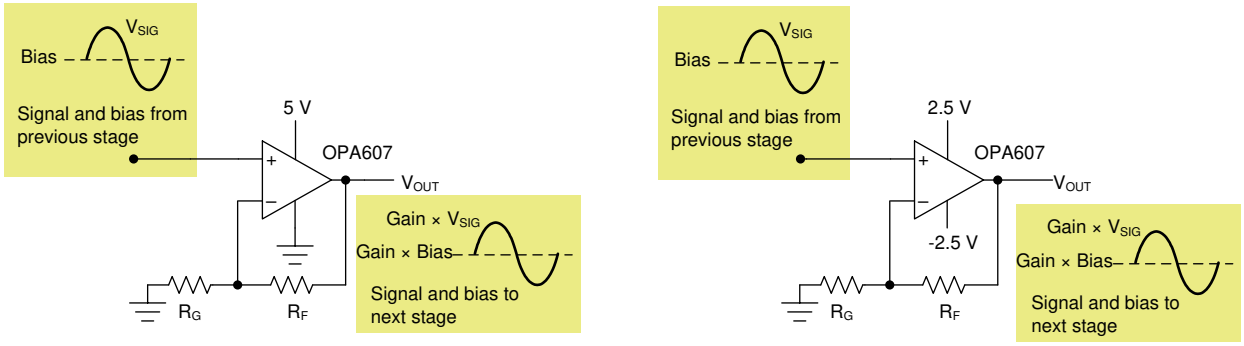

Figure 3. Single-Supply and Dual-Supply Operation

8.4.2 Power-Down Mode

The OPAX607 features a power-down mode for power critical applications. Under logic control, the amplifier can be switched from normal operation (consuming ≤ 1 mA) to a power-down current of less than 1 µA. When the $\overline{PD}$ pin is connected high, the amplifier is active. Connecting the $\overline{PD}$ pin to logic low disables the amplifier and places the output in a high-impedance state. The output of an op amp is high impedance similar to a tri-state high-impedance gate under a power-down condition; however, the feedback network behaves as a parallel load. If the power-down mode is not used, connect $\overline{PD}$ to the positive supply pin or leave floating. See the *Power Down (Device Enabled When Floating)* section in the *Electrical Characteristics* table for the enable and disable threshold voltages. The $\overline{PD}$ pin can be left floating to keep the op amp always enabled, which is primarily possible because of the presence of an internal pullup resistor within the op amp that, by default, always keeps the $\overline{PD}$ pin weakly tied to V_{S+}. However it is perfectly also acceptable to strengthen the pull up from $\overline{PD}$ pin by connecting a low value resistance from $\overline{PD}$ pin to V_{S+}. This shall help make the part less susceptibly to noise/transient pick up on the $\overline{PD}$ pin.

The $\overline{PD}$ logic states are transistor-transistor logic (TTL) with reference to the negative supply rail, V_{S-}. When the op amp is powered from a single supply and ground, driving from logic devices with similar V_{S+} voltages to the op amp does not require any special consideration. When the op amp is powered from a split supply, V_{S-} is below ground and an open-collector type of interface with a pullup resistor is more appropriate.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAX607 features a 50-MHz gain bandwidth with 900 µA of supply current, providing good AC performance at low-power consumption. The low input noise voltage of 3.8 nV/√Hz, the approximate pA of bias current, and a typical input offset voltage of 0.1 mV make the device very suitable for both AC and DC applications.

9.2 Typical Applications

9.2.1 High-Input Impedance (Hi-Z), Large-Gain Signal Front-End

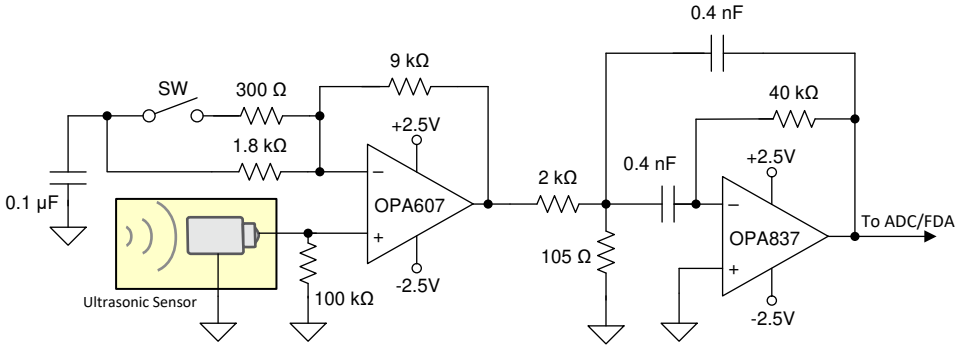

Figure 4. Hi-Z, Large-Gain Front-End Circuit

9.2.1.1 Design Requirements

The objective is to design a high-input impedance, high-dynamic range, signal-conditioning front-end. An example application for such a front-end circuit is the receive signal chain in an ultrasonic-based end equipment (EE) such as fish finders, printers, and flow meters. Table 1 lists the design requirements for this application.

Table 1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier supply	±2.5 V
Input signal frequency	200 kHz
Minimum voltage	300 µVrms
Minimum SNR at 300 µVrms	40 dB

9.2.1.2 Detailed Design Procedure

The concept used in an ultrasonic transmit (Tx) and receive (Rx) system is to send a large-amplitude tone at a known frequency and to calculate the time elapsed for the reflections to be received using a highly selective band-pass filter and to calculate the distance using:

Distance = Time × Speed (1)

Ultrasound speed is constant for a given medium and the time-of-flight (ToF) is calculated using the method explained in this section. The transmitter creates these ultrasonic signals by exciting a piezo crystal at its resonant frequency, which is in turn tuned to be in the ultrasonic frequency spectrum. Fish finders are one the primary end equipments that use such a Tx and Rx system. Based on the aperture angle and the distance to be measured in water, a frequency range from 50 kHz to 200 kHz is chosen as a base carrier frequency.

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The signal chain discussed here, is with a signal frequency at 200 kHz. The signal chain can be tweaked to support lower frequencies with an appropriate tuning of the band-pass filter. Because the reflected signal amplitude varies based on the distance of the reflecting object, one of the prime challenges in a design is to have a wide dynamic range.

To achieve a SNR of greater than 40 dB for signals from 300 uVrms to 30 mV, a variable-gain front-end stage based on the OPAX607 was chosen. The front-end stage has two gain settings: 6 V/V and 31 V/V. The SW (switch, relay, or analog mux) can be dynamically toggled to ensure maximum sensitively to the receiving signal. The OPAX607 proves to be an attractive solution for this front-end signal chain because of the high input impedance of the OPAX607. Besides the high input impedance, the OPAX607 also has very low quiescent current, making the device very suitable for a dense, high-channel-count system. The ultrasonic receive sensors (piezo crystal) have source impedance in the range of a few tens of kilohms. The OPAX607 has an input bias current of 20 pA (maximum). This small bias current results in reduced distortion when compared with a bipolar amplifier with input bias currents in the range of a few hundreds of nano-amperes. The OPAX607 large-gain front-end is followed by a narrowband band-pass filter that is tuned to a 200-kHz center frequency. The narrowband filter is designed using the OPA836,TI's 5-V bipolar family of op amps with excellent bandwidth to I_Q ratio. The driving stage of the OPA836 is a low-impedance output of the OPAX607, hence the higher input bias current of the OPA836 is not a cause of concern. The OPA836-based band-pass filter was designed using the techniques mentioned in the *Filter Design in Thirty Seconds* application report. A 1-µF capacitor is placed in the feedback network of the OPAX607 (as in Figure 4) to reject the DC bias in the received signal since the AC component is of interest in the received signal. The 1-µF capacitor gives the OPAX607 a high-pass response with a low cutoff frequency that ensures any DC signal picked up by the Rx node is filtered and only the AC signal gets gained.

Figure 6 shows the frequency response of Figure 4. As shown in Figure 6, the frequency response is a high-Q factor band-pass filter centered around 200 kHz. Designing such a high-Q band-pass filter helps eliminate white band noise along with other interferences present in the circuitry, resulting in a high SNR signal chain. The OPAX607 front-end and the OPA836-based band-pass filter together help achieve a total gain of 33 dB (44 V/V) or 50 dB (316 V/V) based on the SW (switch) position. Assuming the maximum full-scale input (FSR) of a dual supply (±2.5 V) powered ADC to be approximately 2.2 V, the 50-dB gain mode can be used to achieve greater than a 40-dB SNR for signals from 300 µVrms to 5 mVrms. Because the received signal is a sine wave at 5 mVrms, the V_{peak} of the 50-dB amplified signal crosses 2.2 V, resulting in a violation of the maximum input range of the following ADC, as per the FSR assumptions. Beyond 5 mV, the 33-dB gain mode is used and helps extend the maximum allowable input voltage from 5 mV to 50 mV. Figure 5 shows the achievable SNR as a function of the input voltage. Figure 5 shows that operating on the 50-dB gain mode is always favorable until the input Vrms voltage nears 5 mV to achieve higher SNR.

The SNR value is for the op-amp-based signal chain only. The SNR value of the ADC or fully differential amplifier (FDA) further effects the reported value in Figure 5 and must be vectorially added to arrive at the total signal-chain SNR.

9.2.1.3 Application Curves

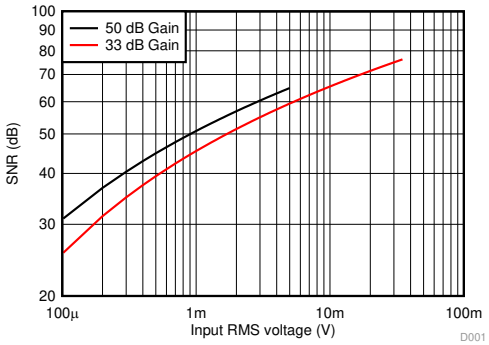

Figure 5. Signal-Chain SNR vs Input

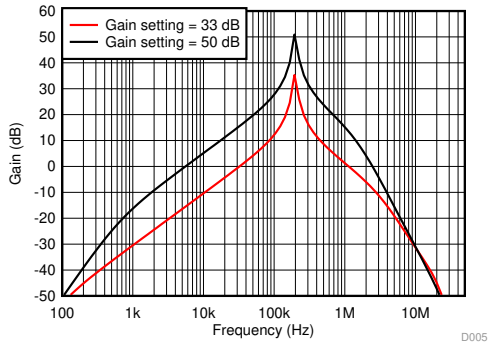

Figure 6. Gain vs Frequency

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9.2.2 Low-Cost, High-Speed Current Sensing

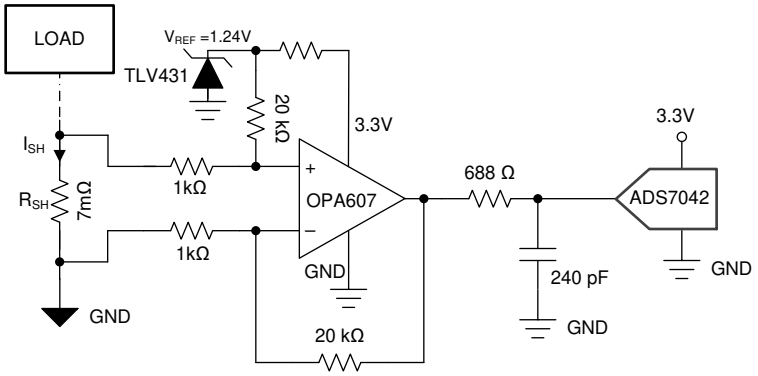

Figure 7. Hi-Z, High-Speed Front-End Circuit

9.2.2.1 Design Requirements

The objective of this design is to create a high-speed, high-gain signal chain for bidirectional current-sensing applications in power systems and motor drive systems. Detailed Design Procedure lists the design requirements of this application.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Amplifier and ADC supply	3.3 V
Peak current to be measured from load to ground	12 A
Peak current to be measured from ground to load	8 A
Accuracy of current measurement	0.1%
Maximum tolerable setting time	1 µs
Current sensing direction	Bidirectional

9.2.2.2 Detailed Design Procedure

The design requirements mentioned in Design Requirements help in designing the complete signal chain. The aim of the schematic (Figure 7) is to measure bidirectional current with relatively high accuracy in a low-side-sensing-based, high-frequency switching system.

As shown in Figure 7, a single op amp of high bandwidth is capable of accurately sensing current in a high-frequency switching circuit along with driving the consecutive SAR ADC.

Equation 2 gives the output of the OPAX607 (V_{OUT}) in Figure 7.

$$V_{OUT} = (20\ k\Omega / 1\ k\Omega \times I_{SH} \times R_{SH}) + V_{REF}$$

where

- $I_{SH} = I_{SHUNT}$ and $R_{SH} = R_{SHUNT}$ (2)

As shown Figure 7, the reference voltage applied is 1.24 V. In Equation 2, when the I_{SH} flowing across R_{SH} equals zero, the output of the difference amplifier is by default biased at a voltage equal to 1.24 V.

When the current (I_{SH}) flows from load to GND, the output of the OPAX607 rises above 1.24 V with a value equal to 20 × V_{SH} where:

$$V_{SH} = R_{SH} \times I_{SH} \quad (3)$$

Similarly, when the current flows from GND to load (in the opposite direction) the output of the OPAX607 goes below 1.24 V with a value proportional to 20 × V_{SH}.

The required peak current to be measured is 12 A in the first direction (load to GND).

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To calculate the required value of R_{SH}, a rule of thumb can be used. The maximum wattage that can be dissipated across a surface-mount device (SMD) resistor on a board having a good thermal layout is approximately 1 W.

Because $W = I^2 \times R$, plugging in the values for W and I_{SH} yields a R_{SH} value of approximately 7 mΩ.

The voltage developed across R_{SH} when I_{SH} = 12A is 84 mV.

The maximum allowable voltage at the input of an ADC such as the ADS7042, powered from a 3.3-V V_{CC}, is 3.3 V. This value can be found in the *Electrical Characteristics* table of the ADS7042 data sheet. However, for this design, the maximum allowable voltage at the input of the ADC under normal operating condition is assumed to be 3 V. Thus, the full-scale reading (FSR) for this design can be considered as 3 V. This value enables the design to have a 300-mV headroom in case the current exceeds the maximum rated value of 12 A. In other words, for faults and other unexpected conditions, the ADC is capable in measuring currents up to 15 A. The voltage across R_{SH} must be gained up before being fed to the ADC to increase the dynamic range of the sensing circuit. Because the considered FSR is 3 V, the output of the OPAX607 must swing from the nominal value of 1.24 V to 3 V, whereas an I_{SH} of 12 A is made to flow across R_{SH}.

Equation 4 defines the signal gain required by the op amp, which results in a gain of approximately 20 V/V.

$$\text{Gain} = (3\ \text{V} - 1.24\ \text{V}) / 84\ \text{mV} \quad (4)$$

Currents flowing across R_{SH} in either direction are gained by 20 V/V and swing the output above or below the nominal 1.24 V proportionally. If the gain value is frozen at 20 V/V, then Equation 5 defines the maximum current that can be measured in the direction of GND to load. I_{SH} = 8.8 A derived from Equation 5 meets the initial design requirement of current measuring capability of 8 A from GND to load.

$$I_{SH} = 1.24\ \text{V} / (R_{SH} \times 20\ \text{V/V}) \quad (5)$$

The next step is to arrive at the right GBW of an op amp that can drive a SAR ADC, while still being able to gain the signal by 20 V/V. As discussed further in this section, the calculations point towards an op amp with GBW in the vicinity of 50 MHz.

A 20-kHz switching system such as a motor driver card has a minimum possible duty cycle of approximately 5%. Thus when the control card is running at its lowest duty cycle, the width of the current pulse (as shown in Figure 8) shrinks to approximately 2.5 µs. The current pulses are very narrow and require the op amp output to settle to the final value within this short span of time. Figure 8 is an exaggerated figure showing the typical current waveform in a low-side current-sensing signal chain of a sinusoidal-driven brushless DC electric motor (BLDC). An op amp must be able to settle to its 0.1% accuracy within this time period to ensure the current value flowing across R_{SH} is captured in less than 2.5 µs. In reality, ensuring the op amp settles in less than 1 µs can be very desirable because the same amplification circuit can be fed to the comparator for short-circuit protection. This feature brings as additional value of using a high-bandwidth op amp in a current-sensing circuit. Because of the high bandwidth of the OPAX607, as with any op amp, the rise time (which is the prime parameter deciding the response time of the short circuit protection circuitry) becomes very small.

Equation 6 describes how the rise time and the bandwidth of a op amp are related to each other.

$$t_R\ (\text{sec}) = 0.35\ \text{Hz} / \text{BW} \quad (6)$$

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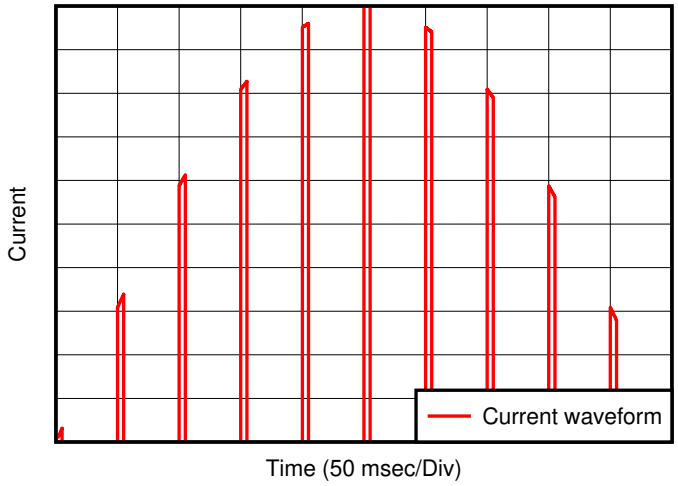

Figure 8. Low-Side Current-Sensing Waveform in a BLDC Motor Control

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An ADC capturing the data at 500 kSPS puts out a sampled data one time every 2 µs. Because the minimum current pulse duration while running at a 5% duty cycle is 2.5 µs, a 500-kSPS sampling rate ADC is sufficient for this BLDC current-sensing application. The ADS7042 is a low-power, 12-bit, 1-MSPS, SAR ADC. The ADS7042 is operated at 500 kSPS via SCLK at a frequency of 12.5 MHz, which is a standard clock frequency available for SPI communications. For an ADC running at a sampling rate of 500 kSPS on a clock of 12.5 MHz, the bandwidth of the op amp required to drive such an ADC is approximately 2.7 MHz. See the TI precision lab videos on driving SAR ADCs to understand the underlying calculation. The OPAX607 has a GBW of 50 MHz. With a gain of 20 V/V, the effective bandwidth available with the OPAX607 comes out to approximately 2.5 MHz, making the device the most suitable, cost-optimized amplifier for this application. The RC (240 Ω and 688 pF in Figure 7) charge bucket designed at the input of the SAR ADC is also derived from the calculations provided in the SAR ADC precision lab videos. The fundamental concept behind the design of this charge bucket is to ensure that the acquisition capacitor is charged up to the required final voltage within the acquisition window of the ADC.

The ADS7042 samples at 500 kSPS with a 12.5-MHz clock, which translates to a conversion time of 1 µs out of the total time period of 2 µs (1 / 500 kHz). These calculations for different sampling rates and clock frequencies can be found in the ADS7042 data sheet. With the conversion time of 1 µs out of the 2 µs, the OPAX607 is left with 1 µs to settle to the required accuracy of 0.1%. Because the full-scale voltage is assumed to be 3 V, an accuracy of 0.1% translates to a maximum allowable error voltage of 3 mV. Thus, the OPAX607 must settle to ±3 mV of its final intended value within 1 µs.

Figure 9 shows the TINA™ simulation plots for the OPAX607 driving the ADS7042. Input voltage (red) is the signal swing across the shunt resistance and the error signal (blue) is representative of the % error in the output of the op amp. As shown at the initial region of the graph in Figure 9, at the time instant (t_o), the input signal sharply transits from its lowermost point to the uppermost point. This transition can be considered as a short-circuit event or step increase in current resulting from a sudden metal-oxide-semiconductor field-effect transistor (MOSFET) switching. The output (black) waveform tries to follow the high slew rate input signal but is limited by the effective bandwidth of the op amp used. Thus, a higher bandwidth op amp results in the output being able to more closely track the input. The difference between the output and input is represented by the error waveform and the goal of the design is to reduce this error to less than 0.1% within the acquisition window of the ADC. The acquisition window of the ADC is shown in the yellow highlighted regions of Figure 9. Thus the % error signal (blue) must settle down to less than 0.1% before the end of this 1-µs window (within the yellow marked region). As illustrated in Figure 9, the error signal comfortably settles to the final value with an error % of –0.025%, which is well within the required 0.1% accuracy. Thus, the OPAX607 settles to 0.1% accuracy within 1 µs with a worst-case, 0-V to 3-V full-scale transient output that is also in a gain configuration of 20 V/V. The OPAX607 enables single-sample settling for the ADS7042 running on a 12.5-MHz clock with 500 kSPS, thus making the device a very cost-optimized, single amplifier solution.

Figure 10 gives the DC transfer characteristics of the circuit in Figure 7. As per the parameters from Table 2 the current across R_{SH} is varied in both directions and the voltage at the output of the OPAX607 is measured. Equation 7 describes the relation between the output of the OPAX607 and the I_{SH} current:

$$V_O = (20 \times I_{SH} \times 7\ m\Omega) + 1.24\ V \quad (7)$$

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The target of the design is to achieve 0.1% measurement accuracy across –8 A to 12 A. As shown in Figure 10, a DC accuracy of higher than 0.05% is achieved with the OPAX607. The simulations are captured with and without voltage offset calibration. The error at the output of the OPAX607 increases drastically below –8 A and above 12 A because of the RRO limitations of the OPAX607. Increasing the supply of the OPAX607 to 5-V V_{CC} with a suitable ADC enables a wider current measurement range to be obtained. Similarly reducing the gain from the existing 20 V/V or reducing the value of R_{SH} can equivalently help scale the required measurement current.

9.2.2.3 Application Curves

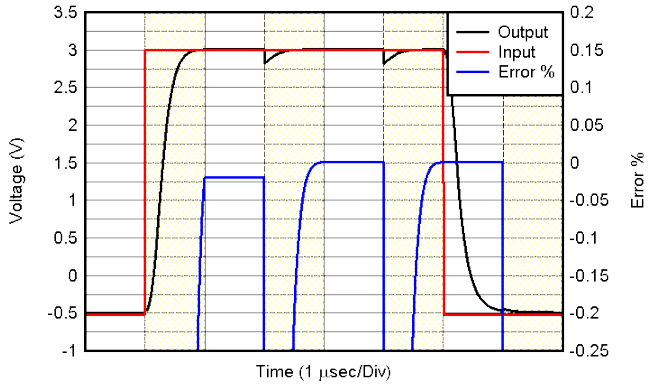

Figure 9. OPA607 Settling Performance With the ADS7042

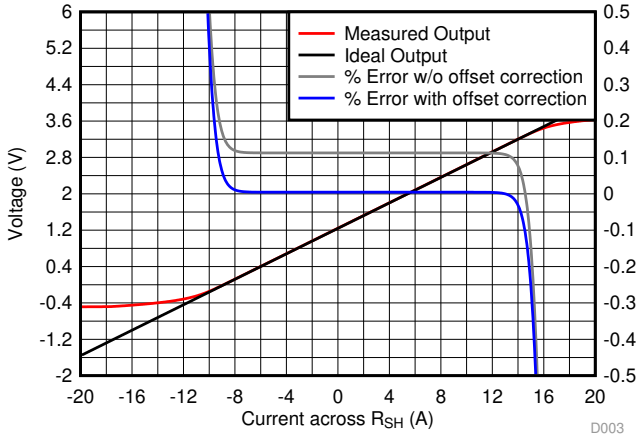

Figure 10. DC Current-Sense Transfer Function

9.2.3 Ultrasonic Flow Meters

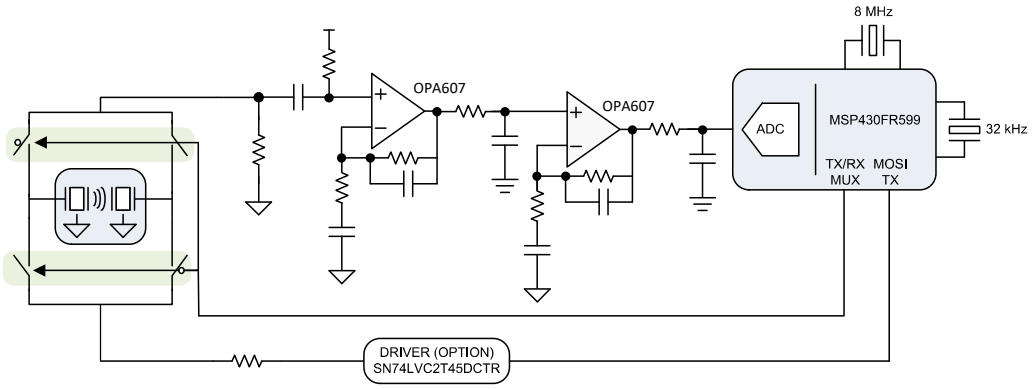

Figure 11. High-Gain Ultrasonic Front-End

9.2.3.1 Design Requirements

The OPAX607 has a wide operating voltage range of 2.2 V to 5.5 V with a maximum quiescent current of 1 mA. The availability of the inbuilt shutdown function enables designers to power cycle the front-end signal chain, reducing the net quiescent current even further. The minimum operating voltage range of 2.2 V proves to be very suitable for battery-powered applications such as the ultrasonic-based flow meters. The high-gain bandwidth of the OPAX607 enables the gain stages and the ADC drive stages to be designed and combined, thereby reducing component count. A schematic similar to that of Figure 7 can be used in ultrasonic flow meters for the front-end signal chain.

The *Ultrasonic sensing subsystem reference design for gas flow measurement* design guide has a detailed design procedure for ultrasonic-based sensing for gas flow measurement. The OPAX607 is a very suitable op amp for the discrete front-end design described in this design guide.

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10 Power Supply Recommendations

The OPAX607 is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V), applicable from –40°C to +125°C. Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

CAUTION

Supply voltages larger than 6 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power-supply pins of the circuit as a whole and of the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-equivalent series resistance (ESR), 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance; see Figure 12 and Figure 13.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Examples

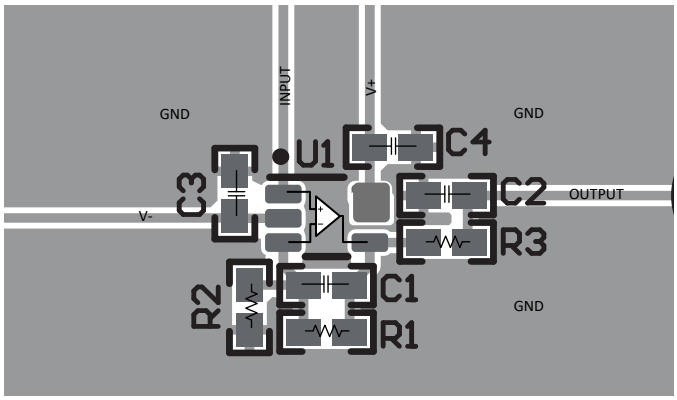

Figure 12. Operational Amplifier Board Layout for a Noninverting Configuration

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Layout Examples (continued)

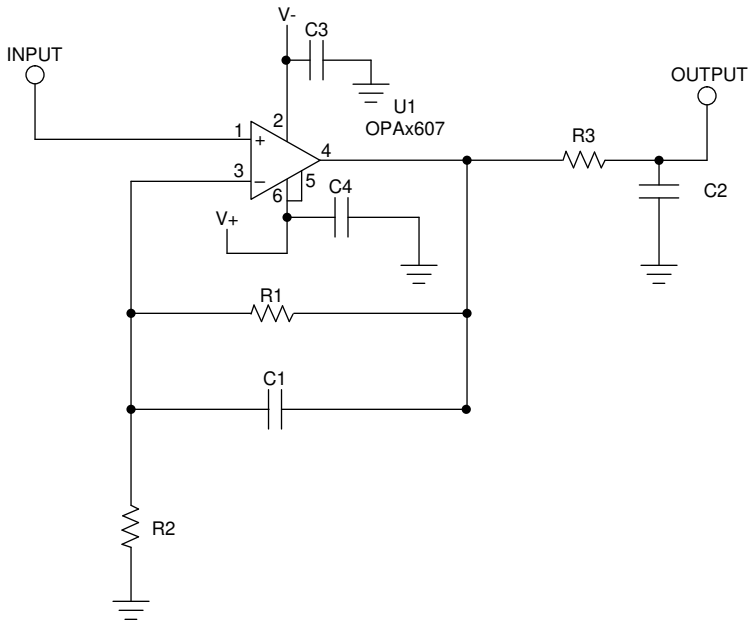

Figure 13. Layout Example Schematic

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Texas Instruments, precision lab videos

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *OPA2834 50-MHz, 170-μA, Negative-Rail In, Rail-to-Rail Out, Voltage-Feedback Amplifier* data sheet
- Texas Instruments, *ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC* data sheet
- Texas Instruments, *Ultrasonic Sensing Subsystem Reference Design For Gas Flow Measurement* design guide
- Texas Instruments, *OPAx836 Very-Low-Power, Rail-to-Rail Out, Negative Rail In, Voltage-Feedback Operational Amplifiers* data sheet
- Texas Instruments, *Filter Design in Thirty Seconds* application report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Trademarks

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Input Offset Drift: 1.5 μV/°C (maximum) is a trademark of others.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA607IDBVR	PREVIEW	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		
OPA607IDBVT	PREVIEW	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		
OPA607IDCKR	PREVIEW	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4	
OPA607IDCKT	PREVIEW	SC70	DCK	6	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1G4	
XOPA607IDBVT	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA607IDCKT	ACTIVE	SC70	DCK	6	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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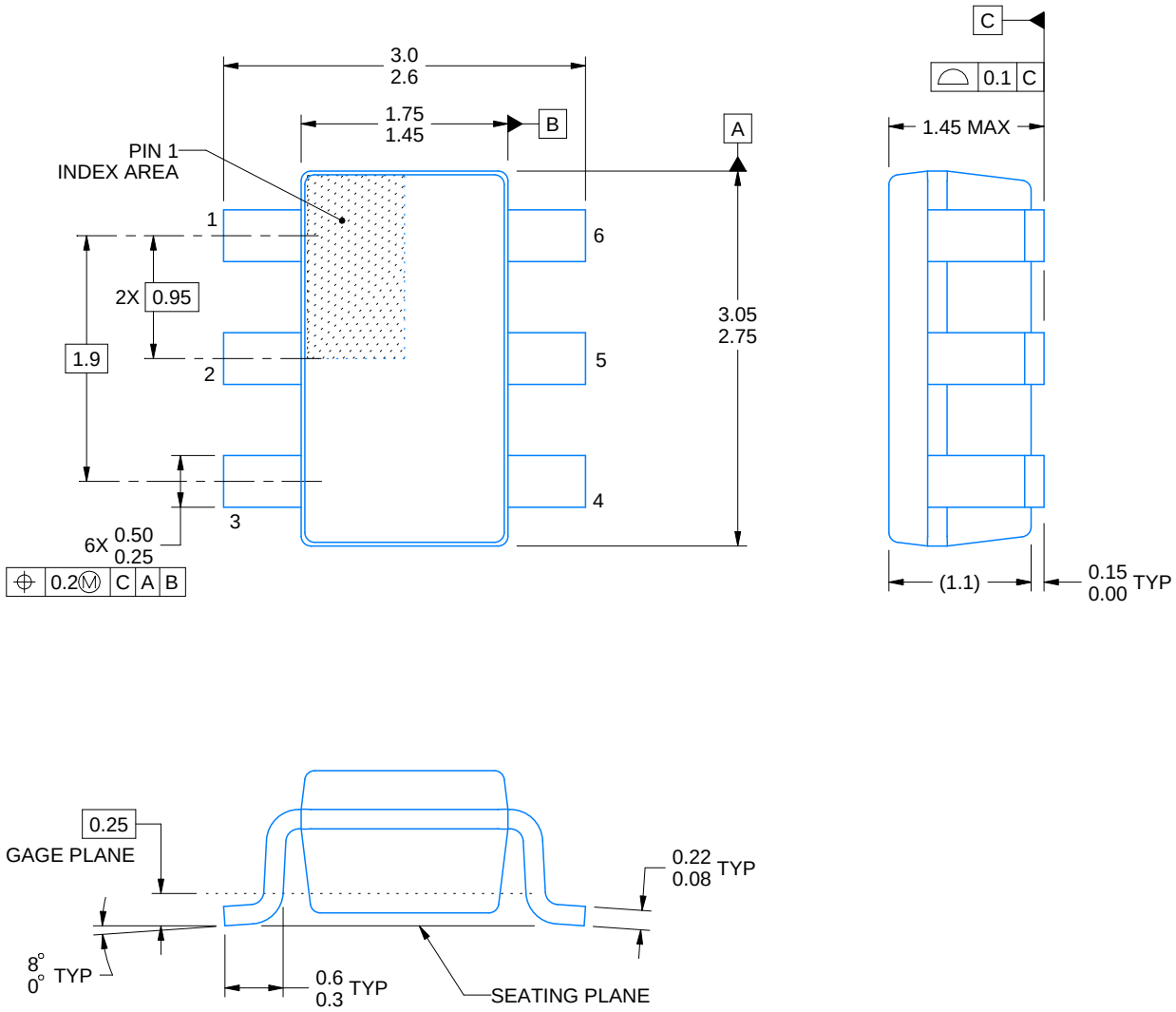
PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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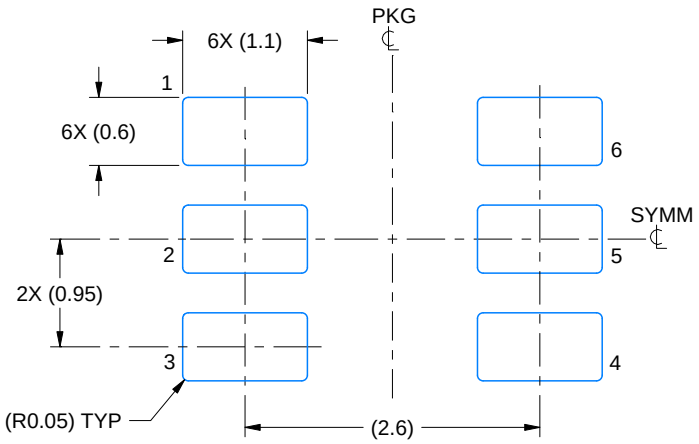
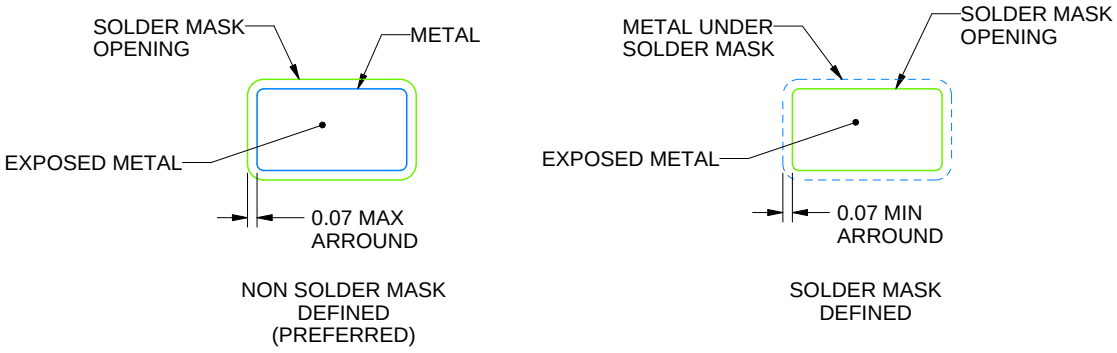
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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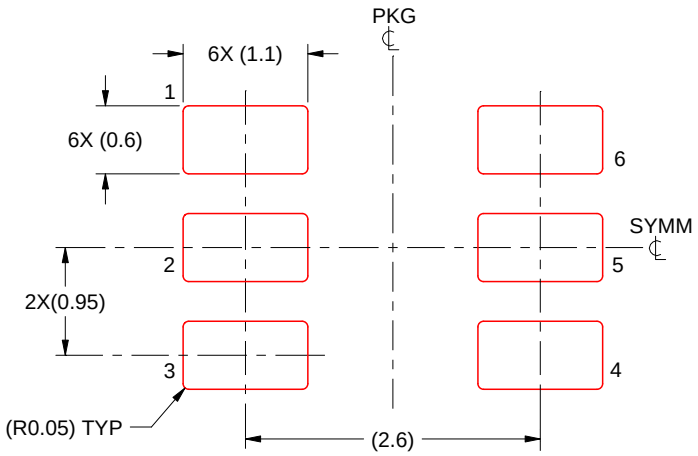
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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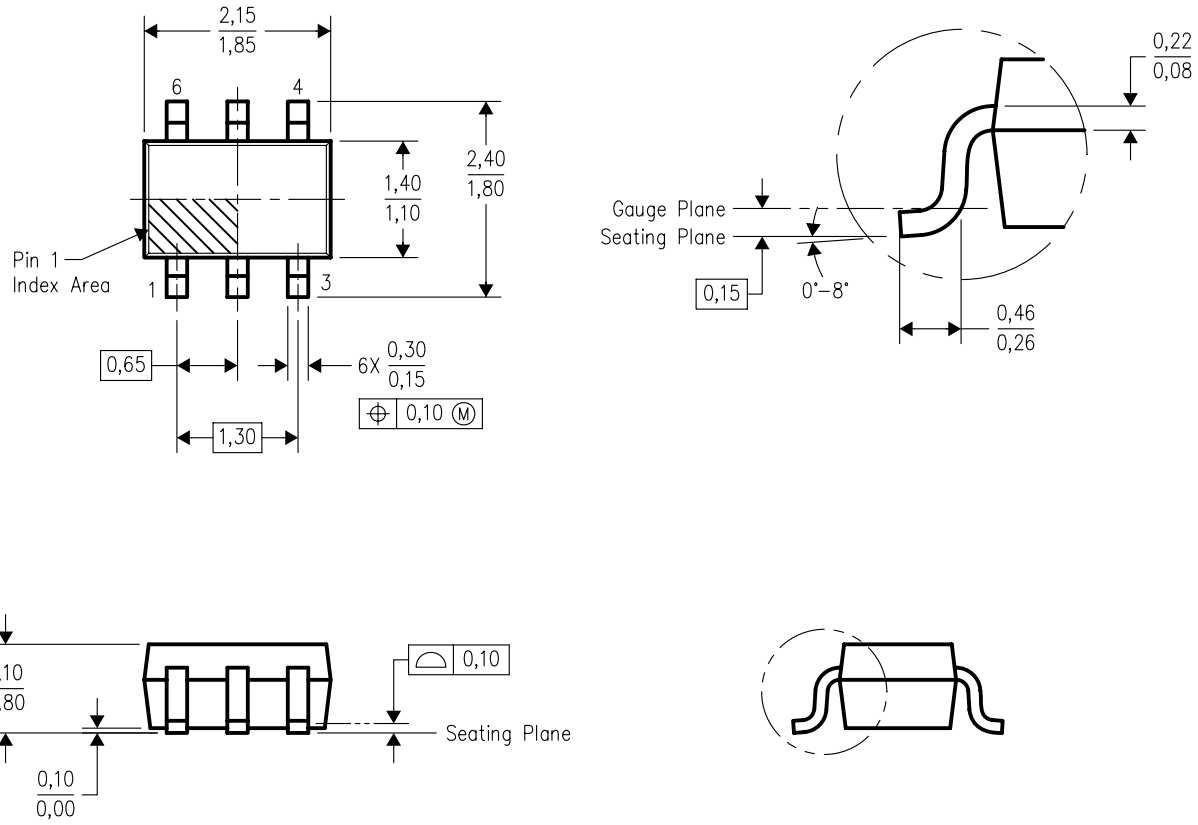
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

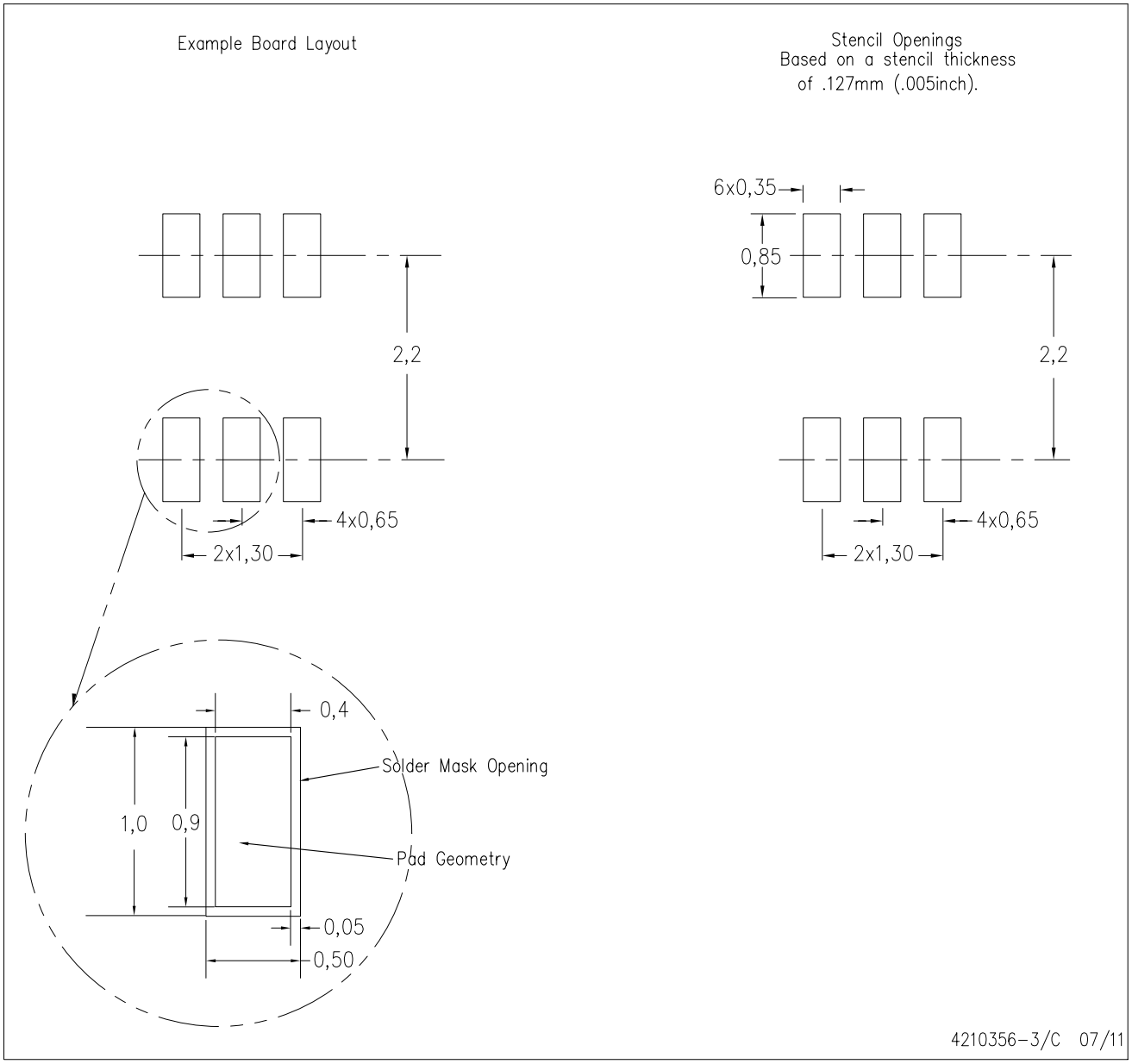
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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