

MMA8491Q

3-Axis Multifunction Digital Accelerometer

Rev. 2.1 — 26 April 2016

Data sheet: Technical data
COMPANY PUBLIC

1 General description

The MMA8491Q is a low voltage, 3-axis low-*g* accelerometer housed in a 3 mm x 3 mm QFN package. The device can accommodate two accelerometer configurations, acting as either a 45° tilt sensor or a digital output accelerometer with I^2C bus.

- As a 45° tilt sensor, the MMA8491Q device offers extreme ease of implementation by using a single line output per axis.
- As a digital output accelerometer, the 14-bit ±8 *g* accelerometer data can be read from the device with a 1 m*g*/LSB sensitivity.

The extreme low power capabilities of the MMA8491Q will reduce the low data rate current consumption to less than 400 nA per Hz.

2 Features and benefits

- Extreme low power, 400 nA per Hz
- Ultra-fast data output time, ~700 µs
- V_{DD} supply range of 1.95 V to 3.6 V
- 3 mm x 3 mm, 0.65 mm pitch with visual solder joint inspection
- ±8 *g* full-scale range
- 14-bit digital output, 1 m*g*/LSB sensitivity
- Output Data Rate (ODR), implementation based from < 1 Hz to 800 Hz[1]
- I^2C digital interface
- 3-axis, 45° tilt outputs

3 Typical applications

- Smart grid: tamper detect
- Anti-theft
- White goods tilt
- Remote controls

1 The ODR for this device is user defined by the period of the Enable pulsed signal. The maximum recommended frequency of the Enable signal or the ODR that can be achieved for this device is 800 Hz.

4 Ordering information

Table 1. Ordering information

Part Number	Temperature Range	Package	Shipping
MMA8491QT	–40 to +85 °C	QFN 12	Tray
MMA8491QR1	–40 to +85 °C	QFN 12	1000 pc / Tape & Reel
MMA8491QR2	–40 to +85 °C	QFN 12	5000 pc / Tape & Reel

5 Related documentation

The MMA8491Q device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most current versions of these documents:

1. Go to the NXP homepage at: http://www.nxp.com/
2. In the Keyword search box at the top of the page, enter the device number MMA8491Q. In the Refine Your Result pane on the left, click on the Documentation link.

6 Block diagram

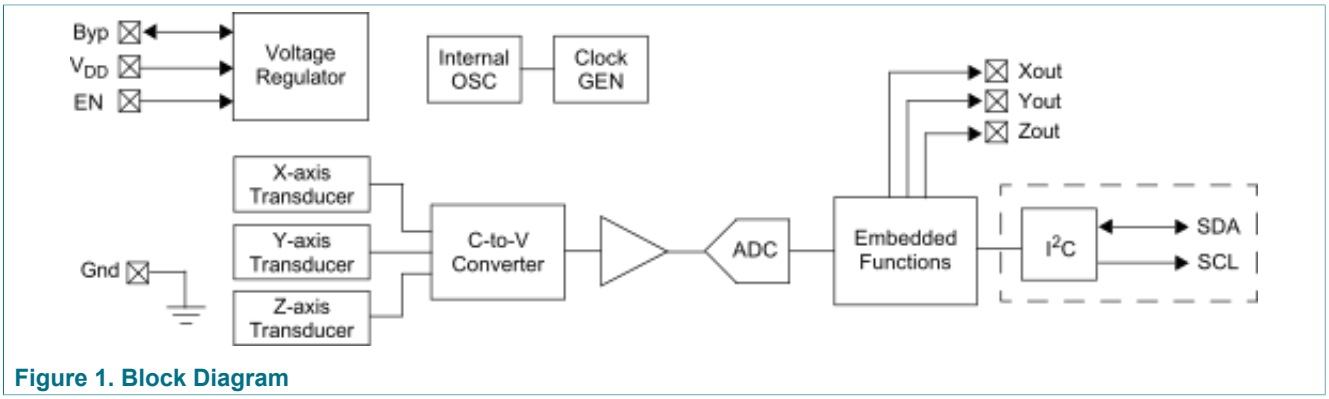


Figure 1. Block Diagram

7 Pinout

MMA8491Q is hosted in a 12-pin 3 mm x 3 mm QFN package. Ten pins are used for functions; two pins are unconnected. Refer to Table 2 for complete pin descriptions and functions.

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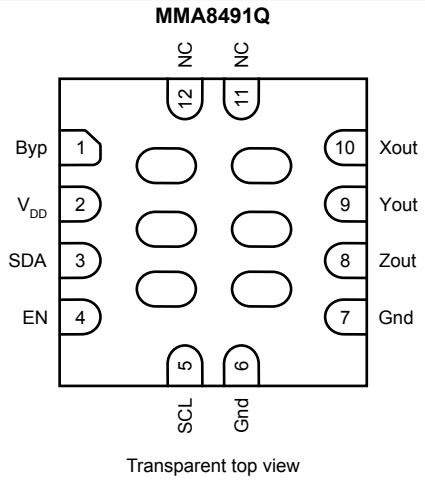


Figure 2. Pin connection diagram

Table 2. Pin descriptions

Pin	Symbol	Function	Description	Pin status
1	Byp	Internal regulator output capacitor connection	The internal regulator voltage of 1.8 V is present on this pin. Connect to external 0.1 µF bypass capacitor.	Output
2	V_{DD}	Power Supply	Device power is supplied through the V_{DD} line. Power supply decoupling capacitors should be placed as near as possible to pin 1 of the device.	Input
3	SDA	I^2C Data	I^2C Slave Data Line, open drain • 7-bit I^2C device address is 0x55 • The SDA and SCL I^2C connections are open drain, and therefore usually require a pull-up resistor	Input/Output
4	EN	Enable pin	The Enable pin fully turns on the accelerometer system when it is pulled up to logic high. The accelerometer system is turned off when the Enable pin is logic low.	Input
5	SCL	I^2C Clock	I^2C Slave Clock Line, open drain	Input
6	Gnd	Ground	Ground	Ground
7	Gnd	Ground	Ground	Ground
8	Zout	Push-pull Z-Axis Tilt Detection Output	• Output is high when acceleration is > 0.688 *g* (axis is |φ| > 45°). • Output is low when acceleration is ≤ 0.688 *g* (axis is |φ| ≤ 45°). • These pins are push-pull output pins.	Output
9	Yout	Push-pull Y-Axis Tilt Detection Output		Output
10	Xout	Push-pull X-Axis Tilt Detection Output		Output
11	NC	No internal connection	No internal connection	
12	NC	No internal connection	No internal connection	

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8 Recommended application diagram

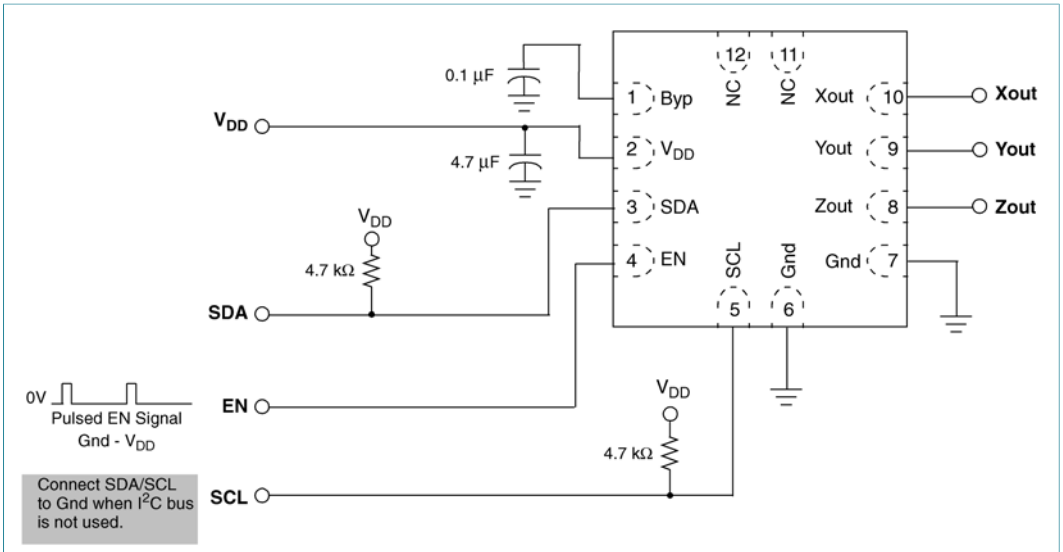


Figure 3. V_{DD} connects to power supply and EN is pulsed

To ensure the accelerometer is fully functional, connect the MMA8491Q as suggested in Figure 3.

- A capacitor must be connected to the Bypass pin (pin 1) to assist the internal voltage regulator. It is recommended to use a 0.1 µF capacitor. The capacitor should be placed as near as possible to the Bypass pin.
- The device power is supplied through the V_{DD} line. The power supply decoupling capacitor should be placed as close as possible to the V_{DD} pin.
  - Use a 1.0 or 4.7 µF capacitor when the V_{DD} and EN are not tied together.
  - When V_{DD} and EN are tied together, use a 0.1 µF capacitor. The 0.1 µF capacitor value has been chosen to minimize the average current consumption while still maintaining an acceptable level of power supply high frequency filtering.
- Both ground pins (pins 6 and 7) must be connected to ground.
- When the I^2C communication line is used, use a pull-up resistor to connect to line SDA and SCL. The SCL line can be driven by a push-pull driver, in which case, no pull-up resistor is necessary. If SDA and SCL pins are not used, then they should be tied to ground.

9 Sensing direction and output response

The MMA8491Q has three tilt detection outputs: Xout, Yout, and Zout. The following figure shows the output results at the six different orientation positions.

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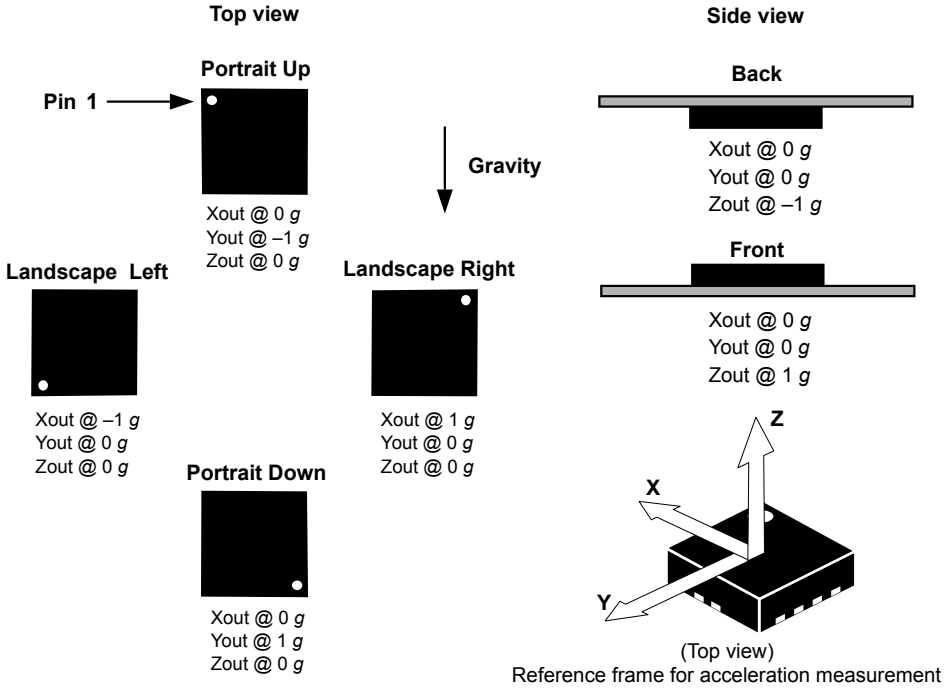


Figure 4. Sensitive axes orientation and output response to ±1 *g* (gravity) stimulus

10 Mechanical and electrical specifications

10.1 Absolute maximum ratings

Absolute maximum ratings are the limits the device can be exposed to without damage. Functional operation at absolute maximum rating is not guaranteed.

Although this device contains circuitry to protect against damage due to high static voltage or electrostatic fields, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum-rated voltage.

Table 3. Absolute maximum ratings

Symbol	Rating	Min	Max	Unit
g_{max}	Maximum acceleration (all axes, 100 µs)	—	10 000	V
V_{DD}	Analog supply voltage	–0.3	3.6	V
D_{drop}	Drop test	—	1.8	m
T_{AGOC}	Operating temperature	–40	+85	°C
T_{STG}	Storage temperature	–40	+125	°C

Table 4. ESD and latch-up protection characteristics

Symbol	Rating	Value	Unit
V_{HBM}	Human body model (HBM)	±2000	V
V_{MM}	Machine model (MM)	±200	V

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Symbol	Rating	Value	Unit
V_{CDM}	Charge device model (CDM)	±500	V
I_{LU}	Latch-up current at T_A = 85 °C	±100	mA

10.2 Mechanical characteristics

Table 5. Accelerometer mechanical characteristics

V_{DD} = 2.8 V, T = 25 °C, unless otherwise noted.
Typical number is the target number, unless otherwise specified.
All numbers are based on V_{DD} cap = 4.7 µF.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Full-scale measurement range	FS[1]	—	—	±8	—	*g*
Sensitivity	So[2]	—	973	1024	1075	counts/*g*
Calibrated sensitivity error	CSE[2]	All axes, all ranges	–5	—	5	%
Cross-axis sensitivity	CX_{SEN}[1]	Die rotation included	–4.2	—	4.2	%
Sensitivity temperature variation	TCS[1]	–40 °C to +85 °C	–0.014	—	0.014	%/°C
Zero-*g* level temperature variation	TCO[1]	–40 °C to +85 °C	–0.98	—	0.98	m*g*/°C
Zero-*g* level offset accuracy	TyOff[2][3]	—	–100	—	100	m*g*
Zero-*g* level after board mount	TyOffPBM[1][4]	—	–120	—	120	m*g*
Noise	RMS[1]	—	—	11.5	18	m*g*-rms
Nonlinearity	NL[1]	—	—	—	1	%FS
Threshold / *g*-value[5]	TDL[6]	25 °C	0.583	0.688	0.780	*g*
	TDL[1][4][6]	–40 °C to +85 °C	0.577	0.688	0.784	
Threshold / Tilt angle[7]	T_{AGOC}[1]	25 °C	35.6	43.5	51.3	degrees
		–40 °C to +85 °C	35.2	43.5	51.7	
Temperature range		—	–40	25	85	°C

[1] Verified by characterization; not tested in production.
[2] Parameters tested 100% at final test at room temperature.
[3] Before board mount.
[4] Post-board mount offset specifications are based on a 4-layer PCB, relative to 25 °C.
[5] Internal threshold of output level change (from 0 *g* reference), *g* values are calculated from trip angles.
[6] All angles are based on the trip angle from static 0 *g* to 1 *g*; the g-values are calculated from the trip angle.
[7] Internal threshold of output level change (from 0 *g* reference).

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10.3 Electrical characteristics

Table 6. Electrical characteristics

V_{DD} = 2.8 V, T = 25 °C, unless otherwise noted.
Typical values represent mean or mean ±1 σ values, depending on the specific parameter.
Typical number is the target number unless otherwise specified.
All numbers are based on V_{DD} cap = 4.7 µF.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage[1]	—	1.71	1.8	3.6	V
I_{DD}	Supply current in one-shot mode	V_{DD} = 2.8 V, EN is pulsed to V_{DD} for 1 ms	—	400[2][3][4]	980[1][5][6]	nA/Hz
I_{SD}	Supply current in shutdown mode	V_{DD} = 2.8 V, EN = 0	—	1.8[2][3]	68[1][6]	nA
C_{BYP}[2]	Bypass capacitor at Byp pin	—	70	100	470	nF
V_{OH}[1]	High level output voltage Xout, Yout, Zout	I_O = 500 µA	0.85 * V_{DD}	—	—	V
V_{OL}[1]	Low level output voltage Xout, Yout, Zout	I_O = 500 µA	—	—	0.15 * V_{DD}	V
V_{IH}[1]	High level input voltage EN	V_{DD} = 2.8 V	0.85 * V_{DD}	—	—	V
V_{IL}[1]	Low level input voltage EN	V_{DD} = 2.8 V	—	—	0.15 * V_{DD}	V
V_{OLS}[7]	Low level output voltage SDA	I_O = 3 mA	—	—	0.4	V
V_{IH}[7]	High level input voltage SDA, SCL	V_{DD} = 2.8 V	0.7 * V_{DD}	—	—	V
V_{IL}[7]	Low level input voltage SDA, SCL	V_{DD} = 2.8 V	—	—	0.3 * V_{DD}	V
I_{SOURCE}[1]	Output source current Xout, Yout, Zout	Voltage high level Vout = 0.85 x V_{DD}, V_{DD} = 2.8 V	—	—	7.3	mA
I_{SINK}[1]	Output sink current Xout, Yout, Zout	Voltage low level Vout = 0.15 x V_{DD}, V_{DD} = 2.8 V	—	—	8.9	mA
T_{ON} / T_{ACTIVE}[8]	Turn-on time Measured from the time EN = 1.95 V to valid outputs	—	—	720[2][3][4]	900[1][5][6]	µs
T_{RST}[7]	Reset Time The time between falling edge of EN and next rising edge of EN	V_{DD} = 2.8 V	1000	—	—	µs

[1] Verified by characterization; not tested in production.
[2] Evaluation data: not tested in production.
[3] Typical number is mean data.
[4] Data is based on typical bypass cap = 100 nF.
[5] Data is based on max bypass cap = 470 nF.
[6] Over temperature -40 °C to 85 °C.
[7] Guaranteed by design.
[8] For application connection, see Figure 3

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11 I²C Interface

Acceleration data may be accessed through an I²C interface, thus making the device particularly suitable for direct interfacing with a microcontroller. The MMA8491Q features three interrupt signals that indicate the tilt-sensing results on X, Y, Z axis respectively. The raw accelerometer data are readable via I²C at the same time when an interrupt signal is available.

The registers embedded inside the MMA8491Q are accessible through the I²C serial interface, Table 7. To enable the I²C interface, the EN pin must be HIGH. If either EN or V_{DD} are absent, the MMA8491Q I²C interface reads invalid data. The I²C interface may be used for communications along with other I²C devices. Removing power from the V_{DD} pin of the MMA8491Q does not affect the I²C bus.

Table 7. Serial interface pins

Pin	Description
SCL	I²C Serial Clock
SDA	I²C Serial Data

There are two signals associated with the I²C bus; the Serial Clock Line (SCL) and the Serial Data Line (SDA). The SDA is a bidirectional line used for sending and receiving the data to/from the interface. External pull-up resistors connected to V_{DD} are expected for SDA and SCL. When the bus is free both the lines are HIGH. The I²C interface is compliant with Fast mode (400 kHz, Table 8).

Table 8. I²C slave timing values

Parameter	Symbol	I2C Fast Mode[1]		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	0	400	kHz
Bus-free time between STOP and START condition	t_{BUF}	1.3	—	µs
(Repeated) START hold time	$t_{HD;STA}$	0.6	—	µs
Repeated START setup time	$t_{SU;STA}$	0.6	—	µs
STOP condition setup time	$t_{SU;STO}$	0.6	—	µs
SDA data hold time	$t_{HD;DAT}$	0.05	0.9[2]	µs
SDA setup time	$t_{SU;DAT}$	100	—	µs
SCL clock low time	t_{LOW}	1.3	—	µs
SCL clock high time	t_{HIGH}	0.6	—	µs
SDA and SCL rise time	t_r	20 + 0.1 C_b[3]	300	µs
SDA and SCL fall time	t_f	20 + 0.1 C_b[3]	300	µs
SDA valid time[4]	$t_{VD;DAT}$	—	0.9[2]	µs
SDA valid acknowledge time[5]	$t_{VD;ACK}$	—	0.9[2]	µs
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	µs
Capacitive load for each bus line	C_b	—	400	pF

[1] All values referred to VIH(min) ($0.3V_{DD}$) and V_{IL}(max) ($0.7V_{DD}$) levels.

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[2] This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
[3] Cb = total capacitance of one bus line in pF.
[4] $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[5] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

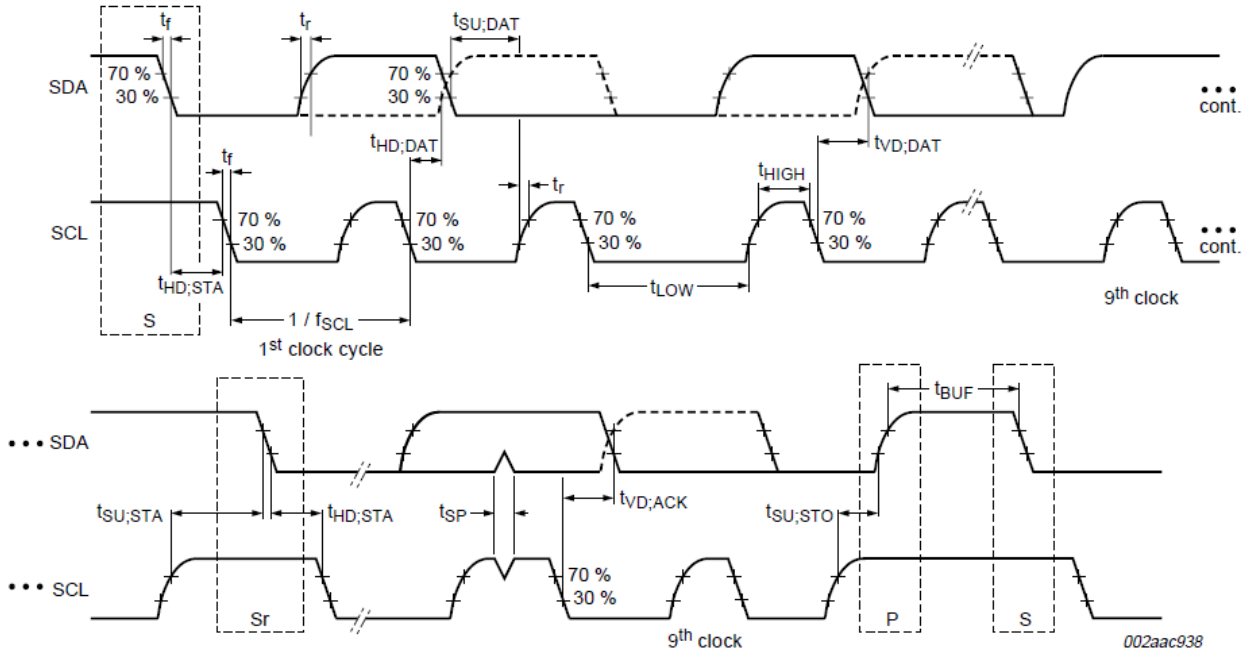


Figure 5. I²C slave timing diagram

11.1 I²C read operations

The transaction on the bus is started through a start condition (START) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH.

After START has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first seven bits, and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, then the device considers itself addressed by the Master.

The ninth clock pulse, following the slave address byte, and each subsequent byte, is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock period.

A LOW-to-HIGH transition on SDA while SCL is HIGH is defined as a stop condition (STOP). A data transfer is always terminated by a STOP.

A Master may also issue a repeated START during a data transfer. The MMA8491Q expects repeated STARTs to be used to randomly read from specific registers.

The MMA8491Q accelerometer standard 7-bit slave address is 01010101(0x55).

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Table 9. I^2C device address sequence

Command	[7:1] Device Address	[7:1] Device Address	[0] R/W	[7:0] 8-bit Final Value
Read	01010101	0x55	1	0xAB
Write	01010101	0x55	0	0xAA

11.1.1 Single-byte read

The transmission of an 8-bit command begins on the falling edge of SCL. After the 8 clock cycles are used to send the command, note that the data returned is sent with the MSB first after the data is received. Figure 6 shows the timing diagram for the accelerometer 8-bit I^2C read operation.

1. The Master (or MCU) transmits a start condition (ST) to the MMA8491Q, slave address (0x55), with the R/W bit set to “0” for a write, and the MMA8491Q sends an acknowledgement.
2. Then the Master (or MCU) transmits the address of the register to read and the MMA8491Q sends an acknowledgement.
3. The Master (or MCU) transmits a repeated start condition (SR) and then addresses the MMA8491Q (0x1D) with the R/ W bit set to 1 for a read from the previously selected register.
4. The Slave then acknowledges and transmits the data from the requested register.
5. The Master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

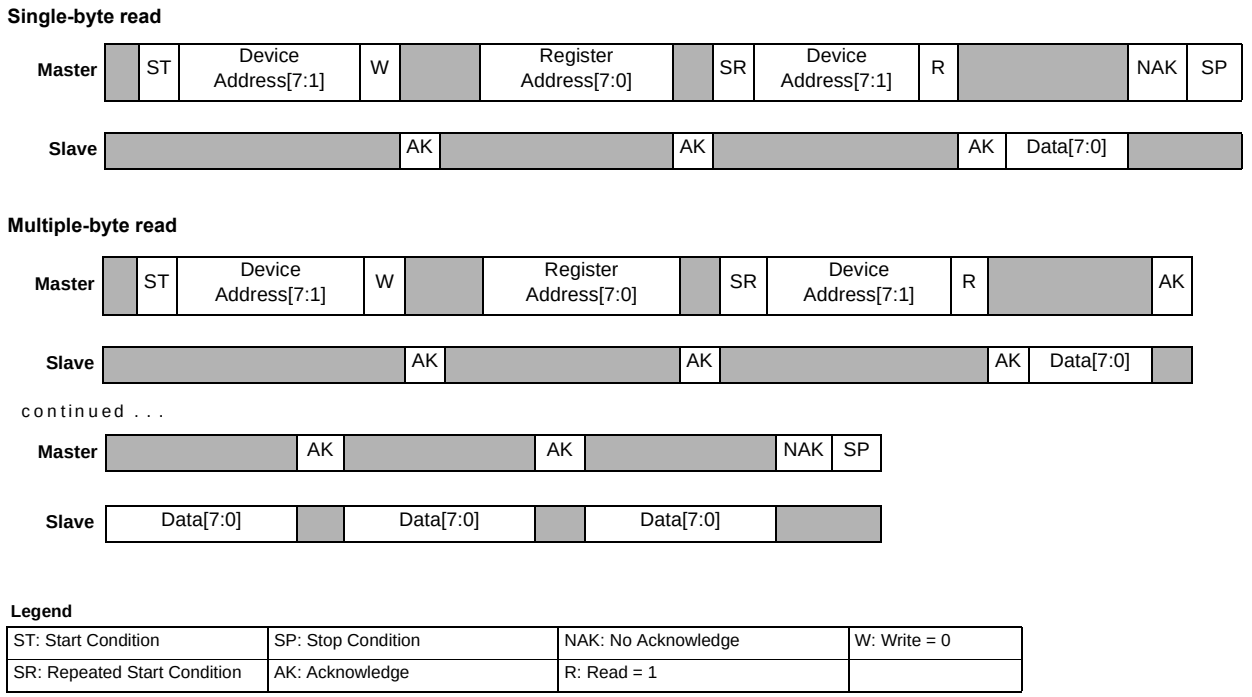
11.1.2 Multiple-byte read

When performing a multiple-byte read or *burst read*, the MMA8491Q automatically increments the received register address commands after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each MMA8491Q acknowledgment (AK) is received, until a no acknowledge (NAK) occurs from the Master, followed by a stop condition (SP) signaling an end of transmission.

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11.1.3 I2C data sequence diagrams

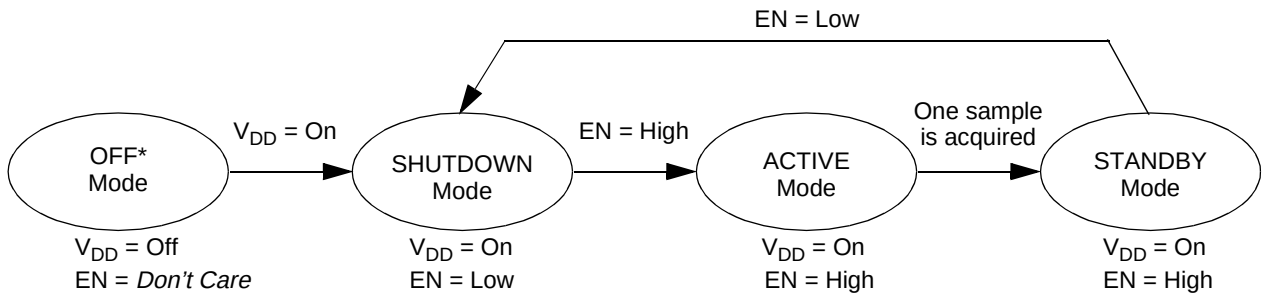


Legend

ST: Start Condition	SP: Stop Condition	NAK: No Acknowledge	W: Write = 0
SR: Repeated Start Condition	AK: Acknowledge	R: Read = 1	

Figure 6. I²C data sequence diagrams

12 Modes of operation



*OFF mode can be entered from any state by removing the power.

Figure 7. MMA8491Q operating modes

Table 10. MMA8491Q operating modes

Mode	Conditions	Function description	Digital output state
OFF	V_{DD} = OFF EN = *Don't Care*	Device is powered off.	Hi-Z
SHUTDOWN	V_{DD} = ON EN = Low	All blocks are shut down.	Hi-Z

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Mode	Conditions	Function description	Digital output state
ACTIVE	V_{DD} = ON EN = High	All blocks are enabled. Device enters Standby mode automatically after data conversion.	Deasserted, Xout = 0, Yout= 0, Zout = 0
STANDBY	V_{DD} = ON EN = High	Only digital output subsystem is enabled. Data is valid and available only in this stage.	Active, I^2C outputs become valid

12.1 ACTIVE mode

The accelerometer subsystem is turned on at the rising edge of the EN pin, and acquires one sample for each of the three axes. Note that EN should not be asserted before V_{DD} reaches 1.95 V. Samples are acquired, converted, and compensated for zero-g offset and gain errors, and then compared to an internal threshold value of 0.688 *g* and stored.

- If any of the X, Y, Z axes sample's **absolute value > this threshold**, then the corresponding outputs on these axes drive logic highs.
- If any of the X, Y, Z axes sample's **absolute value ≤ this threshold**, then the corresponding outputs on these axes drive logic lows.

Read register 00h in this stage to determine whether the sample data is ready to be read.

12.2 STANDBY mode

The device enters STANDBY mode automatically after the previously described function (powers into SHUTDOWN mode, ACTIVE mode) is accomplished. The digital output system outputs valid data, which can also be read via the I^2C communication bus. This is the appropriate phase to read the measured data, either from the three push-pull logic outputs or through the I^2C transaction. All other subsystems are turned off.

These outputs are held until the MMA8491Q operation mode changes. For lower power consumption, deassert the EN pin as soon as data is read (to enter SHUTDOWN mode).

12.3 Next sample acquisition

The MMA8491Q needs to be brought back to the ACTIVE mode again by pulling EN pin up to a Logic 1. Another option is to power down the device and start from OFF mode as illustrated in Figure 7.

For applications where sampling intervals are greater than 30 seconds, the host can shut off the tilt sensor power after acquisition of tilt sensor output data to conserve energy and prolong battery life.

12.4 Power-up timing sequences

The power-up timing sequence for MMA84591Q is shown in the following figure, where V_{DD} is powered and the EN pin is activated to acquire a single sample. Additional samples can be acquired by repeating the EN pulse.

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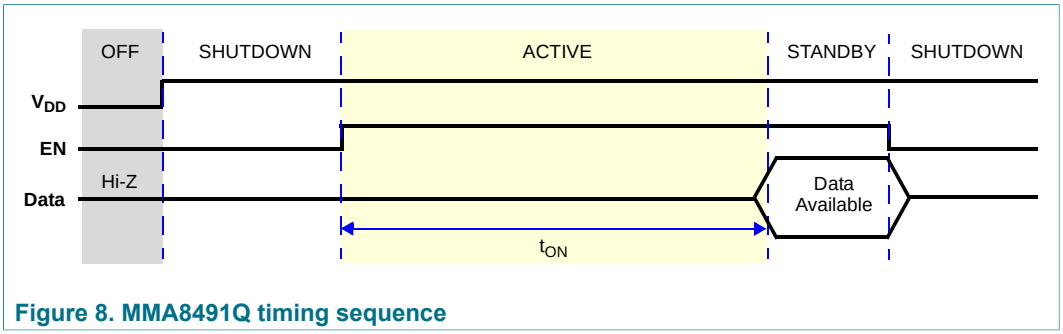


Figure 8. MMA8491Q timing sequence

t_{ON} is the time between EN to the end of ACTIVE stage, after which the newly acquired sample data is available.

12.5 45° tilt detection

The output value changes according to the **absolute value** of the acceleration of the MMA8491Q compared to the threshold:

- When the acceleration's **absolute value** > the threshold 0.688 *g*, the output = 1.
- When the acceleration's **absolute value** ≤ the threshold, the output = 0.

$$Output = \begin{cases} 1, when\ (|\text{g-value}| > 0.688g) \\ 0, when\ (|\text{g-value}| \leq 0.688g) \end{cases}$$

For example,

- When the MMA8491Q is set on a table, it senses 1 *g* acceleration on Z-axis and senses 0 *g* on X- and Y-axes.
- When the MMA8491Q is flipped upside down on the table, it senses –1 *g* acceleration on Z-axis and senses 0 *g* on X- and Y-axes.

In both cases Xout = 0, Yout = 0, and Zout = 1.

12.6 Tilt angle

Tilt angles can be calculated from the *g*-value threshold using the equation below. The tilt threshold is 0.688 *g*, which corresponds to 43.5°. Figure 9 illustrates the tilt angle threshold.

$$Tilt\ Angle = asin\left(\frac{g\text{-value}}{1g}\right)$$

- When 0 *g* acceleration is present on an axis, the tilt angle = 0°; when 1 *g* acceleration is present on an axis, the tilt angle = 90°.
- When the tilt angle > the tilt threshold, the output for the axis is HIGH; when the tilt angle ≤ the tilt threshold, the output for the axis is LOW.

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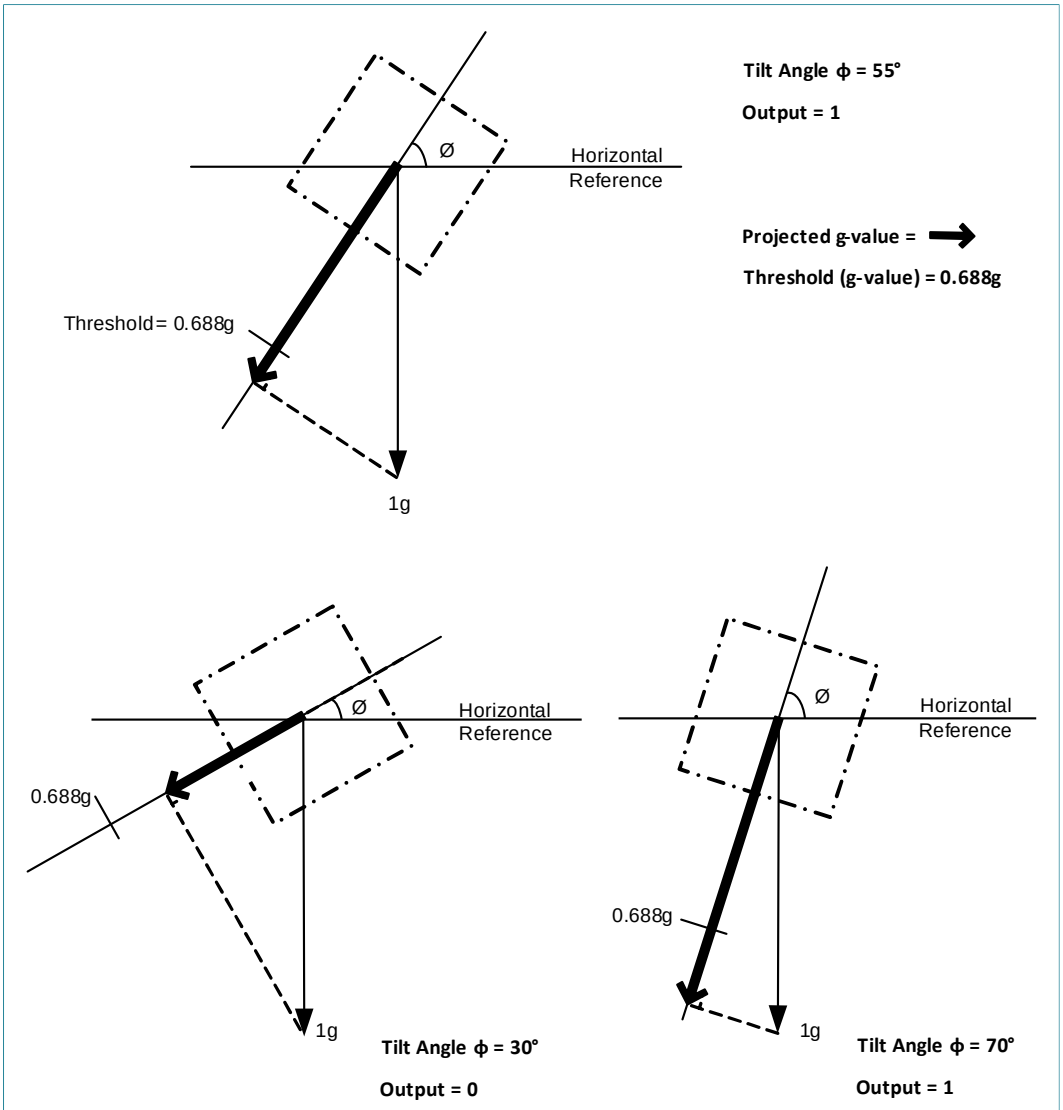


Figure 9. MMA8491Q output is based on tilt angle and sensor g-value

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13 Register descriptions

Table 11. Register address map

Name	Type	Register Address	Auto-increment Address[1]	Reset	Comment
STATUS	R	0x00	0x01	0x00	Read time status
OUT_X_MSB	R	0x01	0x02	Output	[7:0] are the 8 MSBs of the 14-bit sample
OUT_X_LSB	R	0x02	0x03	Output	[7:2] are the 6 LSBs of the 14-bit sample
OUT_Y_MSB	R	0x03	0x04	Output	[7:0] are the 8 MSBs of the 14-bit sample
OUT_Y_LSB	R	0x04	0x05	Output	[7:2] are the 6 LSBs of the 14-bit sample
OUT_Z_MSB	R	0x05	0x06	Output	[7:0] are the 8 MSBs of the 14-bit sample
OUT_Z_LSB	R	0x06	**0x00**	Output	[7:2] are the 6 LSBs of the 14-bit sample

[1] Auto-increment is the I^2C feature that the I^2C read address is automatically updated after each read. Auto-increment addresses that are not a simple increment are highlighted in bold. The auto-increment addressing is only enabled when device registers are read using I^2C burst read mode. Therefore the internal storage of the auto-increment address is cleared whenever a stop-bit is detected.

Notes:

- *Register contents are preserved when EN pin is set high after sampling.*
- *Register contents are reset when EN pin is set low.*

13.1 STATUS - Status register (address 00h)

Register 0x00 reflects the real-time status information of the X, Y, and Z sample data. The data read bits (ZYXDR, ZDR, YDR, XDR) are set when samples are taken and ready to be read.

Table 12. STATUS - Status register (address 00h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	—				ZYXDR	ZDR	YDR	XDR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 13. STATUS - Status register (address 00h) field descriptions

Field	Description
3 ZYXDR	X-, Y-, Z-axis new Data Ready (and available) • ZYXDR signals that a new sample for all channels is available. • ZYXDR is cleared when the high-bytes of the acceleration data (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) of all channels are read.. 0: No new set of data ready (default value) 1: A new set of XYZ acceleration and temperature data is available
2 ZDR	Z-axis new Data Ready (and available) • ZDR is set whenever a new acceleration sample related to the Z-axis is generated. • ZDR is cleared anytime OUT_Z_MSB register is read. 0: No new Z-axis data is ready (default value) 1: A new Z-axis data is ready

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Field	Description
1 YDR	Y-axis new Data Ready (and available) • YDR is set whenever a new acceleration sample related to the Y-axis is generated. • YDR is cleared anytime OUT_Y_MSB register is read. 0: No new Y-axis data ready (default value) 1: A new Y-axis data is ready
0 XDR	X-axis new Data Ready (and available) • XDR is set whenever a new acceleration sample related to the X-axis is generated. • XDR is cleared anytime OUT_X_MSB register is read. 0: No new X-axis data ready (default value) 1: A new X-axis data is ready

13.2 Output data registers (addresses 01h to 06h)

These registers contain the X-axis, Y-axis, and Z-axis14-bit output sample data (expressed as 2's complement numbers).

- OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the autoincrementing address range of 0x01 – 0x06.
- The LSB registers can only be read immediately following the read access of the corresponding MSB register. A random read access to the LSB registers is not possible.
- Reading the MSB register and then the LSB register in sequence ensures that both bytes (LSB and MSB) belong to the same data sample, even if a new data sample arrives between reading the MSB and the LSB byte.
- The accelerometer data registers should be read only after the status register has confirmed that new data on all axes is available.

Table 14. OUT_X_MSB - Output data register (address 01h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	XD[13:6]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 15. OUT_X_LSB - Output data register (address 02h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	XD[5:0]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

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Table 16. OUT_Y_MSB - Output data register (address 03h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	YD[13:6]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 17. OUT_Y_LSB - Output data register (address 04h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	YD[13:6]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 18. OUT_Z_MSB - Output data register (address 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	OUT_Z[7:0]							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 19. OUT_Z_LSB - Output data register (address 06h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ZD[5:0]						—	—
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

13.3 Accelerometer output conversion

Table 20. Accelerometer output data

14-bit Data	Range ±8 *g* (1 mg/count)
01 1111 1111 1111	+8.000 *g*
01 1111 1111 1110	+7.998 *g*
...	...
00 0000 0000 0000	0.000 *g*
11 1111 1111 1111	–0.001 *g*
...	...
10 0000 0000 0001	–7.998 *g*
10 0000 0000 0000	–8.000 *g*

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14 Mounting guidelines

Surface-mount printed circuit board (PCB) layout is a critical portion of the total design. The footprint for the surface mount package must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the package will self-align when subjected to a solder reflow process. The purpose is to minimize the stress on the package after board mounting. The MMA8491Q accelerometers use the QFN package. This section describes suggested methods of soldering and mounting these devices to the PCB for consumer applications.

14.1 Overview of soldering considerations

The information provided here is based on experiments executed on QFN devices. They do not represent exact conditions present at a customer site. Therefore, information herein should be used as guidance only, and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

14.2 Halogen content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

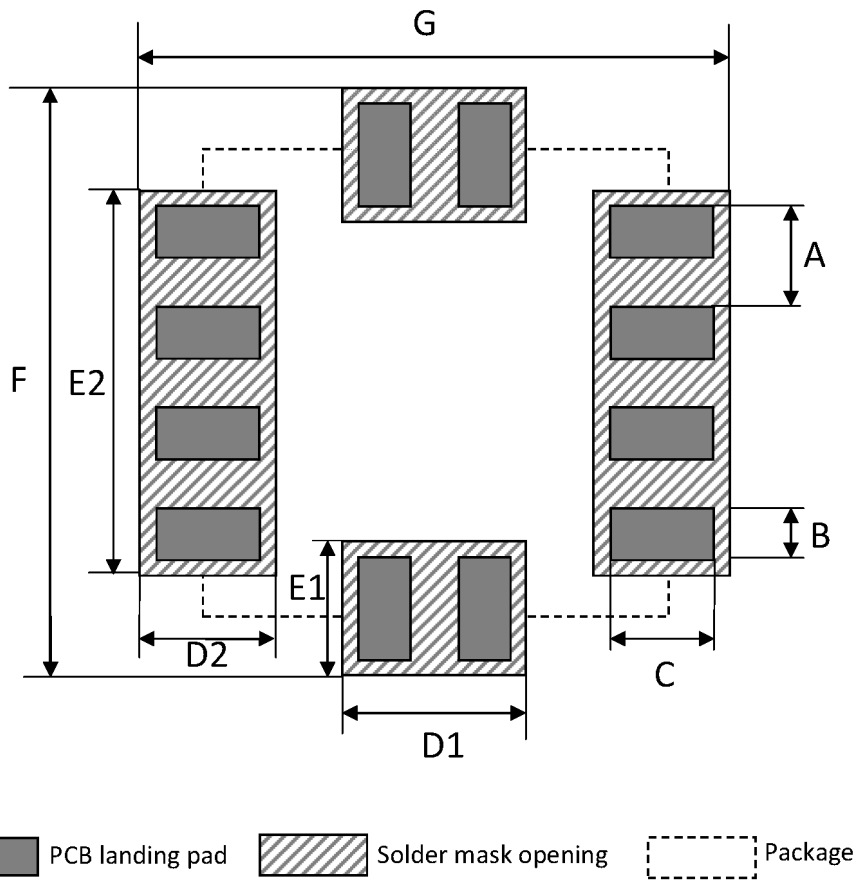
14.3 PCB mounting recommendations

- Do not solder down the six exposed pads under the package, thus minimizing board-mounting stress impact to product performance.
- PCB landing pad is 0.675 mm x 0.325 mm as shown in Figure 10.
- Solder mask opening = PCB land pad edge + 0.2 mm larger all around.
- Stencil opening size is 0.625 mm x 0.3 mm.
- Stencil thickness is 100 µm or 125 µm.
- The solder mask should not cover any of the PCB landing pads, as shown in Figure 10.
- No additional via nor metal pattern underneath package on the top of the PCB layer.
- Do not place any components or vias within 2 mm of the package land area. This may cause additional package stress if it is too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on NC pads, to have the same length of exposed trace for all pads.
- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Customers are advised to be cautious about the proximity of screw-down holes to the sensor, and the location of any press fit to the assembled PCB when in an enclosure. It is important that the assembled PCB remain flat after assembly to keep electronic operation of the device optimal.
- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.
- NXP sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These

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terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.



Symbol	Description	Value (mm)
A	Pitch	0.650
B	Landing Pad Width	0.325
C	Landing Pad Length	0.675
D1	Solder Mask Pattern Width	1.175
D2	Solder Mask Pattern Length	0.875
E1	Solder Mask Pattern Width	0.875
E2	Solder Mask Pattern Length	2.475
F	I/O Pads Extended Length	3.8
G	I/O Pads Extended Length	3.8

Figure 10. PCB footprint guidelines

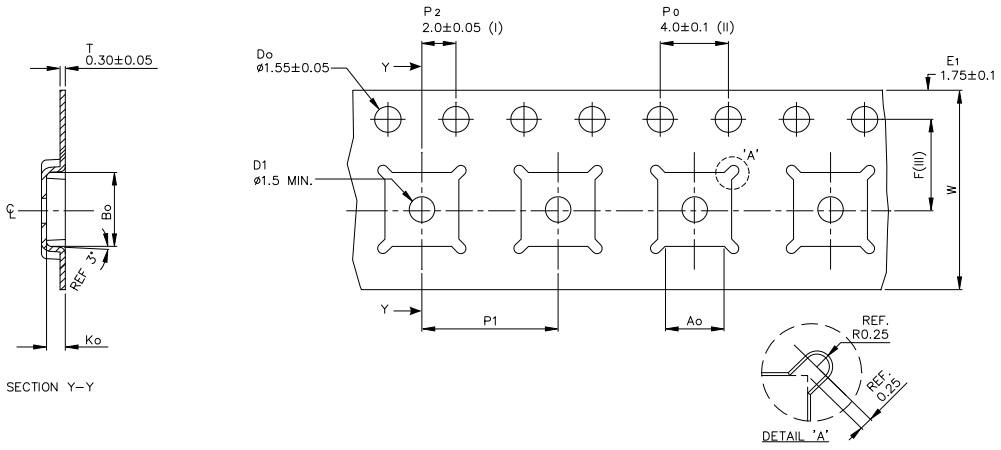
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15 Package Information

The MMA8491Q uses a 12-lead QFN package, case number 98ASA00290D.

15.1 Tape and reel information



Ao	4.35 +/− 0.1
Bo	4.35 +/− 0.1
Ko	1.10 +/− 0.1
F	5.50 +/− 0.05
P1	8.00 +/− 0.1
W	12.00 +/− 0.3

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
(V) Typical SR value Max 10^9 OHM/SQ
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Figure 11. Tape dimensions

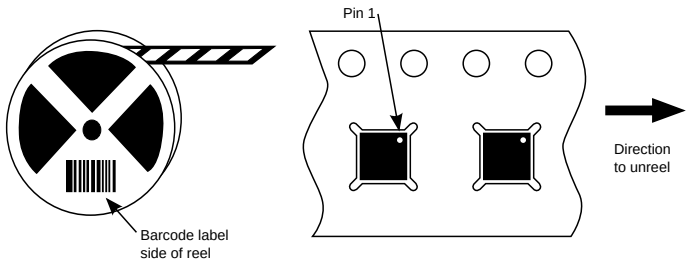


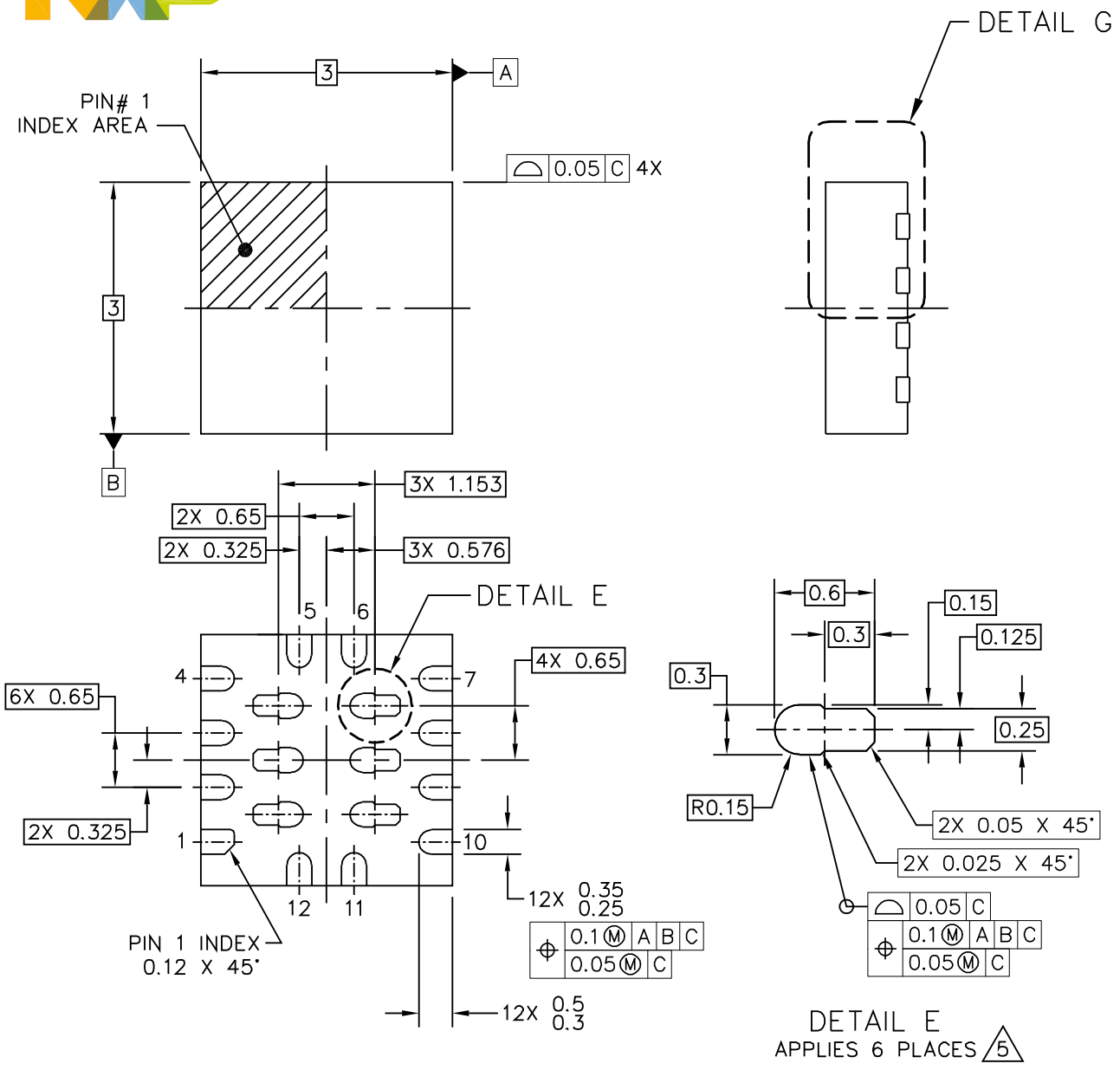
Figure 12. Tape and reel orientation

15.2 Package description

This drawing is available for download at http://www.nxp.com/files/shared/doc/package_info/98ASA00290D.pdf. Please consult the most recently issued drawing before initiating or completing a design.

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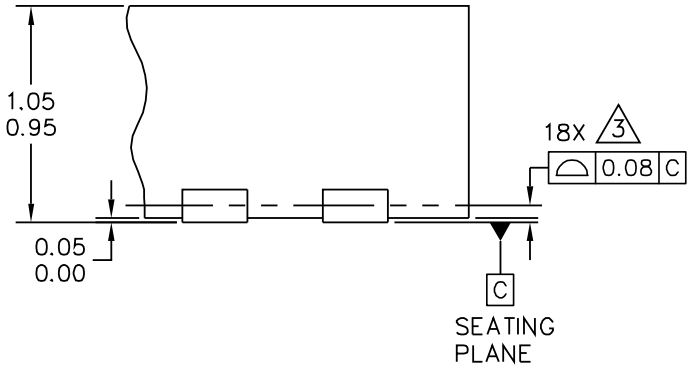


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	STANDARD: NON–JEDEC	
	SOT1679–1	11 JAN 2016

Figure 13. Case 2169-02, Issue X1, 12-Lead QFN—page 1

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DETAIL G
VIEW ROTATED 90° CW

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Figure 14. Case 2169-02, Issue X1, 12-Lead QFN—page 2

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. COPLANARITY APPLIES TO LEADS.
4. MIN. METAL GAP SHOULD BE 0.2 MM.
5. LEADS 13 TO 18 ARE NOT SOLDERABLE.

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Figure 15. Case 2169-02, Issue X1, 12-Lead QFN—page 3

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16 Revision history

Revision number	Revision date	Description
1.0	10/2012	• Initial release
2.0	11/2012	• Characterization data verified to be complete and final
2.1	4/2016	• Added MMA8491QR2 to Ordering information table • Added paragraphs describing absolute maximum ratings • Revised package dimensions drawings to the NXP format, no technical changes • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate

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Released on 26 April 2016