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AN350

Si4708/09 Antenna, Schematic, Layout, and Design Guidelines

1. Introduction

This document provides general Si4708/09 design guidelines and an FM antenna selection that includes schematic, BOM, and layout and design checklist. All users should follow the Si4708/09 design guidelines presented in Section 2 and headphone antenna design guidelines in Section 3. To get an in-depth knowledge about the headphone antenna, the antenna theory and interface model is presented in the Appendix.

2. Si4708/09 2.5 x 2.5 mm QFN Schematic and Layout

This section shows the minimal schematic and layout options required for optimal Si4708/09 performance. Population options are provided to support the layout for all 2.5 x 2.5 mm QFN devices, mitigate system noise, and filter VCO energy.

2.1. Si4708/09 2.5 x 2.5 mm Design

C1 (22 nF) is a required bypass capacitor for VD supply pin 10. Place C1 as close as possible to the VD pin 10 and GND pin 11. Place a VIA connecting C1 VD supply to the power rail such that the cap is closer to the Si4708/09 than the VIA. Route C1 GND directly and only to GND pin 11 with a wide, low inductance trace. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance, and return all currents to the GND pad.

C2 (22 nF) is an optional bypass capacitor for VA supply pin 14 and may be placed to mitigate supply noise. Place C2 as close as possible to the VA pin 14. Place a VIA connecting C2 VA supply to the power rail such that the cap is closer to the Si4708/09 than the VIA. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance, and return all currents to the GND pad.

C3 (100 nF) is an optional bypass capacitor for the VIO supply pin 8 and may be placed to mitigate supply noise. Place C3 as close as possible to the VIO pin 8 and the GND pin 11. Place a VIA connecting C3 VIO supply to the power rail such that the cap is closer to the Si4708/09 than the VIA. Route C3 GND directly and only to GND pin 11 with a wide, low inductance trace. These recommendations are made to reduce the size of the current loop created by the bypass cap and routing, minimize bypass cap impedance, and return all currents to the GND pad.

C4 (2–5 pF) is an optional filter capacitor for FMI pin 2 and may be placed to shunt VCO energy to GND and prevent it from radiating from an antenna connected to the FMI pin. This filter is only required if regulatory testing requires measuring emissions at the VCO frequency of 3 to 4 GHz and the antenna implementation is an efficient radiator at these frequencies. Place C4 as close as possible to FMI pin 2 and RFGND pin 3. Place a VIA connecting C4 FMI to another layer as needed such that the cap is closer to the Si4708/09 than the VIA.

C8 and C9 (0.39 µF) are ac coupling caps for receiver analog audio output from ROUT pin 12 and LOUT pin 13. The input resistance of an amplifier, such as a headphone amplifier, and the capacitor will set the high pass pole given by Equation 1. Placement location is not critical.

R1 (1 kΩ) *or* C5 (2-5 pF) are required for filtering when using GPO interrupts (polling not an issue). Place R1 on the opposite side of the PCB as the tuner (as close to pin 15 as possible) and route the GPO trace to the system controller on this layer. Alternatively, capacitor C5 (2-5 pF) may be placed as a filter capacitor also on the opposite side of the tuner and connected directly to ground.

R2-R6 (25 Ω–2 kΩ) are optional series termination resistors and are used to mitigate system noise. The recommended value of the resistors is 2 kΩ for optimal edge rate and noise suppression. Confirm that timing requirements are met with the selected series termination resistor value. Place the series termination resistors R2-R6 as close to the host controller as possible.

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R7 and R8 (4.7 kΩ) are optional pull-up resistors for the SCLK and SDIO lines required only when using an I^2C bus. The size of pull-up resistor value will vary based on the number of devices, capacitance, and speed of the bus. Placement location is not critical. Refer to the I^2C specification for additional design information.

$$f_c = \frac{1}{2\pi RC}$$

Equation 1. High-Pass Pole Calculation

2.2. Si4708/09 2.5 x 2.5 mm Schematic

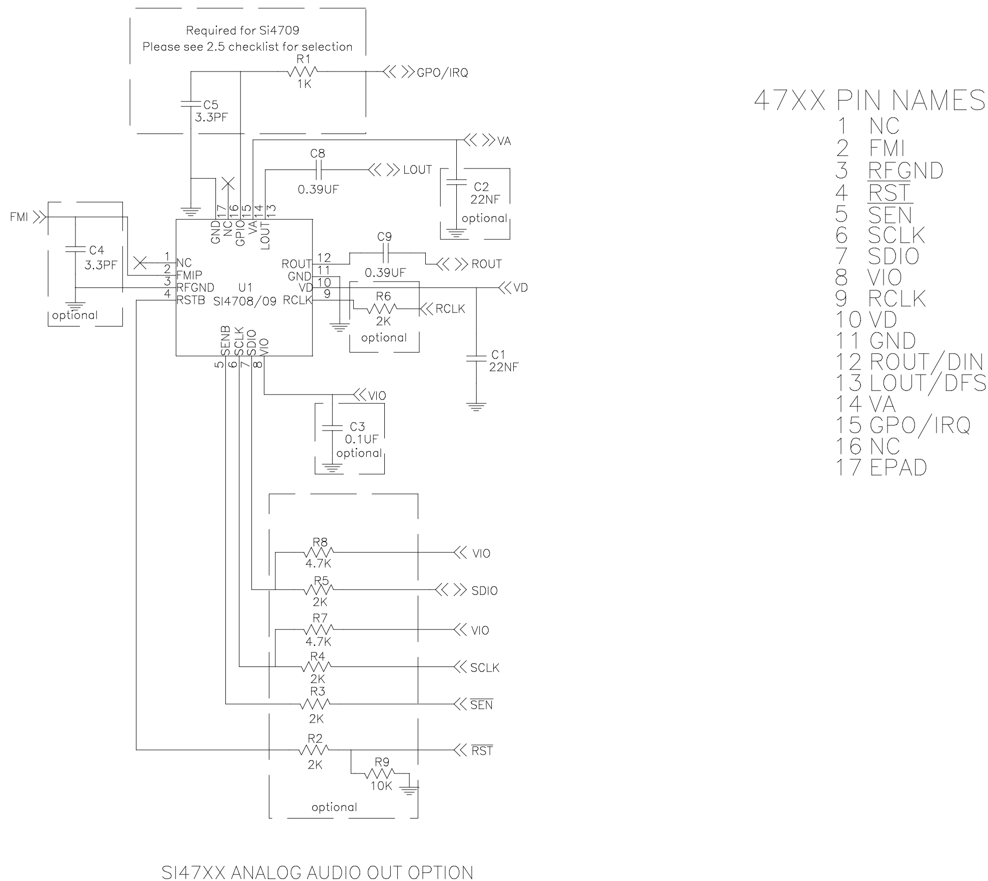

Figure 1. Si4708/09 2.5 x 2.5 mm QFN Schematic

2.3. Si4708/09 2.5 x 2.5 mm Bill of Materials

The required bill of materials for Figure 1 is shown in Table 1.

Table 1. Required Bill of Materials

Designator	Description	Note
C1	VD Supply bypass capacitor, 22 nF, 10%, Z5U/X7R	
U1	Silicon Laboratories Si4708/09, 2.5 x 2.5 mm, 16 pin, QFN	
R1	Series termination resistor, 1 kΩ	For noise mitigation (Si4709 only)

The optional bill of materials for Figure 1 is shown in Table 2.

Table 2. Optional Bill of Materials

Designator	Description	Note
C2	VA Supply bypass capacitor, 22 nF, 10%, Z5U/X7R	For supply noise mitigation
C3	VI0 Supply bypass capacitor, 100 nF, 10%, Z5U/X7R	For supply noise mitigation
C4	VCO filter capacitor, 3.3 pF, 0402, C0G, Venkel C0402COG2503R3JN	For filtering of VCO energy
C8, C9	AC coupling capacitor, 0.39 µF, X7R/X5R	For analog audio output
R2–R6	Series termination resistor, 2 kΩ	For system noise mitigation
R7, R8	Pullup resistor, 4.7 kΩ	For I^2C bus mode communication
R3	Pulldown resistor	
C5	GPO bypass capacitor, 3.3 pF	For noise mitigation (Si4709 only)

2.4. Si4708/09 2.5 x 2.5 mm Layout

The following layout rules are used:

- Layer 1 top side placement and routing (shown in Figure 2)
- Layer 2 bottom side placement and routing (shown in Figure 2)
- Power routed by trace (not shown)
- Ground routed by trace (not shown)
- 0402 component size or larger
- 6 mil traces
- 6 mil trace spacing
- 15 mil component spacing

Figure 2 shows critical component layout with top and bottom side placement, top and bottom side routing, and analog output support.

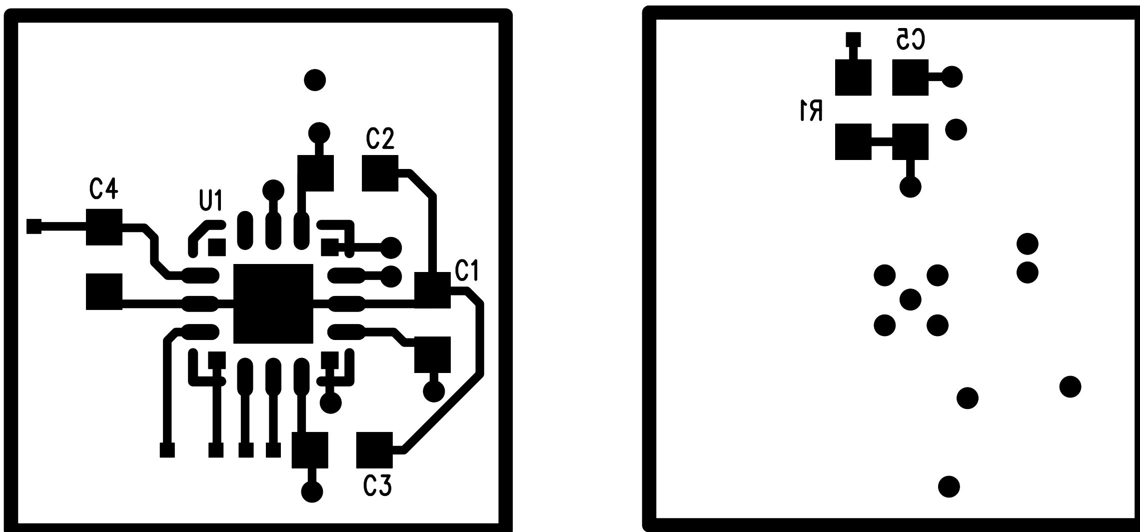

Figure 2. Top and Bottom Layer Example

Place a ground plane under the Si4708/09 as shown in Figure 3, "Two Layer Stackup" or Figure 4, "Four Layer Stackup". For designs in which a continuous ground plane is not possible, place a local ground plane directly under the Si4708/09. Do not route signal traces on the ground layer under the Si4708/09 and do not route signal traces under the Si4708/09 without a ground plane between the Si4708/09 and signal trace. Flood the primary and secondary layers with ground and place stitching VIAs to create a low impedance connection between planes.

Do not route digital or RF traces over breaks in the ground plane. Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small. In particular, care should be taken to avoid routing digital signals or reference clock traces near or parallel to the VCO pins 1, 16 or LOUT/ROUT pins 13, 12.

Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane using multiple VIAs to minimize ground potential differences.

Route power to the Si4708/09 by trace, ensuring that each trace is rated to handle the required current. Some trace impedance is preferable so that the decoupling currents are forced to flow through decoupling caps C1, C2, and C3 directly to the ground pins and not by alternate pathways.

Place the Si4708/09 close to the antenna(s) to minimize antenna trace length and capacitance and to minimize inductive and capacitive coupling. This recommendation must be followed for optimal device performance. Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling. Design, Place, and Route other circuits such that radiation in the band of interest is minimized.

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Figure 3. Two Layer Stackup

Figure 4. Four Layer Stackup

2.5. Si4708/09 2.5 x2.5 mm Design Checklist

The following design checklist summarizes the guidelines presented in this section:

- ☐ Place bypass caps C1, C2, and C3 as close as possible to the supply and ground pins.
- ☐ Place a VIA connecting C1, C2, and C3 to the power supplies such that the cap is between the Si4708/09 and the VIA.
- ☐ Route a wide, low inductance return current path from the C1, C2, and C3 to the Si4708/09 GND pins.
- ☐ Place C4 as close as possible to FMI pin 2 and RFGND pin 3.
- ☐ Place a VIA connecting C4 to FMI on another layer as needed such that the cap is between Si4708/09 and the VIA.
- ☐ Place the series termination resistors R2–R6, as close to the host controller as possible.
- ☐ Place a ground plane under the device as shown in Figure 3, “Two Layer Stackup” or Figure 4, “Four Layer Stackup”.
- ☐ Place a local ground plane directly under the device for designs in which a continuous ground plane is not possible.
- ☐ Required for Si4709: Place R1 *or* C5 on opposite side of the PCB as the Si4709 for noise suppression. Place the VIA as close to pin 15 as possible and route the GPO trace to the system controller on this layer.
- ☐ Route all traces to minimize inductive and capacitive coupling by keeping digital traces away from analog and RF traces, minimizing trace length, minimizing parallel trace runs, and keeping current loops small.
- ☐ Route all GND (including RFGND) pins to the ground pad. The ground pad should be connected to the ground plane by using multiple VIAs to minimize ground potential differences.
- ☐ Route power to the Si4708/09 by trace, ensuring that each trace is rated to handle the required current.
- ☐ Do not route signal traces on the ground layer directly under the Si4708/09.
- ☐ Do not route signal traces under the Si4708/09 without a ground plane between the Si4708/09 and signal trace.
- ☐ Do not route digital or RF traces over breaks in the ground plane.
- ☐ Do not route digital signals or reference clock traces near the VCO pin 1 and 16 or the LOUT/ROUT output pin 13 and 12.
- ☐ Do not route VCO pin 1 and 16 (NC). These pins must be left floating to guarantee proper operation.
- ☐ Flood the primary and secondary layers with ground and place stitching VIAs.
- ☐ Place the Si4708/09 close to the antenna(s) to minimize antenna trace length and capacitance and to minimize inductive and capacitive coupling. This recommendation must be followed for optimal device performance.
- ☐ Route the antenna trace over an unobstructed ground plane to minimize antenna loop area and inductive coupling.
- ☐ Design, place, and route other circuits such that radiation in the band of interest is minimized.

3. Headphone Antenna for FM Receive

Refer to"AN383: Si47xx Antenna, Schematic, Layout, and Design," Section 3.

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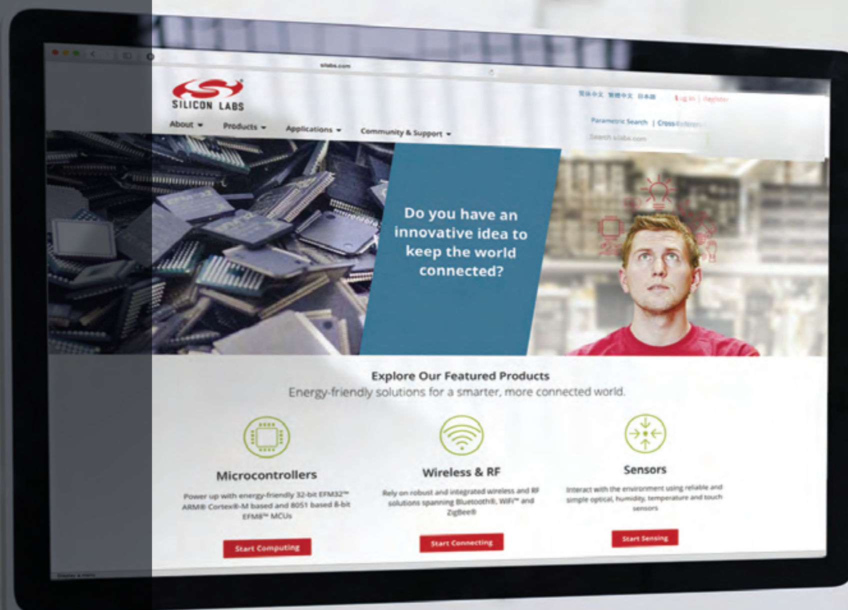
Appendix A—FM Receive Headphone Antenna Interface Model

Refer to"AN383: Si47xx Antenna, Schematic, Layout, and Design," Appendix A.



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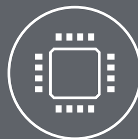

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