



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (16K x 4-BIT) with Output Control

IDT6198S
IDT6198L

FEATURES:

- High-speed (equal access and cycle times)
 - Military: 20/25/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- Output Enable ($\overline{OE}$) pin available for added system flexibility
- Low-power consumption
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin Cerdip, high-density 28-pin leadless chip carrier, and 24-pin SOJ
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CMOS. This state-of-the-art technology, combined with innovative circuit design tech-

niques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

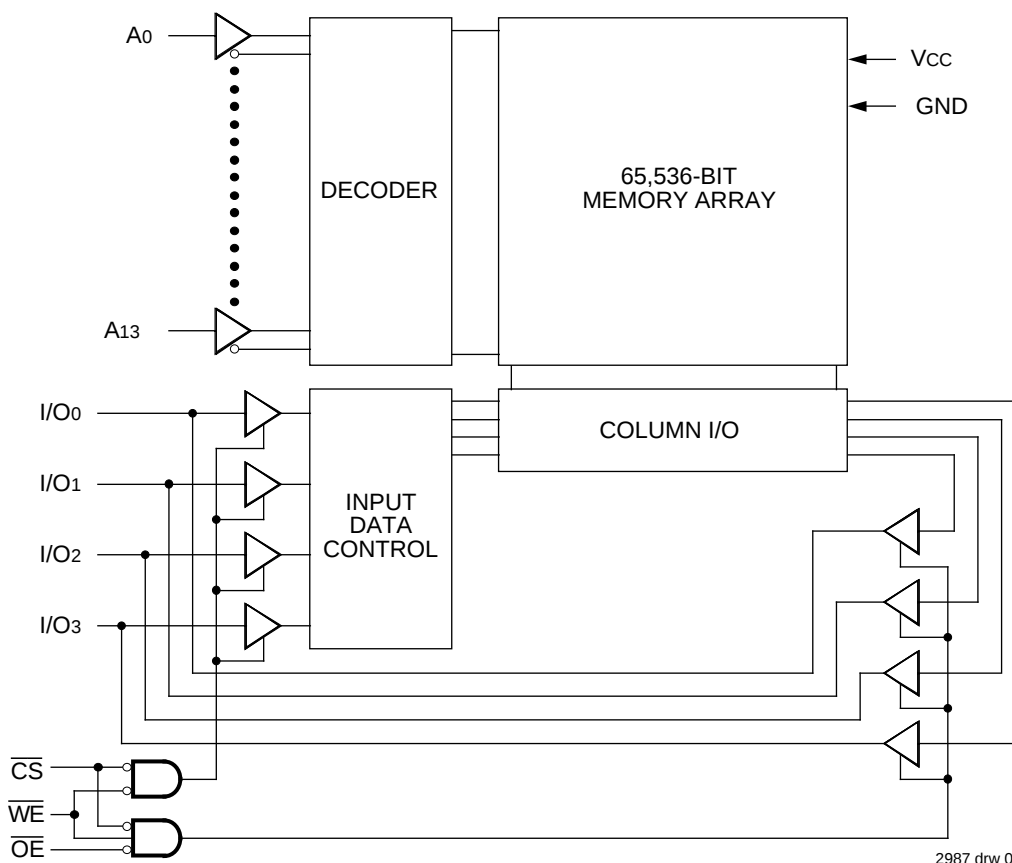
Access times as fast as 15ns are available. The IDT6198 offers a reduced power standby mode, ISB_1 , which is activated when $\overline{CS}$ goes HIGH. This capability significantly decreases system, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30 μ W when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply.

The IDT6198 is packaged in either a 24-pin 300 mil Cerdip, 28-pin leadless chip carrier or 24-pin J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



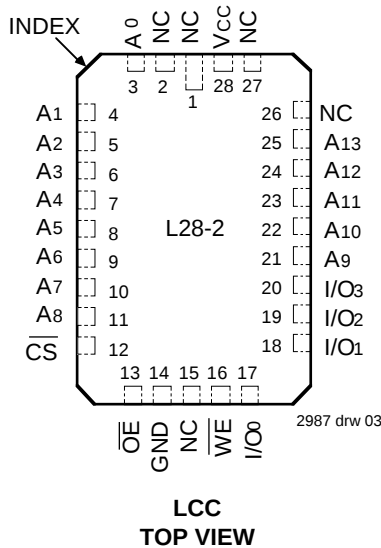
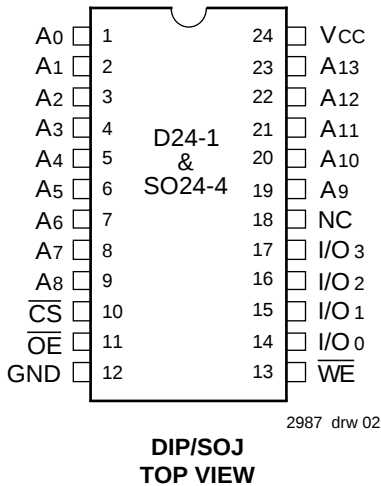
2987 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1994

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Name	Description
A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O0–I/O3	Data Input/Output
VCC	Power
GND	Ground

2987 tbl 01

TRUTH TABLE⁽¹⁾

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	H	L	DATAOUT	Active
Write	L	L	X	DATAIN	Active
Read	L	H	H	High-Z	Active

NOTE: 2987 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2987 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
CI/O	I/O Capacitance	VOUT = 0V	7	pF

NOTE: 2987 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

2987 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6198S		IDT6198L		Unit
				Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL. COM'L.	— —	10 5	— —	5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = GND to V _{CC}	MIL. COM'L.	— —	10 5	— —	5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min.			0.5	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.		—	0.4	—	0.4	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.		2.4	—	2.4	—	V

2987 tbl 07

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45 6198L45		6198S55/70/85 6198L55/70/85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC1}	Operating Power Supply Current $\overline{CS}$ = V _{IL} , Outputs Open V _{CC} = Max., f = 0 ⁽²⁾	S	100	—	100	105	100	105	100	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	
I _{CC2}	Dynamic Operating Current $\overline{CS}$ = V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	S	135	—	130	160	125	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
I _{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	60	—	55	70	50	60	45	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	35	—	35	—	35	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V _{HC} , V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽²⁾	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

2987 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

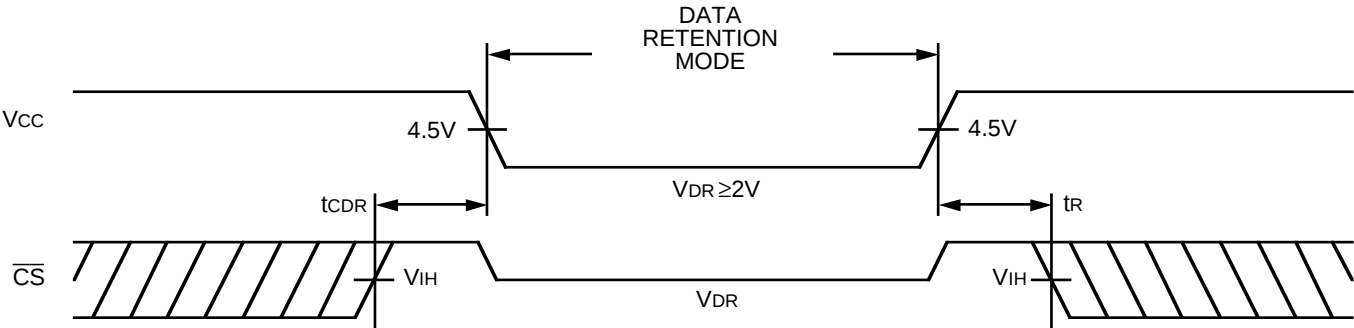
(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0v	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	MIL. COM'L.	— —	10 10	15 15	600 150	900 225	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

- NOTES:
- TA = +25°C.
 - t_{RC} = Read Cycle Time.
 - This parameter is guaranteed by device characterization but is not production tested.

2987 tbl 09

LOW V_{CC} DATA RETENTION WAVEFORM

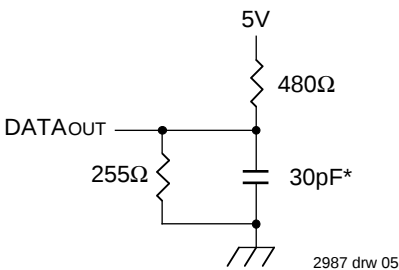


2987 drw 04

AC TEST CONDITIONS

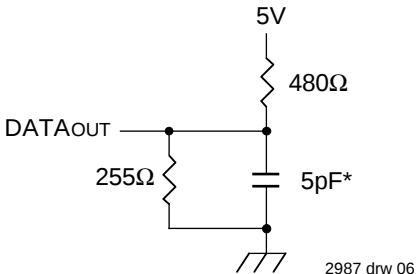
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2987 tbl 10



2987 drw 05

Figure 1. AC Test Load



2987 drw 06

Figure 2. AC Test Load
(for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ and tOW)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

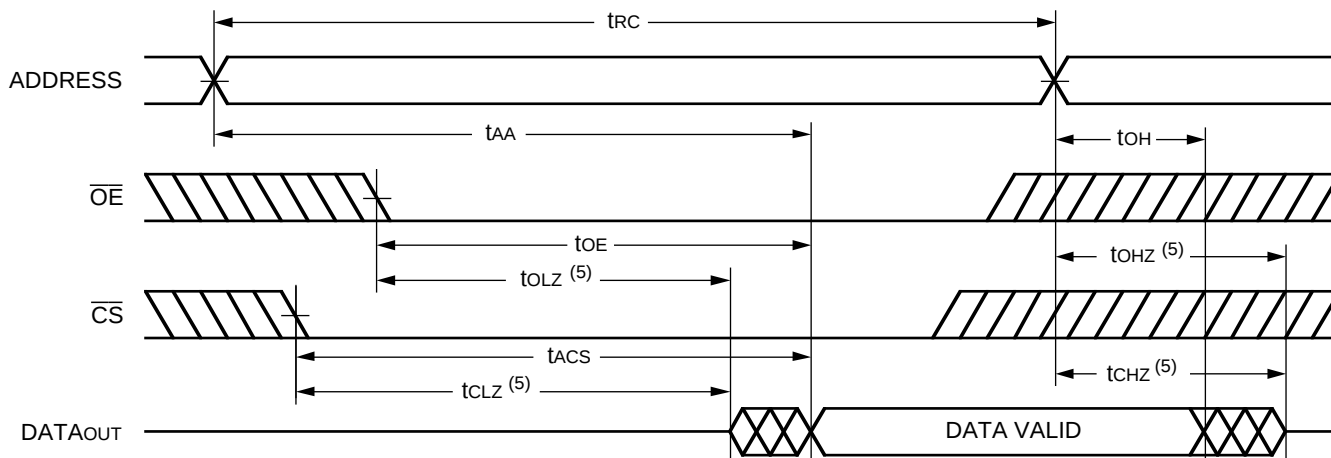
Symbol	Parameter	6198S15 ⁽¹⁾ 6198L15 ⁽¹⁾		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55 ⁽²⁾ 6198L45/55 ⁽²⁾		6198S70/85 ⁽²⁾ 6198L70/85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Read Cycle												
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ ⁽³⁾	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ ⁽³⁾	Output Enable to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ ⁽³⁾	Chip Select to Output in High-Z	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ ⁽³⁾	Output Disable to Output in High-Z	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU ⁽³⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD ⁽³⁾	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter is guaranteed by device characterization but is not production tested.

2987 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾

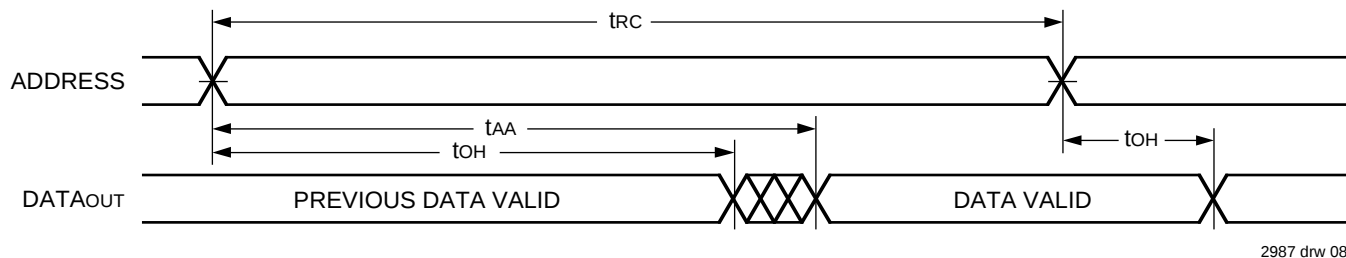


2987 drw 07

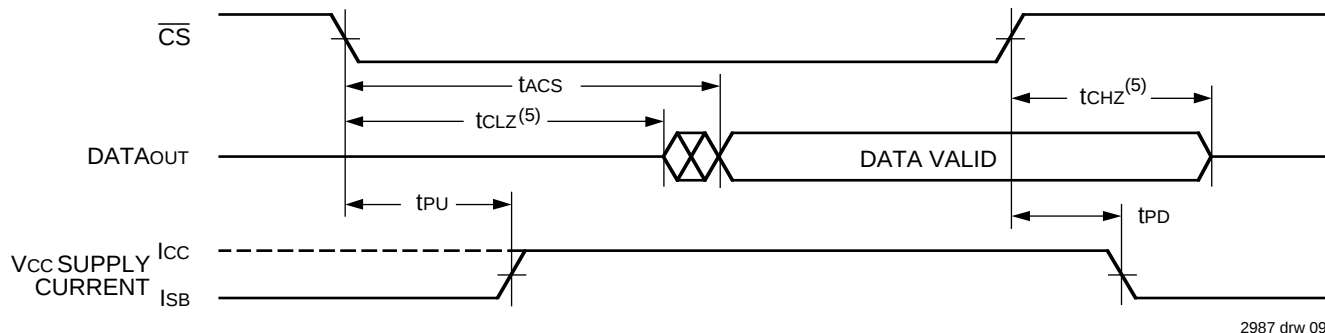
NOTES:

- $\overline{WE}$ is HIGH for Read cycle.
- Device is continuously selected, $\overline{CS}$ is LOW.
- Address valid prior to or coincident with $\overline{CS}$ transition LOW.
- $\overline{OE}$ is LOW.
- Transition is measured ±200mV from steady state voltage.

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



NOTES:

1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage.

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{V} \pm 10\%$, All Temperature Ranges)

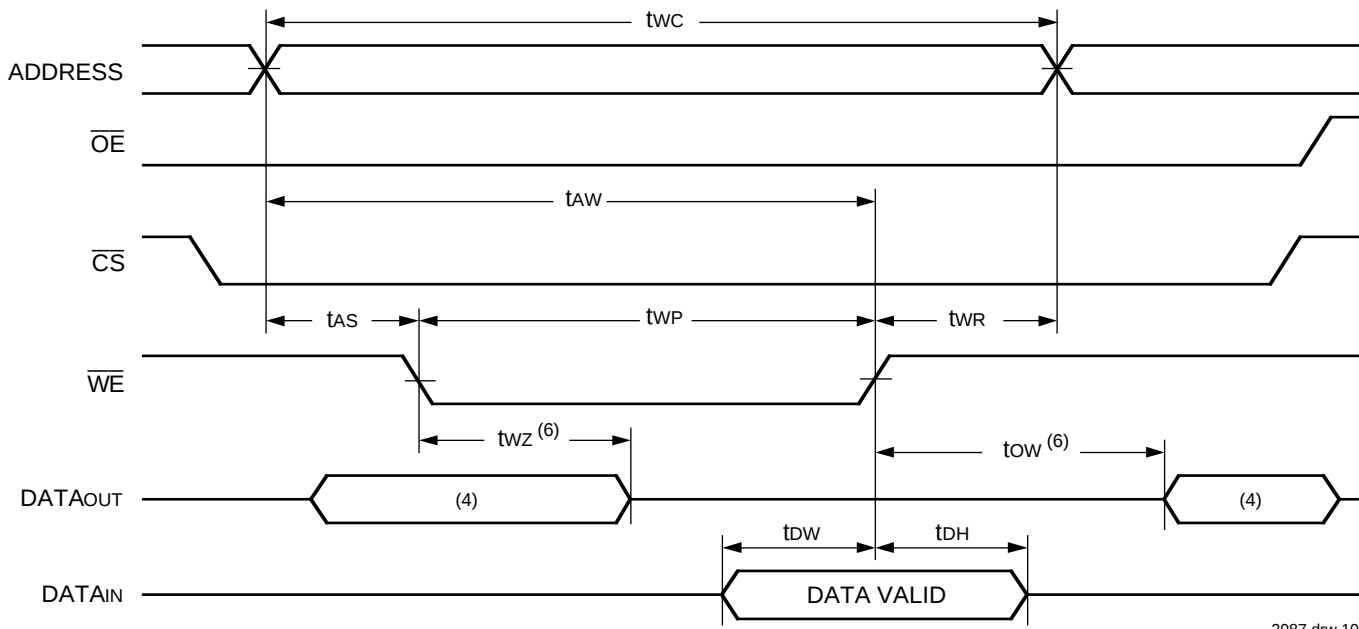
Symbol	Parameter	6198S15 ⁽¹⁾ 6198L15 ⁽¹⁾		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55 ⁽²⁾ 6198L45/55 ⁽²⁾		6198S70/85 ⁽²⁾ 6198L70/85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Write Cycle												
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tCW	Chip Select to End-of-Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAW	Address Valid to End-of-Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ ⁽³⁾	Write Enable to Output in High-Z	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tDW	Data Valid to End-of-Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW ⁽³⁾	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

1. 0° to $+70^\circ\text{C}$ temperature range only.
2. -55°C to $+125^\circ\text{C}$ temperature range only.
3. This parameter is guaranteed by device characterization, but is not production tested.

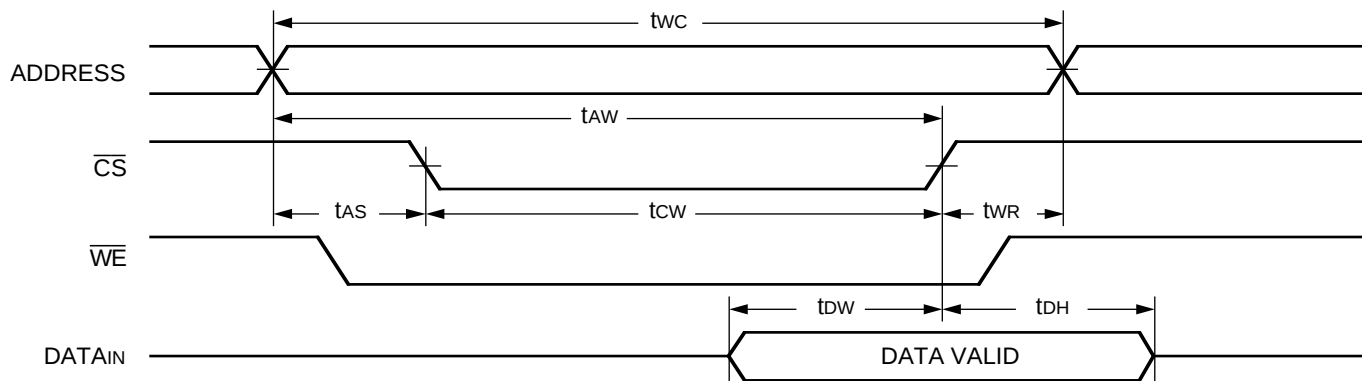
2987 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 3, 7)



2987 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2, 3)



2987 drw 11

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{wp}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{wr} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{wp} or ($t_{whz} + t_{dw}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{dw} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{wp} .

ORDERING INFORMATION

IDT6198	X	XX	X	X		
Device Type	Power	Speed	Package	Process/ Temperature Range		
					Blank	Commercial (0°C to +70°C)
					B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B
					D	300 mil CERDIP (D24-1)
					L	Leadless Chip Carrier (L28-2)
					Y	Small Outline IC J-Bend (SO24-4)
					15	Commercial Only } Speed in nanoseconds
					20	
					25	
					35	
					45	
					55	
					70	
					85	
					S	Standard Power
					L	Low Power

2987 drw 12