National Semiconductor

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LMH0346
3 Gbps HD/SD SDI Reclocker with Dual Differential Outputs

General Description

The LMH0346 3 Gbps HD/SD SDI Reclocker retimes serial digital video data conforming to the SMPTE 424M, SMPTE 292M, and SMPTE 259M (C) standards. The LMH0346 operates at serial data rates of 270 Mbps, 1.483 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps. The LMH0346 supports DVB-ASI operation at 270 Mbps.

The LMH0346 automatically detects the incoming data rate and adjusts itself to retime the incoming data to suppress accumulated jitter. The LMH0346 recovers the serial data-rate clock and optionally provides it as an output. The LMH0346 has two differential serial data outputs; the second output may be selected as a low-jitter, data-rate clock output. Controls and indicators are: serial clock or second serial data output select, manual rate select input, SD/HD rate indicator output, lock detect output, auto/manual data bypass and output mute. The serial data inputs, outputs, and serial clock outputs are differential LVPECL compatible. The CML serial data and serial clock outputs are suitable for driving 100Ω differentially terminated networks. The control logic inputs and outputs are LVCMOS compatible.

The LMH0346 is powered from a single 3.3V supply. Power dissipation is typically 370 mW.

The device is available in two space–saving packages: a 6.5 X 4.4 mm 20-pin e-TSSOP and an even more space–efficient 5 X 4 mm 24-pin LLP package.

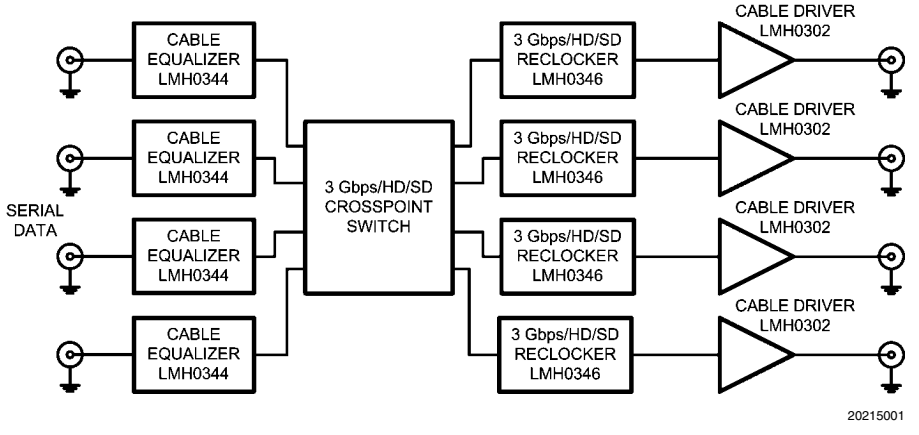
Features

- Supports SMPTE 424M, SMPTE 292M, and SMPTE 259M (C) serial digital video standards
- Supports 270 Mbps, 1.483 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps serial data rate operation
- Supports DVB-ASI at 270 Mbps
- Single 3.3V supply operation
- 370 mW typical power consumption
- Two differential, reclocked outputs
- Choice of second reclocked output or low-jitter, differential, data-rate clock output
- Single 27 MHz external crystal or reference clock input
- Manual or automatic rate select input
- SD/HD operating rate indicator output
- Lock Detect indicator output
- Output mute function for data and clock
- Auto/Manual reclocker bypass
- Differential LVPECL compatible serial data inputs and outputs
- LVCMOS control inputs and indicator outputs
- 20-pin e-TSSOP or 24-pin LLP package
- Industrial temperature range: -40°C to +85°C
- Footprint compatible with the LMH0046 andLMH0026 (e-TSSOP package)

Applications

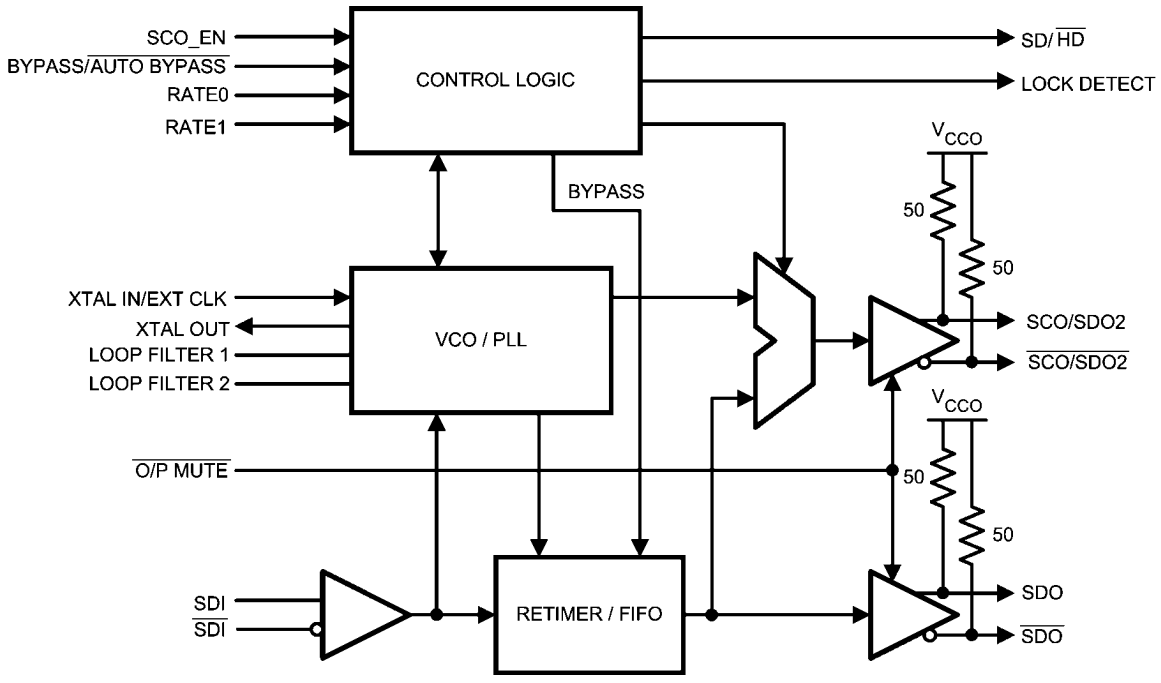
- SDTV/HDTV and 3 Gbps serial digital video interfaces for:
  - Digital video routers and switchers
  - Digital video processing and editing equipment
  - DVB-ASI equipment
  - Video standards and format converters

Typical Application



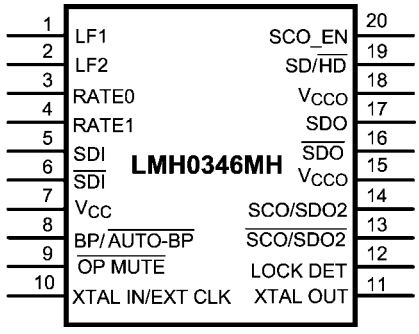
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Block Diagram



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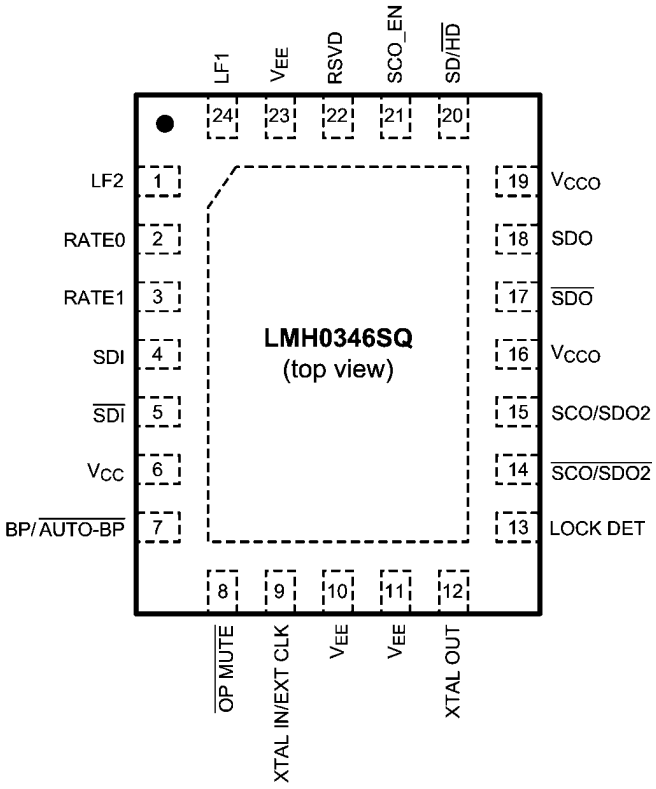
Connection Diagrams



20215002

The exposed die attach pad is the negative electrical terminal for this device. It must be connected to the negative power supply voltage.

20-Pin e-TSSOP
Order Number LMH0346MH
See NS Package Number MXA20A



20215006

The exposed die attach pad is the primary negative electrical terminal for this device. It must be connected to the negative power supply voltage.

24-Pin LLP
Order Number LMH0346SQ
See NS Package Number SQA24B

Pin Descriptions

e-TSSOP Pin	LLP Pin	Name	Description
1	24	LF1	Loop Filter.
2	1	LF2	Loop Filter.
3	2	RATE 0	Data Rate select input. This pin has an internal pulldown
4	3	RATE 1	Data Rate select input. This pin has an internal pulldown
5	4	SDI	Data Input True.
6	5	$\overline{\text{SDI}}$	Data Input Complement.
7	6	V_{CC}	Positive power supply.
8	7	BYPASS/$\overline{\text{AUTO BYPASS}}$	Bypass/Auto Bypass mode select. Bypasses reclocking when high. This pin has an internal pulldown.
9	8	OUTPUT $\overline{\text{MUTE}}$	Data and Clock Output Mute Input. Mutes the output when low. This pin has an internal pullup.
10	9	XTAL IN/EXT CLK	Crystal or External Oscillator Input.
11	12	XTAL OUT	Crystal Oscillator Output.
12	13	LOCK DETECT	PLL Lock Detect Output (active high).
13	14	$\overline{\text{SCO/SDO2}}$	Serial Clock or Serial Data Output 2 Complement.
14	15	SCO/SDO2	Serial Clock or Serial Data Output 2 True.
15	16	V_{CCO}	Positive power supply (Output Driver).
16	17	$\overline{\text{SDO}}$	Data Output Complement.
17	18	SDO	Data Output True.
18	19	V_{CCO}	Positive power supply (Output Driver).
19	20	SD/$\overline{\text{HD}}$	Data Rate Range Output. Output is high for SD and low for HD or 3G.
20	21	SCO_EN	Serial Clock or Serial Data 2 Output select. Sets second output to output the clock when high and the data when low. This pin has an internal pulldown.
—	10, 11, 23	V_{EE}	Negative power supply.
—	22	RSVD	Reserved for future use. Do not connect.
DAP	DAP	V_{EE}	Connect exposed DAP to negative power supply (ground).

Absolute Maximum Ratings (Note 1)

It is anticipated that this device will not be offered in a military qualified version. If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}–V_{EE})	4.0V
Logic Input Voltage (Vi)	V_{EE}–0.15V to V_{CC} +0.15V
Logic Input Current (single input):	
Vi = V_{EE}–0.15V	–5 mA
Vi = V_{CC}+0.15V	+5 mA
Logic Output Voltage (Vo)	V_{EE}–0.15V to V_{CC} +0.15V
Logic Output Source/Sink Current	±8 mA
Serial Data Input Voltage (V_{SDI})	V_{CC} to V_{CC}–2.0V
Serial Data Output Sink Current (I_{SDO})	24 mA
Package Thermal Resistance	
θ_{JA} 20-pin e-TSSOP	26.6°C/W
θ_{JA} 24-pin LLP	33.0°C/W
θ_{JC} 20-pin e-TSSOP	2.4°C/W
θ_{JC} 24-pin LLP	3.2°C/W
Storage Temp. Range	–65°C to +150°C
Junction Temperature	+125°C
Lead Temperature (Soldering 4 Sec)	+260°C (Pb-free)
ESD Rating (HBM)	8 kV
ESD Rating (MM)	400V
ESD Rating (CDM)	2 kV

Recommended Operating Conditions

Supply Voltage (V_{CC}–V_{EE})	3.3V ±5%
Logic Input Voltage	V_{EE} to V_{CC}
Differential Serial Input Voltage	800 mV ±10%
Serial Data or Clock Output Sink Current (I_{SO})	16 mA max.
Operating Free Air Temperature (T_A)	–40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic inputs	2		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
I_{IH}	Input Current High Level	$V_{IH} = V_{CC}$			47	65	µA
I_{IL}	Input Current Low Level	$V_{IL} = V_{EE}$			–18	–25	µA
V_{OH}	Output Voltage High Level	I_{OH} = –2 mA	Logic outputs	2			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				V_{EE} + 0.6	V
V_{SDID}	Serial Input Voltage, Differential	(Note 8)	SDI	200		1600	mV_{P-P}
V_{CMI}	Input Common Mode Voltage	V_{SDID} = 200 mV, (Note 8)		V_{EE}+1.2		V_{CC}–0.2	V
V_{SDOD}	Serial Data Output Voltage, Differential	100Ω differential load	SDO	620	750	880	mV_{P-P}
V_{SCOD}	Serial Clock Output Voltage, Differential	100Ω differential load, 2970 Mbps, (Note 8)	SCO	400	525	650	mV_{P-P}
V_{CMO}	Output Common Mode Voltage	100Ω differential load	SDO, SCO		V_{CC}– V_{SDOD}		V
I_{CC}	Supply Current	2970 Mbps			111	126	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SD}	Serial Data Rate	SMPTE 259M, C	SDI, SDO		270		Mbps
BR_{SD}	Serial Data Rate	SMPTE 292M			1483, 1485		Mbps
BR_{SD}	Serial Data Rate	SMPTE 424M			2967, 2970		Mbps
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (Notes 7, 8, 9)	SDI	>6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	270 Mbps, (Notes 7, 8, 10)		>0.6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	1483 or 1485 Mbps, (Notes 7, 8, 9)		>6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	1483 or 1485 Mbps, (Notes 7, 8, 10)		>0.6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	2967 or 2970 Mbps, (Notes 7, 8, 9)		>6			UI_{P-P}
TOL_{JIT}	Serial Input Jitter Tolerance	2967 or 2970 Mbps, (Notes 7, 8, 10)		>0.6			UI_{P-P}
t_{JIT}	Serial Data Output Jitter	270 Mbps, (Notes 8, 11)	SDO		0.01	0.03	UI_{P-P}
t_{JIT}	Serial Data Output Jitter	1483 or 1485 Mbps, (Notes 8, 12)			0.03	0.04	UI_{P-P}
t_{JIT}	Serial Data Output Jitter	2967 or 2970 Mbps, (Notes 8, 13)			0.06	0.08	UI_{P-P}
BW_{LOOP}	Loop Bandwidth	270 Mbps, <0.1dB Peaking			275		kHz
		1485 Mbps, <0.1dB Peaking			1.5		MHz
		2970 Mbps, <0.1dB Peaking			2.75		MHz
F_{CO}	Serial Clock Output Frequency	270 Mbps data rate	SCO		270		MHz
F_{CO}	Serial Clock Output Frequency	1483 Mbps data rate			1483		MHz
F_{CO}	Serial Clock Output Frequency	1485 Mbps data rate			1485		MHz
F_{CO}	Serial Clock Output Frequency	2967 Mbps data rate			2967		MHz
F_{CO}	Serial Clock Output Frequency	2970 Mbps data rate			2970		MHz
t_{JIT}	Serial Clock Output Jitter				2	3	ps_{RMS}
	Serial Clock Output Alignment with respect to Data Interval	(Note 8)	SDO, SCO	40		60	%
	Serial Clock Output Duty Cycle	(Note 8)	SCO	45		55	%
T_{ACQ}	Acquisition Time	(Note 6)				15	ms
t_r, t_f	Input rise/fall time	10%–90%	Logic inputs		1.5		ns

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
t_r, t_f	Input rise/fall time	20%–80%, 270 Mbps, (Note 4)	SDI			1500	ps
t_r, t_f	Input rise/fall time	20%–80%, 1483 or 1485 Mbps, (Note 4)				270	ps
t_r, t_f	Input rise/fall time	20%–80%, 2967 or 2970 Mbps, (Note 4)				135	ps
t_r, t_f	Output rise/fall time	10%–90%	Logic outputs		1.5		ns
t_r, t_f	Output rise/fall time	20%–80%, (Notes 5, 8)	SDO, SCO		90	130	ps
F_{REF}	Reference Clock Frequency				27		MHz
F_{TOL}	Reference Clock Frequency Tolerance				±50		ppm

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are referenced to V_{EE} (equal to zero volts).

Note 3: Typical values are stated for: V_{CC} = +3.3V, T_A = +25°C.

Note 4: This specification is guaranteed by design.

Note 5: R_L = 100Ω differential.

Note 6: Measured from first SDI transition until Lock Detect (LD) output goes high (true).

Note 7: Peak-to-peak amplitude with sinusoidal modulation per SMPTE RP 184-1996 paragraph 4.1. The test data signal shall be color bars.

Note 8: This parameter is guaranteed by characterization over voltage and temperature limits.

Note 9: Refer to "A1" in Figure 1 of SMPTE RP 184-1996.

Note 10: Refer to "A2" in Figure 1 of SMPTE RP 184-1996.

Note 11: PRBS 2^{10}–1, input jitter = 31 ps_{P-P}

Note 12: PRBS 2^{10}–1, input jitter = 24 ps_{P-P}

Note 13: PRBS 2^{10}–1, input jitter = 22 ps_{P-P}

Device Description

The LMH0346 3 Gbps HD/SD SDI Reclocker is used in many types of digital video signal processing equipment. Supported serial digital video standards are SMPTE 259M (C), SMPTE 292M, and SMPTE 424M. Corresponding serial data rates are 270 Mbps, 1.483 Gbps, 1.485 Gbps, 2.967 Gbps, and 2.97 Gbps. DVB-ASI data at 270 Mbps may also be retimed. The LMH0346 retimes the serial data stream to suppress accumulated jitter. It provides two low-jitter, differential, serial data outputs. The second output may be selected to output either serial data or a low-jitter serial data-rate clock. Controls and indicators are: serial clock or second serial data output select, manual rate select input, SD/HD rate output, lock detect output, auto/manual data bypass and output mute.

Serial data inputs are CML and LVPECL compatible. Serial data and clock outputs are differential CML and produce LVPECL compatible levels. The output buffer design can drive AC or DC-coupled, terminated 100Ω differential loads. The differential output level is 750 mV_{P-P} into 100Ω AC or DC-coupled differential loads. Logic inputs and outputs are LVCMOS compatible.

The device package is a 20-pin e-TSSOP or a 24-pin LLP. Both package options have an exposed die attach pad. The exposed die attach pad is electrically connected to device ground (V_{EE}) and is the negative electrical terminal for the device. This terminal must be connected to the negative power supply or circuit ground.

Serial Data Inputs, Serial Data and Clock Outputs

SERIAL DATA INPUT AND OUTPUTS

The differential serial data input, SDI, accepts serial digital video data at the rates specified in *Table 1*. The serial data input is differential LVPECL compatible. The input is intended to be DC interfaced to devices such as the LMH0344 adaptive cable equalizer. The input is not internally terminated or biased. The input may be AC-coupled if a suitable input bias voltage is provided. *Figure 1* shows the equivalent input circuit for SDI and $\overline{\text{SDI}}$.

The LMH0346 has two, retimed, differential, serial data outputs, SDO and SCO/SDO2. These outputs provide low jitter, differential, retimed data to devices such as the LMH0302 cable driver. Output SCO/SDO2 is multiplexed and can provide either a second serial data output or a serial clock output. *Figure 2* shows the equivalent output circuit for SDO, $\overline{\text{SDO}}$, SCO/SDO2, and $\overline{\text{SCO/SDO2}}$.

The SCO_EN input controls the operating mode for the SCO/SDO2 output. When the SCO_EN input is high the SCO/SDO2 output provides a serial clock. When SCO_EN is low, the SCO/SDO2 output provides retimed serial data.

Both differential serial data outputs, SDO and SCO/SDO2, are muted when the OUTPUT $\overline{\text{MUTE}}$ input is a logic low level. SCO/SDO2 also mutes when the Bypass mode is activated and this output is operating as the serial clock output (SCO_EN input is high). When muted, SDO and $\overline{\text{SDO}}$ (or SDO2 and $\overline{\text{SDO2}}$) will assume opposite differential output levels. The CML serial data outputs are differential LVPECL compatible. These outputs have internal 50Ω pull-ups and are suitable for driving AC or DC-coupled, 100Ω center-tapped, AC grounded or 100Ω un-center-tapped, differentially terminated networks.

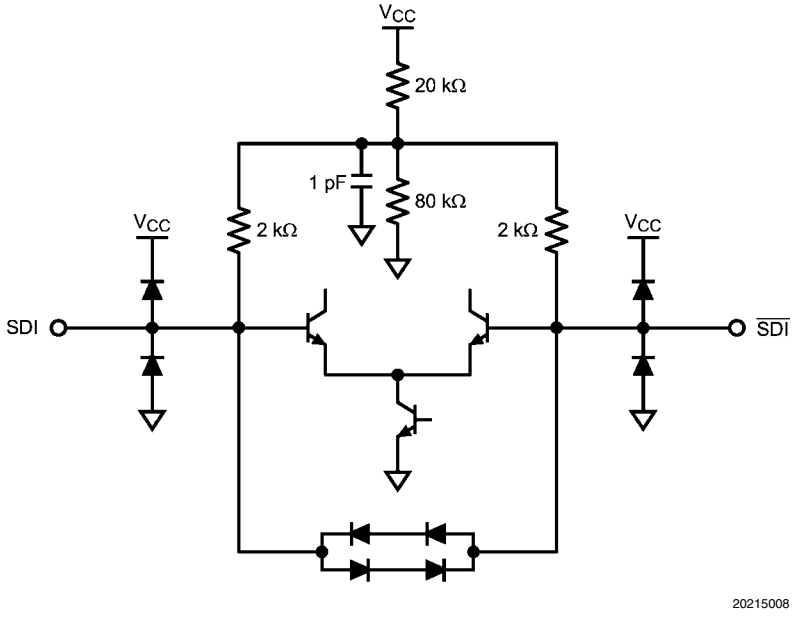


FIGURE 1. Equivalent SDI Input Circuit (SDI, $\overline{\text{SDI}}$)

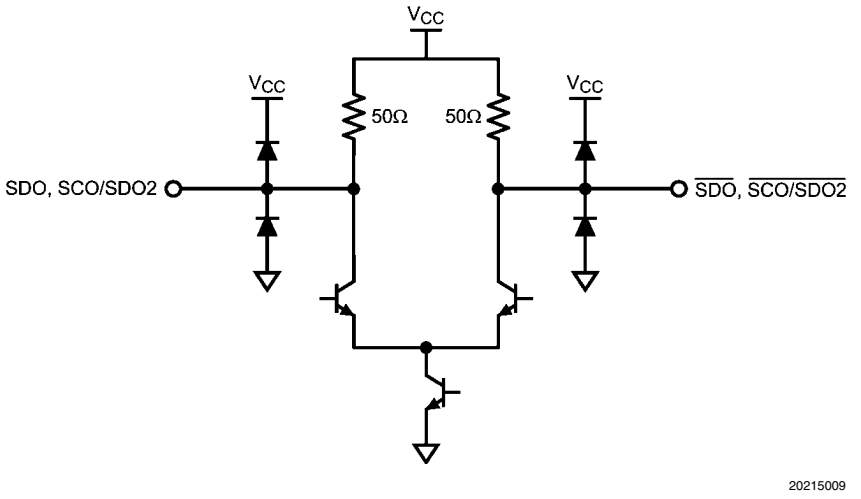


FIGURE 2. Equivalent SDO Output Circuit (SDO, SDO, SCO/SDO2, SCO/SDO2)

OPERATING SERIAL DATA RATES

This device operates at serial data rates of 270 Mbps, 1483 Mbps, 1485 Mbps, 2967 Mbps, and 2970 Mbps. The device does not lock to harmonics of these rates. The device does not lock and automatically enters the reclocker bypass mode for the following data rates: 143 Mbps, 177 Mbps, 360 Mbps, and 540 Mbps.

SERIAL DATA CLOCK/SERIAL DATA 2 OUTPUT

The Serial Data Clock/Serial Data 2 Output is controlled by the SCO_EN input and provides either a second retimed serial data output or a low jitter differential clock output appropriate to the serial data rate being processed. When operating as a serial clock output, the rising edge of the clock will be positioned within the corresponding serial data bit interval within 10% of the center of the data interval.

Differential output SCO/SDO2 functions as the second serial data output when the SCO_EN input is a logic-low level. This output functions as the serial clock output when the SCO_EN input is a logic-high level. The SCO_EN input has an internal pull-down device and the default state of SCO_EN is low (serial data output 2 enabled). SCO/SDO2 is muted when the OUTPUT MUTE input is a logic low level. When the Bypass mode is activated and this output is functioning as a serial clock output (SCO_EN is high), the output will also be muted. If an unsupported data rate is used while in Auto Bypass mode with this output functioning as a serial clock output, the output is invalid.

Control Inputs and Indicator Outputs

SERIAL DATA RATE SELECTOR

The Serial Data Rate Selector (RATE [1:0]) permits the user to fix the operating serial data rate. The pins have internal pull-downs which maintain a logic-low input condition unless externally driven to a logic-high condition. This input also serves to place the device in a test mode. The codes shown in *Table 1* select the desired operating serial data rate. The LMH0346 then enters either the Auto-Rate Detect mode or a single operating rate. Selecting the 270 Mbps rate mode may also be used when reclocking DVB-ASI data. DVB-ASI data is MPEG2 coded data that is transmitted in 8B10B coding. The device will reclock this data without harmonic locking. Auto-Rate Detect mode may be used for any supported data rate, including DVB-ASI.

TABLE 1. Data Rate Select Input Codes

Rate [1:0] Code	Data Rate or Mode	Comments
00	Auto-Rate Detect mode	
01	270 Mbps	May be used to support DVB-ASI operation
10	1483/1485 Mbps, 2967/2970 Mbps	

LOCK DETECT

The Lock Detect (LD) output, when high, indicates that data is being received and the PLL is locked. LD may be connected to the OUTPUT MUTE input to mute the data and clock outputs when no data signal is being received. Note that when the Bypass/Auto Bypass input is set high, Lock Detect will remain low. See *Table 2*.

OUTPUT MUTE

The OUTPUT MUTE input, when low, mutes the serial data and clock outputs. It may be connected to Lock Detect or externally driven to mute or un-mute the outputs. If OUTPUT MUTE is connected to LD, then the data and clock outputs are muted when the PLL is not locked. This function overrides the Bypass function: see *Table 2*. OUTPUT MUTE has an internal pull-up device to enable the output by default.

BYPASS/AUTO BYPASS

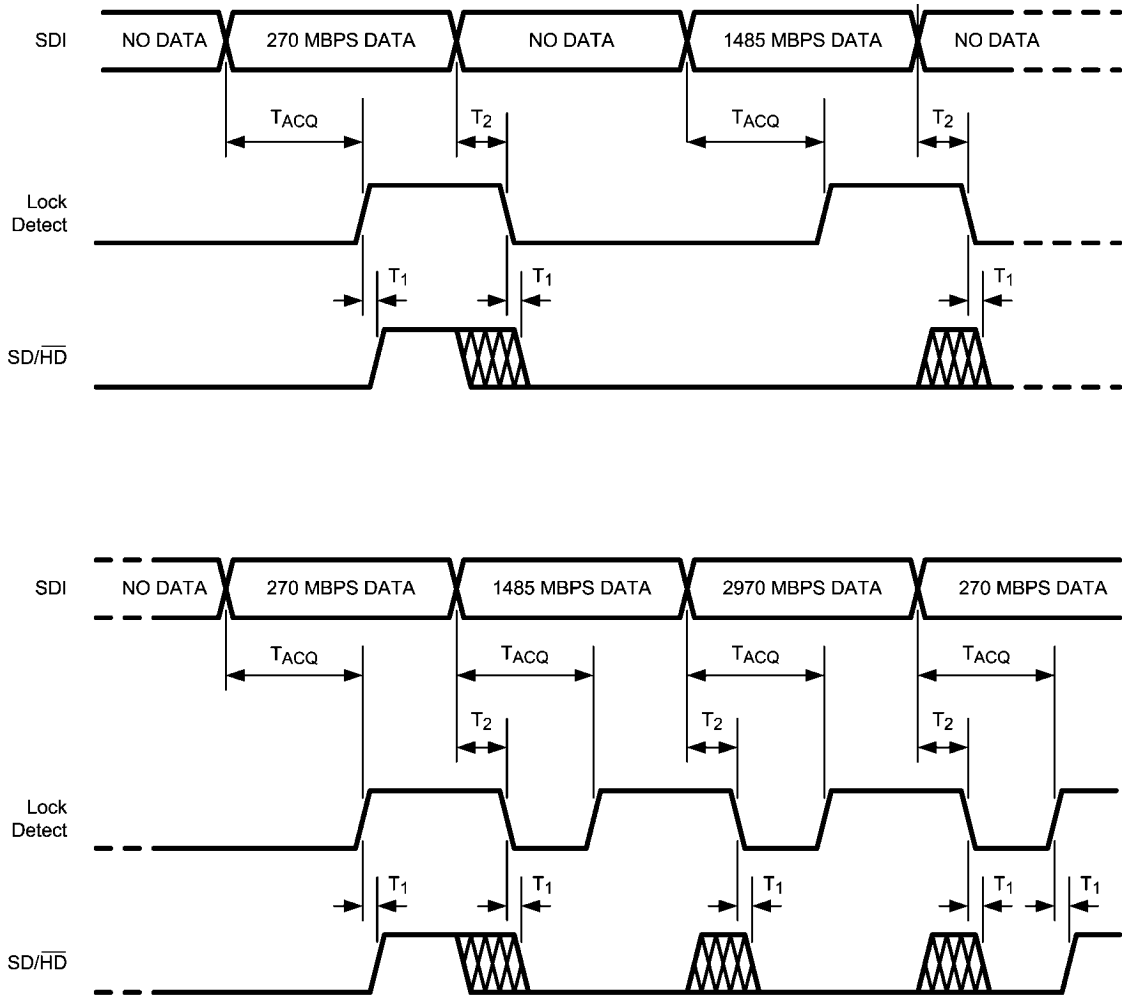
The Bypass/Auto Bypass input, when high, forces the device to output the data without reclocking it. When this input is low, the device automatically bypasses the reclocking function when the device is in an unlocked condition or the detected data rate is a rate which the device does not support. Note that when the Bypass/Auto Bypass input is set high, Lock Detect will remain low. See *Table 2*. BYPASS/AUTO BYPASS has an internal pull-down device.

TABLE 2. Control Functionality

LOCK DETECT	OUTPUT $\overline{\text{MUTE}}$	BYPASS/$\overline{\text{AUTO BYPASS}}$	DEVICE STATUS
0	1	X	PLL unlocked, reclocker bypassed
1	1	0	PLL locked to supported data rate, reclocker not bypassed
X	0	X	Outputs muted
0	LOCK DETECT	X	Outputs muted
1	LOCK DETECT	0	PLL locked to supported data rate, reclocker not bypassed

SD/$\overline{\text{HD}}$

The SD/$\overline{\text{HD}}$ output indicates whether the LMH0346 is processing SD or HD / 3 Gbps data rates. It may be used to control another device such as the LMH0302 cable driver. When this output is high it indicates that the data rate is 270 Mbps. When low, the indicated data rate is 1483, 1485, 2967, or 2970 Mbps. The SD/$\overline{\text{HD}}$ output is a registered function and is only valid when the PLL is locked and the Lock Detect output is high. When the PLL is not locked (the Lock Detect output is low), the SD/$\overline{\text{HD}}$ output defaults to HD (low). The SD/$\overline{\text{HD}}$ output is undefined for a short time after lock detect assertion or deassertion due to a data rate change on SDI. See *Figure 3* for a timing diagram showing the relationship between SDI, Lock Detect, and SD/$\overline{\text{HD}}$.



T_{ACQ} = Acquisition Time, defined in the AC Electrical Characteristics Table

T_1 = Time from Lock Detect assertion or deassertion until SD/$\overline{\text{HD}}$ output is valid, typically 37 ns (one 27 MHz clock period)

T_2 = Time from SDI input change until Lock Detect de-assertion, 1 ms maximum. SD/$\overline{\text{HD}}$ output is not valid during this time.

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FIGURE 3. SDI, Lock Detect, and SD/$\overline{\text{HD}}$ Timing

SCO_EN

Input SCO_EN enables the SCO/SDO2 differential output to function either as a serial clock or second serial data output. SCO/SDO2 functions as a serial clock when SCO_EN is high. This pin has an internal pull-down device. The default state (low) enables the SCO/SDO2 output as a second serial data output.

CRYSTAL OR EXTERNAL CLOCK REFERENCE

The LMH0346 uses a 27 MHz crystal or external clock signal as a timing reference input. A 27 MHz parallel resonant crystal and load network may be connected to the XTAL IN/EXT CLK and XTAL OUT pins. Alternatively, a 27 MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK. Parameters for a suitable crystal are given in *Table 3*.

TABLE 3. Crystal Parameters

Parameter	Value
Frequency	27 MHz
Frequency Stability	±50 ppm @ recommended drive level
Operating Mode	Fundamental mode, Parallel Resonant
Load Capacitance	18–20 pF
Shunt Capacitance	7 pF
Series Resistance	40Ω max.
Recommended Drive Level	100 µW
Maximum Drive Level	500 µW
Operating Temperature Range	−10°C to +60°C

Application Information

Figure 4 shows an application circuit for the LMH0346 along with the LMH0344 3 Gbps HD/SD SDI Adaptive Cable Equalizer and LMH0302 3 Gbps HD/SD SDI Cable Driver.

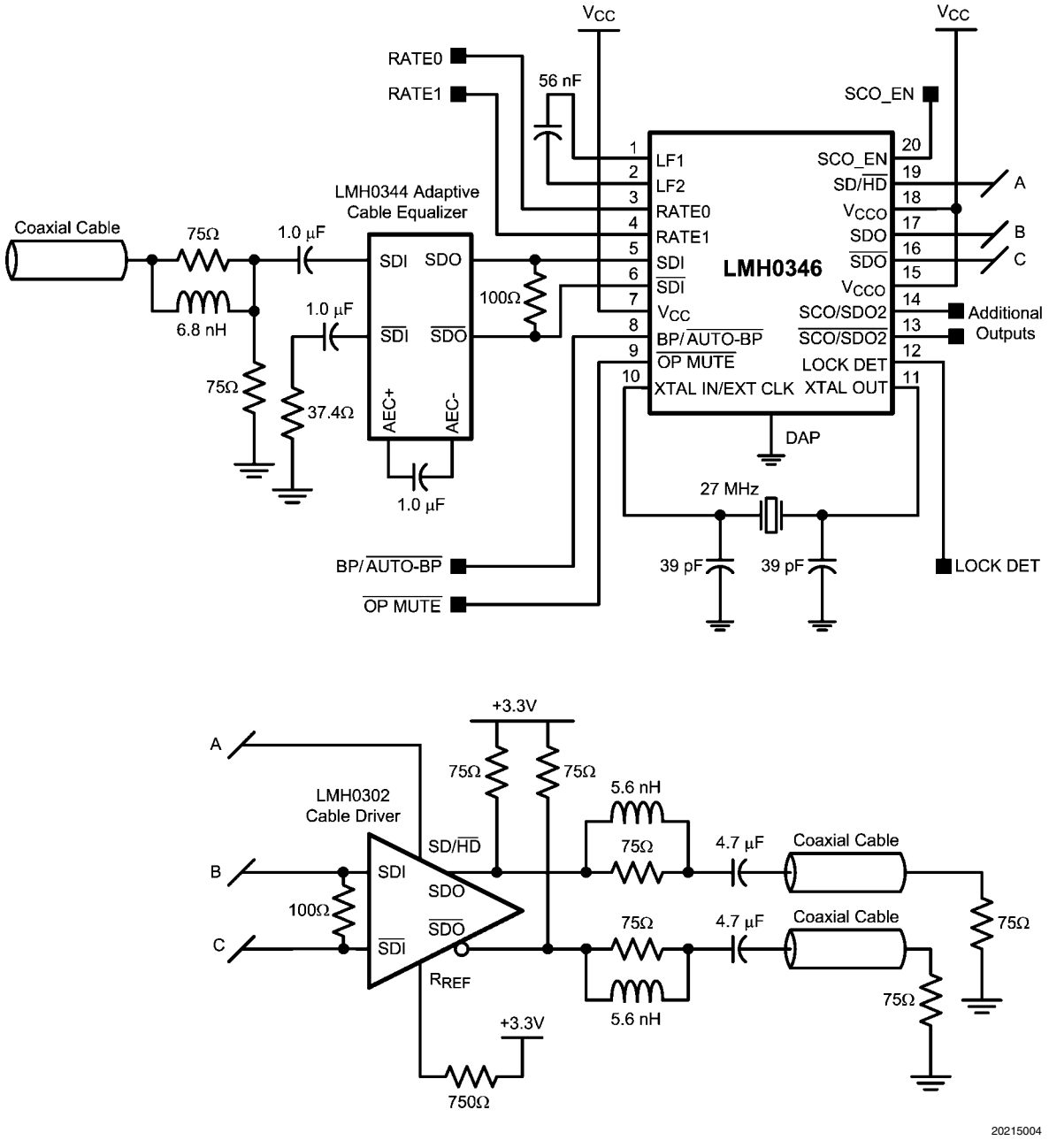


FIGURE 4. Application Circuit

The LMH0346 inputs are LVPECL compatible. The LMH0346 has a wide input common mode range and in most cases the input should be DC coupled. For DC coupling, the inputs must be kept within the common mode range specified in *DC Electrical Characteristics*. *Figure 4* shows an example of a DC coupled interface between the LMH0344 cable equalizer and the LMH0346. The LMH0344 output common mode voltage and voltage swing are within the range of the input common mode voltage and voltage swing of the LMH0346. All that is required is a 100Ω differential termination as shown. The resistor should be placed as close to the LMH0346 input as possible. If desired, this network may be terminated with two 50Ω resisters and a center tap capacitor to ground in place of the single 100Ω resistor.

The LMH0346 outputs are LVPECL compatible. SDO is the primary data output and SCO/SDO2 is a second output that may be set as the serial clock or a second data output. Both outputs are always active. The LMH0346 output should be

DC coupled to the input of the receiving device as long as the common mode ranges of both devices are compatible. *Figure 4* shows an example of a DC coupled interface between the LMH0346 and LMH0302 cable driver. All that is required is a 100Ω differential termination as shown. The resistor should be placed as close to the LMH0302 input as possible. If desired, this network may be terminated with two 50Ω resisters and a center tap capacitor to ground in place of the single 100Ω resistor.

The external loop filter capacitor (between LF1 and LF2) should be 56 nF. This is the only supported value; the loop filter capacitor should not be changed.

RATE0 and RATE1 have internal pulldowns to select Auto-Rate Detect mode by default. These pins may also be used to set the device to SD mode or HD/3G mode.

BYPASS/$\overline{\text{AUTO BYPASS}}$ has an internal pulldown to enable Auto Bypass mode by default. This pin may be pulled high to force the LMH0346 to bypass all data.

OUTPUT $\overline{\text{MUTE}}$ has an internal pullup to enable the outputs by default. This pin may be pulled low to mute the outputs.

The XTAL IN/EXT CLK and XTAL OUT pins are shown with a 27 MHz crystal and the proper loading. The crystal should match the parameters described in *Table 3*. Alternately, a 27MHz LVCMOS compatible clock signal may be input to XTAL IN/EXT CLK.

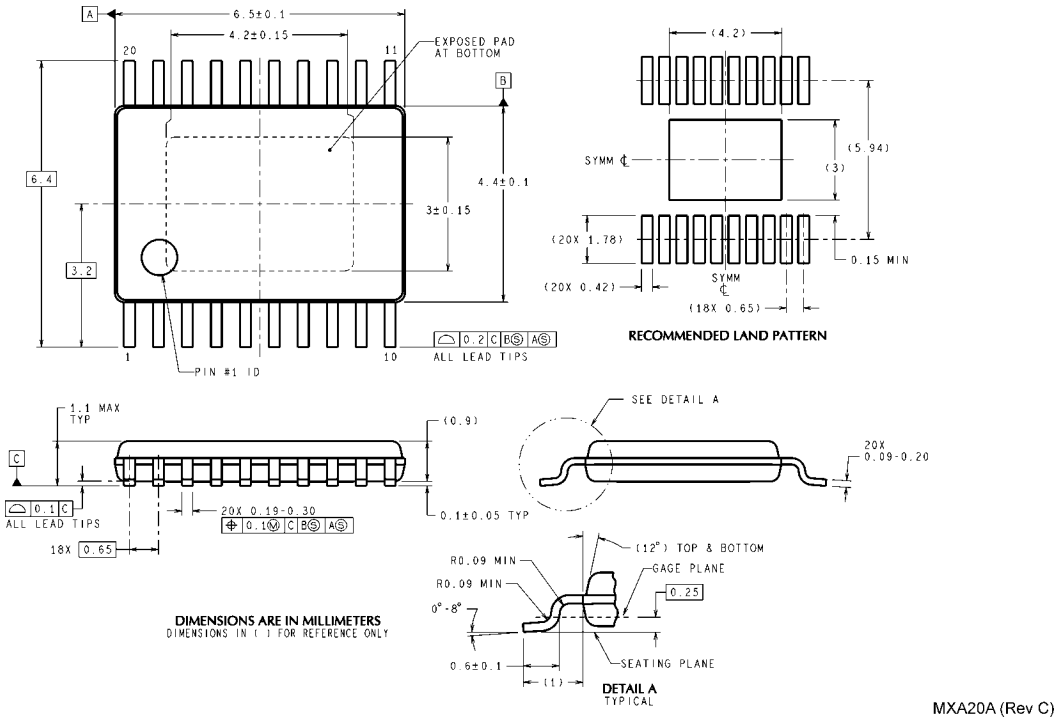
The active high LOCK DETECT output provides an indication that proper data is being received and the PLL is locked.

The SD/$\overline{\text{HD}}$ output may be used to drive the SD/$\overline{\text{HD}}$ pin of an SDI cable driver (such as the LMH0302) in order to properly set the cable driver's edge rate for SMPTE compliance. It defaults to HD/3G (low) when the LMH0346 is not locked.

SCO_EN has an internal pulldown to set the second output (SCO/SDO2) to output data. This pin may be pulled high to set the second output as a serial clock.

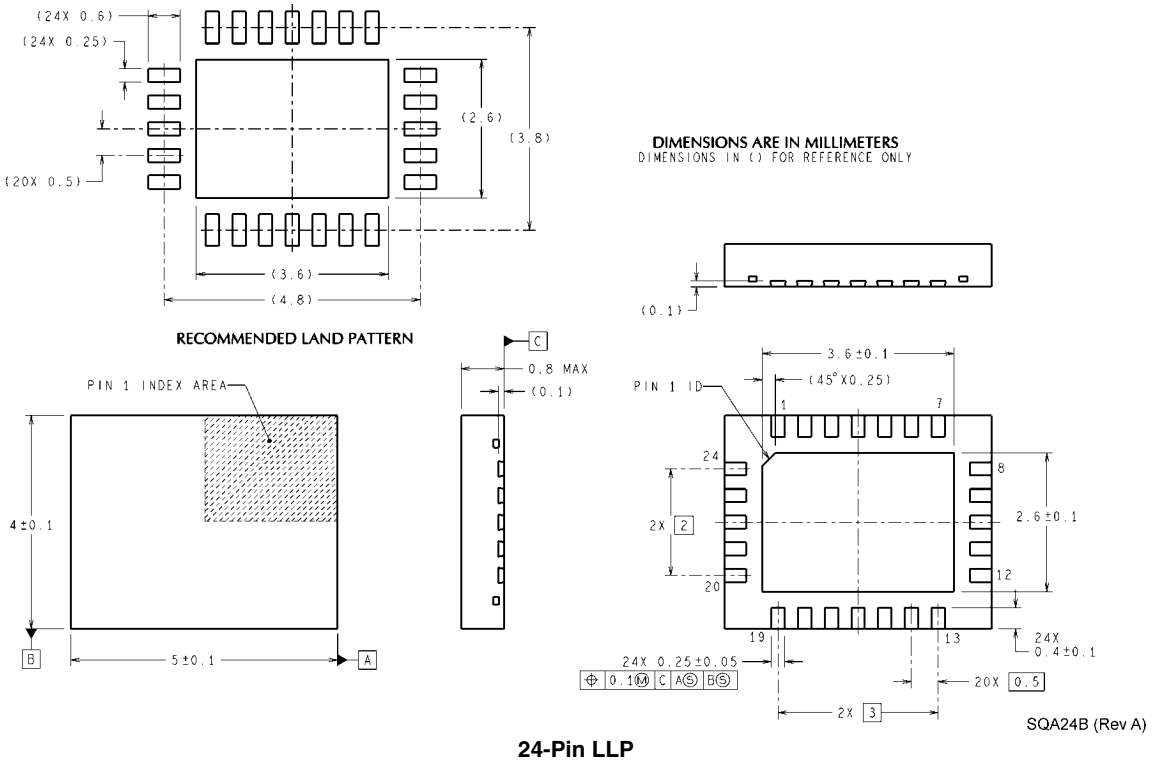
The ground connection for the LMH0346 is through the large exposed DAP. The DAP must be connected to ground for proper operation of the LMH0346. This is the only ground connection for the LMH0346MH. It is the primary ground connection, required for good signal integrity, for the LMH0346SQ.

Physical Dimensions inches (millimeters) unless otherwise noted



MXA20A (Rev C)

20-Pin e-TSSOP
Order Number LMH0346MH
NS Package Number MXA20A



SQA24B (Rev A)

24-Pin LLP
Order Number LMH0346SQ
NS Package Number SQA24B

Notes

Notes

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