



# CAT25C64

## 64K-Bit SPI Serial CMOS EEPROM

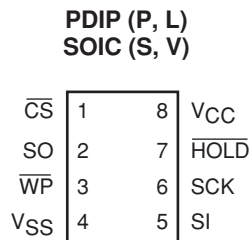
### FEATURES

- 10 MHz SPI compatible
- 1.8 to 5.5 volt operation
- Hardware and software protection
- Low power CMOS technology
- SPI modes (0,0 & 1,1)
- Commercial, industrial and automotive temperature ranges
- 1,000,000 program/erase cycles
- 100 year data retention
- Self-timed write cycle
- 8-pin DIP and SOIC
- 64-Byte page write buffer
- Block write protection
  - Protect 1/4, 1/2 or all of EEPROM array

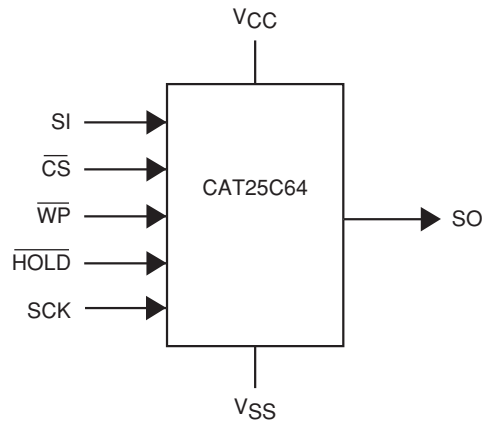
### DESCRIPTION

The CAT25C64 is a 64K-Bit SPI Serial CMOS EEPROM internally organized as 8Kx8 bits. Catalyst's advanced CMOS Technology substantially reduces device power requirements. The CAT25C64 features a 64-byte page write buffer. The device operates via the SPI bus serial interface and is enabled through a Chip Select ( $\overline{CS}$ ). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are required to access the device. The  $\overline{HOLD}$  pin may be used to suspend any serial communication without resetting the serial sequence. The CAT25C64 is designed with software and hardware write protection features including Block write protection. The device is available in 8-pin DIP and SOIC packages.

### PIN CONFIGURATION



### FUNCTIONAL SYMBOL



### PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
$\overline{WP}$	Write Protect
VCC	+1.8V to +5.5V Power Supply
VSS	Ground
$\overline{CS}$	Chip Select
SI	Serial Data Input
$\overline{HOLD}$	Suspends Serial Input

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on any Pin with Respect to $V_{SS}^{(1)}$ .....	-2.0V to $+V_{CC} + 2.0V$
$V_{CC}$ with Respect to $V_{SS}$ .....	-2.0V to +7.0V
Package Power Dissipation Capability ( $T_a = 25^\circ\text{C}$ ) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units
$N_{END}^{(3)}$	Endurance	1,000,000		Cycles/Byte
$T_{DR}^{(3)}$	Data Retention	100		Years

**D.C. OPERATING CHARACTERISTICS**

$V_{CC} = +1.8V$  to  $+5.5V$ , unless otherwise specified.

Symbol	Parameter	Limits			Test Conditions	Units
		Min.	Typ.	Max.		
$I_{CC1}$	Power Supply Current (Operating Write)			10	$V_{CC} = 5V @ 10MHz$ $SO = \text{open}; CS = V_{SS}$	mA
$I_{CC2}$	Power Supply Current (Operating Read)			2	$V_{CC} = 5.0V$ $F_{CLK} = 10MHz$	mA
$I_{SB}^{(4)}$	Power Supply Current (Standby)			1	$\overline{CS} = V_{CC}$ $V_{IN} = V_{SS} \text{ or } V_{CC}$	$\mu A$
$I_{LI}$	Input Leakage Current			2		$\mu A$
$I_{LO}$	Output Leakage Current			3	$V_{OUT} = 0V \text{ to } V_{CC},$ $CS = 0V$	$\mu A$
$V_{IL}^{(5)}$	Input Low Voltage	-1		$V_{CC} \times 0.3$		V
$V_{IH}^{(5)}$	Input High Voltage	$V_{CC} \times 0.7$		$V_{CC} + 0.5$		V
$V_{OL1}$	Output Low Voltage			0.4	$2.7V \leq V_{CC} < 5.5V$ $I_{OL} = 3.0mA$ $I_{OH} = -1.6mA$	V
$V_{OH1}$	Output High Voltage	$V_{CC} - 0.8$				V
$V_{OL2}$	Output Low Voltage			0.2	$1.8V \leq V_{CC} < 2.7V$ $I_{OL} = 150\mu A$ $I_{OH} = -100\mu A$	V
$V_{OH2}$	Output High Voltage	$V_{CC} - 0.2$				V

Note:

- (1) The minimum DC input voltage is  $-0.5V$ . During transitions, inputs may undershoot to  $-2.0V$  for periods of less than 20 ns. Maximum DC voltage on output pins is  $V_{CC} + 0.5V$ , which may overshoot to  $V_{CC} + 2.0V$  for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) These parameter are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- (4) Maximum standby current ( $I_{SB}$ ) =  $10\mu A$  for the Automotive and Extended Automotive temperature range.
- (5)  $V_{IL}$  min and  $V_{IH}$  max are reference values only and are not tested.

**PIN CAPACITANCE (1)**

 Applicable over recommended operating range from  $T_A=25^\circ\text{C}$ ,  $f=1.0\text{ MHz}$ ,  $V_{CC}=\pm 5.0\text{V}$  (unless otherwise noted).

Symbol	Test Conditions	Max.	Conditions	Units
$C_{OUT}$	Output Capacitance (SO)	8	$V_{OUT}=0\text{V}$	pF
$C_{IN}$	Input Capacitance ( $\overline{CS}$ , SCK, SI, $\overline{WP}$ , HOLD)	6	$V_{IN}=0\text{V}$	pF

**A.C. CHARACTERISTICS**

SYMBOL	PARAMETER	CAT25C64-1.8		CAT25C64				Test Conditions	UNITS
		$V_{CC} = 1.8\text{V} - 5.5\text{V}$		$V_{CC} = 2.5\text{V} - 5.5\text{V}$		$V_{CC} = 4.5\text{V} - 5.5\text{V}$			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{SU}$	Data Setup Time	50		50		20		$C_L = 50\text{pF}$ (2)	ns
$t_H$	Data Hold Time	50		50		20			ns
$t_{WH}$	SCK High Time	250		125		40			ns
$t_{WL}$	SCK Low Time	250		125		40			ns
$f_{SCK}$	Clock Frequency	DC	1	DC	3	DC	10		MHz
$t_{LZ}$	$\overline{HOLD}$ to Output Low Z		50		50		50		ns
$t_{RI}^{(1)}$	Input Rise Time		2		2		2		$\mu\text{s}$
$t_{FI}^{(1)}$	Input Fall Time		2		2		2		$\mu\text{s}$
$t_{HD}$	$\overline{HOLD}$ Setup Time	100		100		40			ns
$t_{CD}$	$\overline{HOLD}$ Hold Time	100		100		40			ns
$t_{WC}^{(3)}$	Write Cycle Time		10		10		5		ms
$t_V$	Output Valid from Clock Low		250		125		40		ns
$t_{HO}$	Output Hold Time	0		0		0			ns
$t_{DIS}$	Output Disable Time		250		250		75		ns
$t_{HZ}$	$\overline{HOLD}$ to Output High Z		150		100		50		ns
$t_{CS}$	$\overline{CS}$ High Time	500		250		100			ns
$t_{CSS}$	$\overline{CS}$ Setup Time	500		250		100			ns
$t_{CSH}$	$\overline{CS}$ Hold Time	500		250		100		ns	

**Power-Up Timing<sup>(4)(5)</sup>**

Symbol	Parameter	Max.	Units
$t_{PUR}$	Power-up to Read Operation	1	ms
$t_{PUW}$	Power-up to Write Operation	1	ms

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) AC Test Conditions:  
 Input Pulse Voltages:  $0.3V_{CC}$  to  $0.7V_{CC}$   
 Input rise and fall times:  $\leq 10\text{ns}$   
 Input and output reference voltages:  $0.5V_{CC}$   
 Output load: current source IOL max/IOH max;  $C_L=50\text{pF}$
- (3)  $t_{WC}$  is the time from the rising edge of  $\overline{CS}$  after a valid write sequence to the end of the internal write cycle.
- (4) This parameter is tested initially and after a design or process change that affects the parameter.
- (5)  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.

## FUNCTIONAL DESCRIPTION

The CAT25C64 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT25C64 to interface directly with many of today's popular microcontrollers. The CAT25C64 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

After the device is selected with  $\overline{CS}$  going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

## PIN DESCRIPTION

### SI: Serial Input

SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the 25C64. Input data is latched on the rising edge of the serial clock.

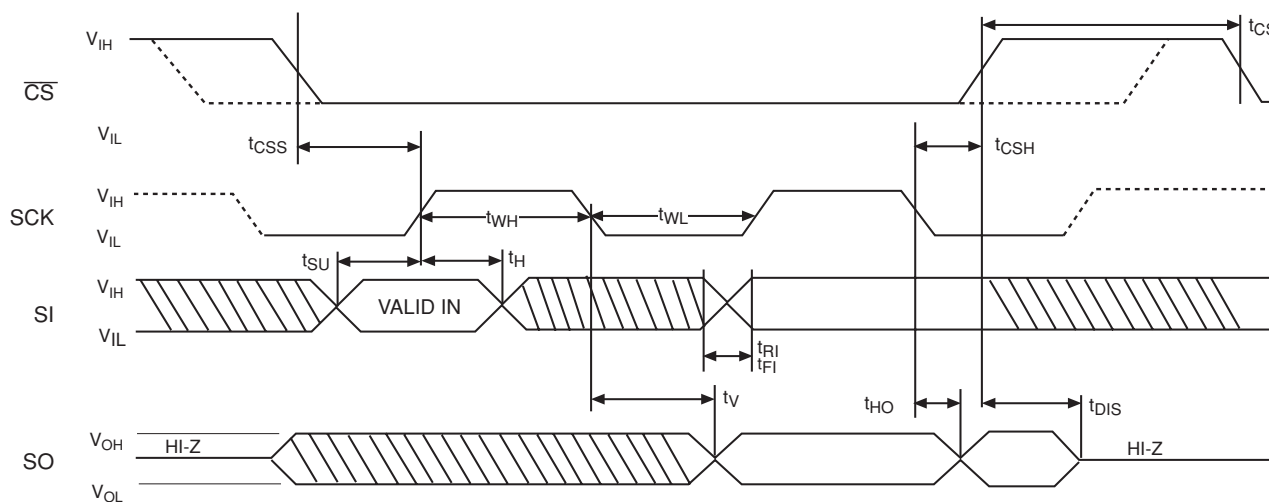
### SO: Serial Output

SO is the serial data output pin. This pin is used to transfer data out of the 25C64. During a read cycle, data is shifted out on the falling edge of the serial clock.

### SCK: Serial Clock

SCK is the serial clock pin. This pin is used to synchronize

**Figure 1. Synchronous Data Timing**



Note: Dashed Line= mode (1, 1) — — — —

## INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

the communication between the microcontroller and the 25C64. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

**$\overline{CS}$ : Chip Select**

$\overline{CS}$  is the Chip select pin.  $\overline{CS}$  low enables the CAT25C64 and  $\overline{CS}$  high disables the CAT25C64.  $\overline{CS}$  high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). The CAT25C64 draws ZERO current in the Standby mode. A high to low transition on  $\overline{CS}$  is required prior to any sequence being initiated. A low to high transition on  $\overline{CS}$  after a valid write sequence is what initiates an internal write cycle.

**$\overline{WP}$ : Write Protect**

$\overline{WP}$  is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When  $\overline{WP}$  is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited.  $\overline{WP}$  going low while  $\overline{CS}$  is still low

will interrupt a write to the status register. If the internal write cycle has already been initiated,  $\overline{WP}$  going low will have no effect on any write operation to the status register. The  $\overline{WP}$  pin function is blocked when the WPEN bit is set to 0.

**$\overline{HOLD}$ : Hold**

The  $\overline{HOLD}$  pin is used to pause transmission to the CAT25C64 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause,  $\overline{HOLD}$  must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication,  $\overline{HOLD}$  is brought high, while SCK is low. ( $\overline{HOLD}$  should be held high any time this function is not being used.)  $\overline{HOLD}$  may be tied high directly to  $V_{CC}$  or tied to  $V_{CC}$  through a resistor. Figure 9 illustrates hold timing sequence.

**STATUS REGISTER**

7	6	5	4	3	2	1	0
WPEN	X	X	X	BP1	BP0	WEL	$\overline{RDY}$

**BLOCK PROTECTION BITS**

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	1800-1FFF	Quarter Array Protection
1	0	1000-1FFF	Half Array Protection
1	1	0000-1FFF	Full Array Protection

**WRITE PROTECT ENABLE OPERATION**

WPEN	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

## STATUS REGISTER

The Status Register indicates the status of the device.

The  $\overline{RDY}$  (Ready) bit indicates whether the CAT25C64 is busy with a write operation. When set to 1 a write cycle is in progress and when set to 0 the device indicates it is ready. This bit is read only.

The WEL (Write Enable) bit indicates the status of the write enable latch. When set to 1, the device is in a Write Enable state and when set to 0 the device is in a Write Disable state. The WEL bit can only be set by the WREN instruction and can be reset by the WRDI instruction.

The BP0 and BP1 (Block Protect) bits indicate which blocks are currently protected. These bits are set by the user issuing the WRSR instruction. The user is allowed to protect quarter of the memory, half of the memory or the entire memory by setting these bits. Once protected the user may only read from the protected portion of the array. These bits are non-volatile.

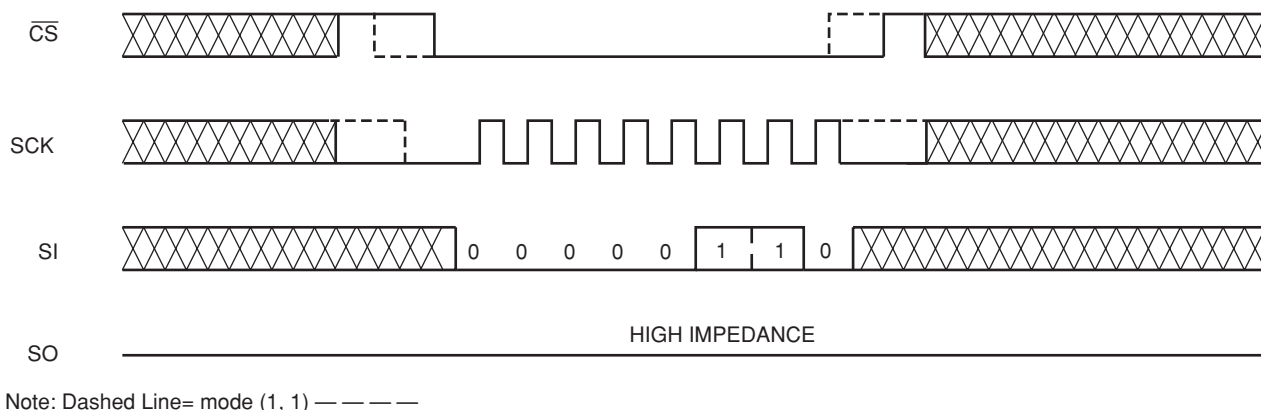
The WPEN (Write Protect Enable) is an enable bit for the WP pin. The WP pin and WPEN bit in the status register control the programmable hardware write protect feature. Hardware write protection is enabled when WP is low and WPEN bit is set to high. The user cannot write to the status register (including the block protect bits and the WPEN bit) and the block protected sections in the memory array when the chip is hardware write protected. Only the sections of the memory array that are not block protected can be written. Hardware write protection is disabled when either WP pin is high or the WPEN bit is zero.

## DEVICE OPERATION

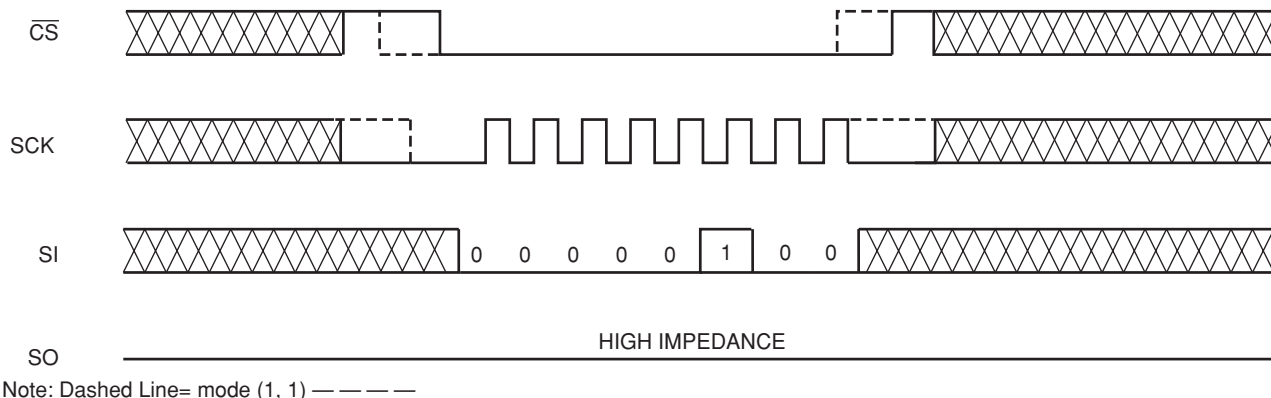
### Write Enable and Disable

The CAT25C64 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when  $V_{CC}$  is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

**Figure 2. WREN Instruction Timing**



**Figure 3. WRDI Instruction Timing**



**READ Sequence**

The part is selected by pulling  $\overline{CS}$  low. The 8-bit read instruction is transmitted to the CAT25C64, followed by the 16-bit address (the three Most Significant Bits are don't care).

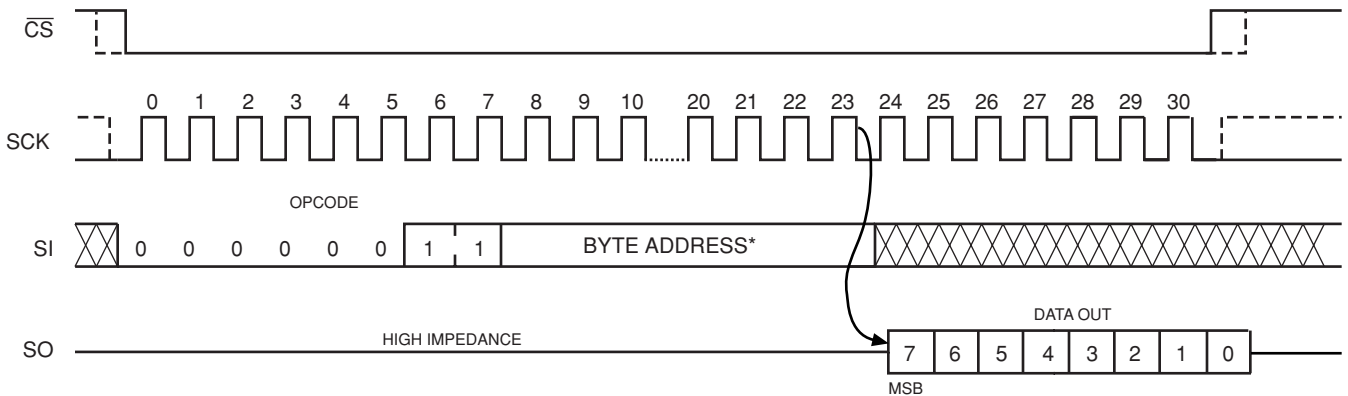
After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address (1FFFh) is reached, the address counter rolls over to 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by pulling the  $\overline{CS}$  high.

To read the status register, RDSR instruction should be sent. The contents of the status register are shifted out on the SO line. The status register may be read at any time even during a write cycle. Read sequence is illustrated in Figure 4. Reading status register is illustrated in Figure 5.

**WRITE Sequence**

The CAT25C64 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to CAT25C64. The device goes into Write enable state by pulling the  $\overline{CS}$  low and then clocking the WREN instruction into CAT25C64. The  $\overline{CS}$  must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without  $\overline{CS}$  being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the address of the memory location(s) to be programmed must be outside the protected address field

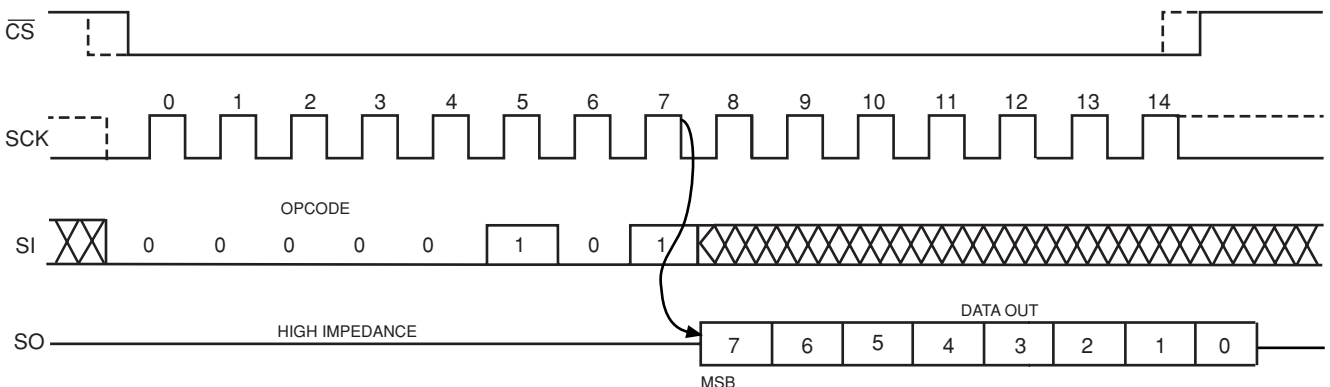
**Figure 4. Read Instruction Timing**



\*Please check the instruction set table for address

Note: Dashed Line= mode (1, 1) — — — —

**Figure 5. RDSR Instruction Timing**



Note: Dashed Line= mode (1, 1) — — — —



location selected by the block protection level.

**Byte Write**

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the  $\overline{CS}$  low, issuing a write instruction via the SI line, followed by the 16-bit address (the three Most Significant Bits are don't care), and then the data to be written. Programming will start after the  $\overline{CS}$  is brought high. Figure 6 illustrates byte write sequence.

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction.

**Page Write**

The CAT25C64 features page write capability. After the first initial byte the host may continue to write up

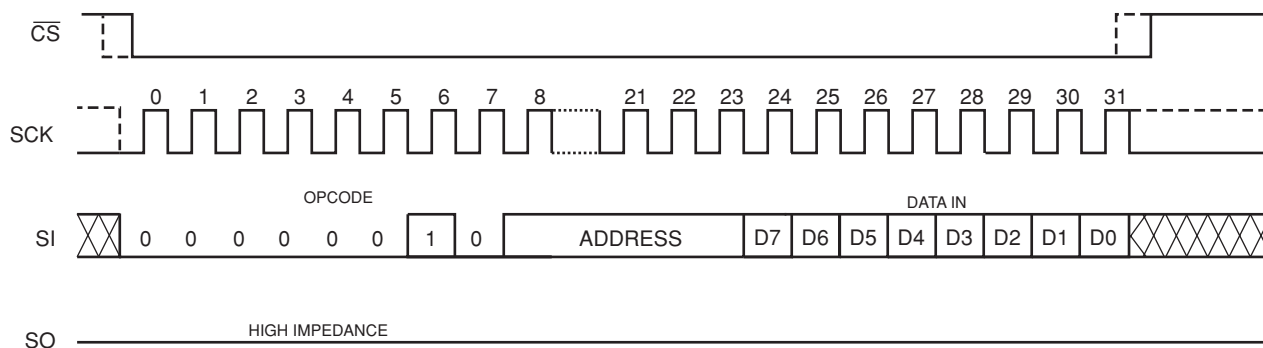
to 64 bytes of data to the CAT25C64. After each byte of data is received, six lower order address bits are internally incremented by one; the high order bits of address will remain constant. The only restriction is that the 64 bytes must reside on the same page. If the address counter reaches the end of the page and clock continues, the counter will “roll over” to the first address of the page and overwrite any data that may have been written. The CAT25C64 is automatically returned to the write disable state at the completion of the write cycle. Figure 8 illustrates the page write sequence.

To write to the status register, the WRSR instruction should be sent. Only Bit 2, Bit 3 and Bit 7 of the status register can be written using the WRSR instruction. Figure 7 illustrates the sequence of writing to status register.

**DESIGN CONSIDERATIONS**

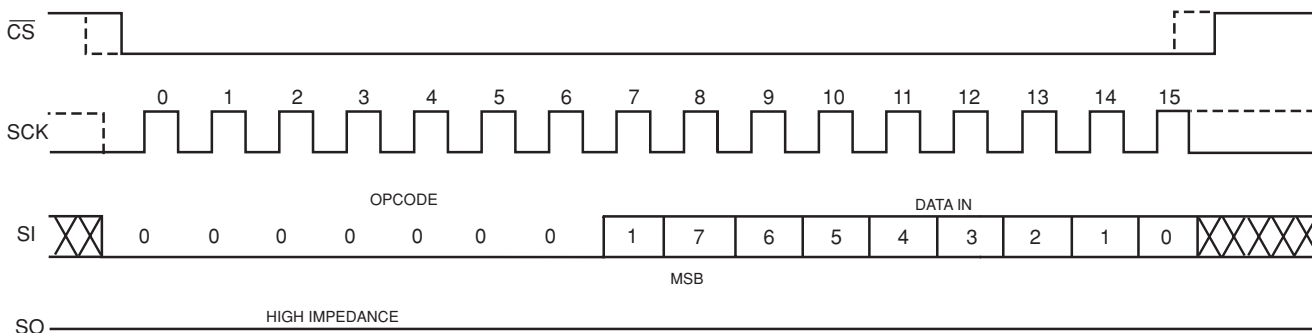
The CAT25C64 powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued to perform any writes to the device after power up. Also, on power up  $\overline{CS}$  should be brought low to enter a ready

**Figure 6. Write Instruction Timing**



Note: Dashed Line= mode (1, 1) - - - -

**Figure 7. WRSR Instruction Timing**



Note: Dashed Line= mode (1, 1) - - - -

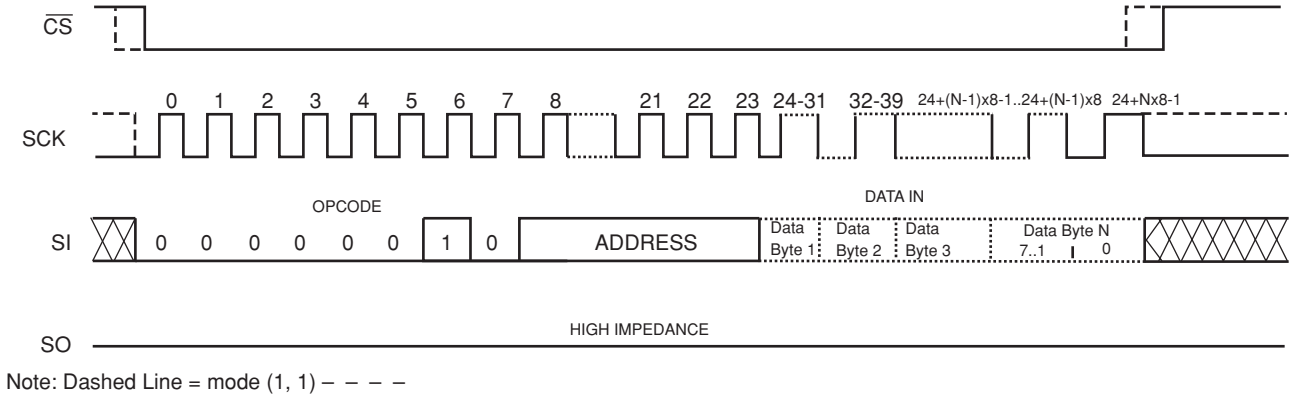


state and receive an instruction. After a successful byte/page write or status register write the CAT25C64 goes into a write disable mode. CS must be set high after the proper number of clock cycles to start an internal write cycle. Access to the array during an internal write cycle is ignored and program-ning is continued. On power up,

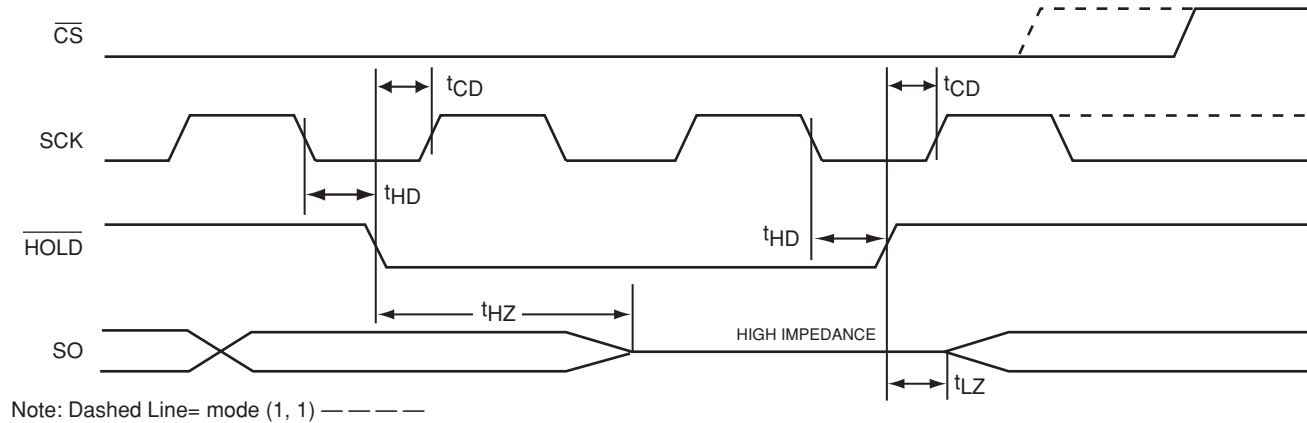
SO is in a high impedance.

When powering down, the supply should be taken down to 0V, so that the CAT25C64 will be reset when power is ramped back up. If this is not possible, then, following a brown-out episode, the CAT25C64 can be reset by refreshing the contents of the Status Register (See Application Note AN10).

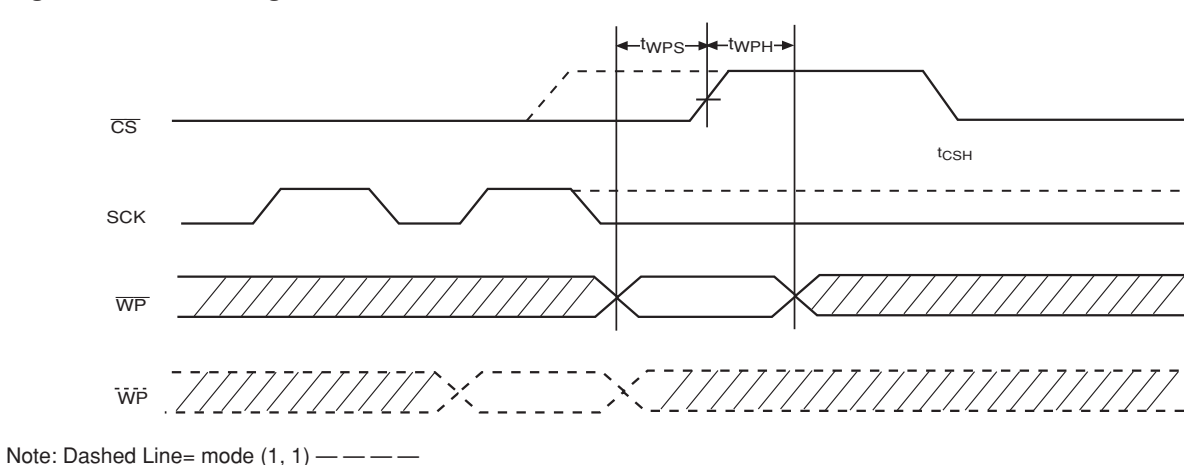
**Figure 8. Page Write Instruction Timing**



**Figure 9. HOLD Timing**

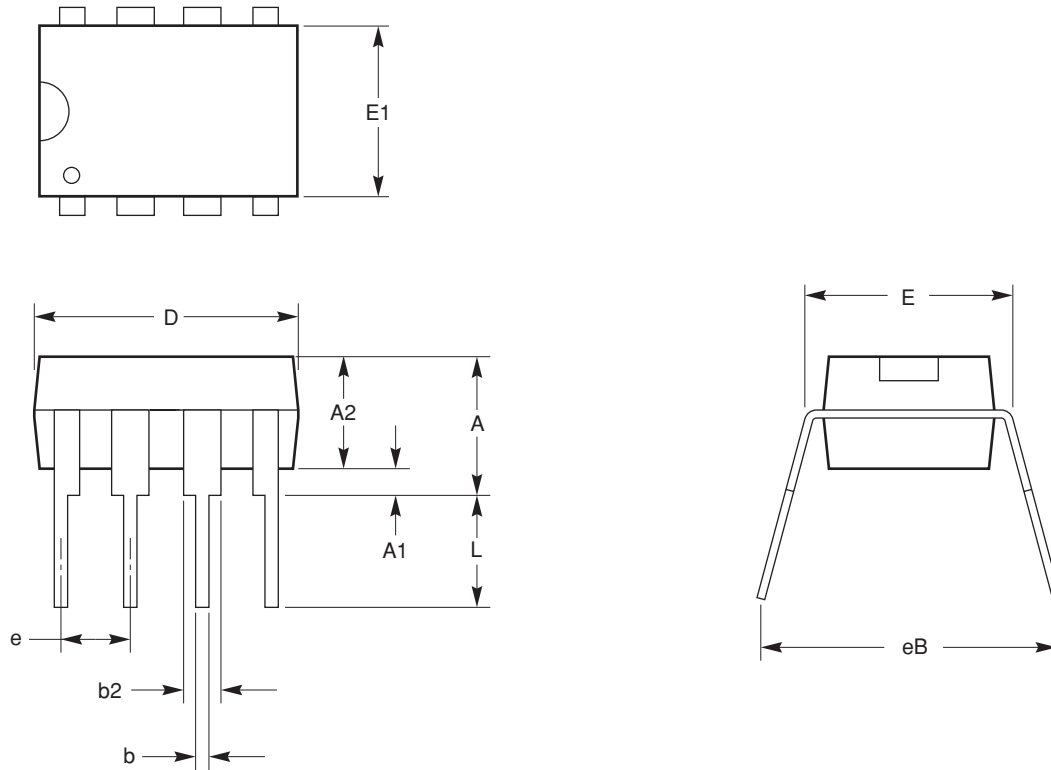


**Figure 10. WP Timing**



**PACKAGE INFORMATION**

**8-LEAD 300 MIL WIDE PLASTIC DIP (P, L)**

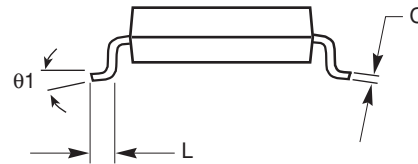
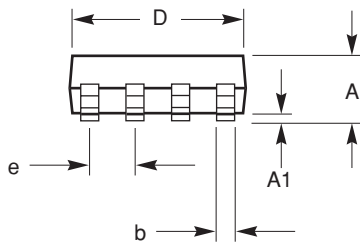
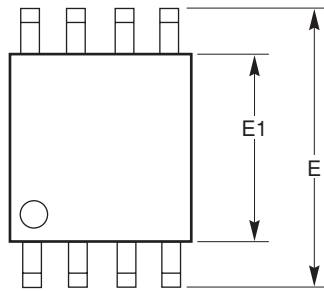


SYMBOL	MIN	NOM	MAX
A	0.120		0.210
A1	0.015		
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b2	0.045	0.060	0.070
D	0.355	0.365	0.400
D2	0.300		0.325
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e		0.100 BSC	
eB			0.430
L	0.115	0.130	0.150

Notes:

1. Complies with JEDEC Standard MS001.
2. All dimensions are in inches.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982

## 8-LEAD 150 MIL WIDE SOIC (S, V)



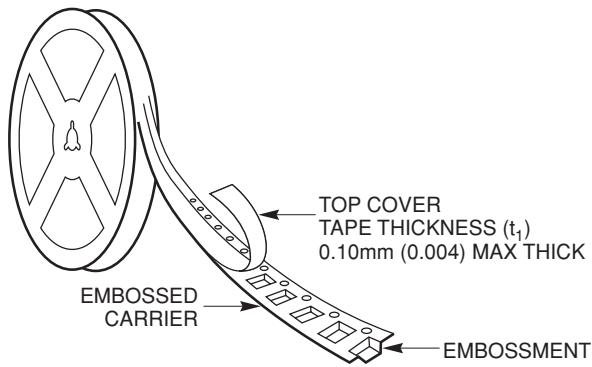
SYMBOL	MIN	NOM	MAX
A1	0.0040		0.0098
A2	0.0532		0.0688
b	0.013		0.020
C	0.0075		0.0098
D	0.1890		0.1968
E	0.2284		0.2440
E1	0.149		0.1574
e		0.050 BSC	
f	0.0099		0.0196
θ1	0°		8°

**Notes:**

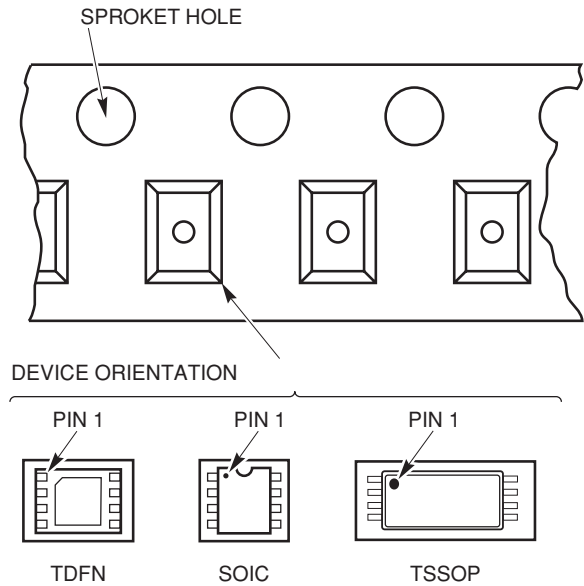
1. Complies with JEDEC specification MS-012 dimensions.
2. All linear dimensions in millimeters.

## TAPE AND REEL

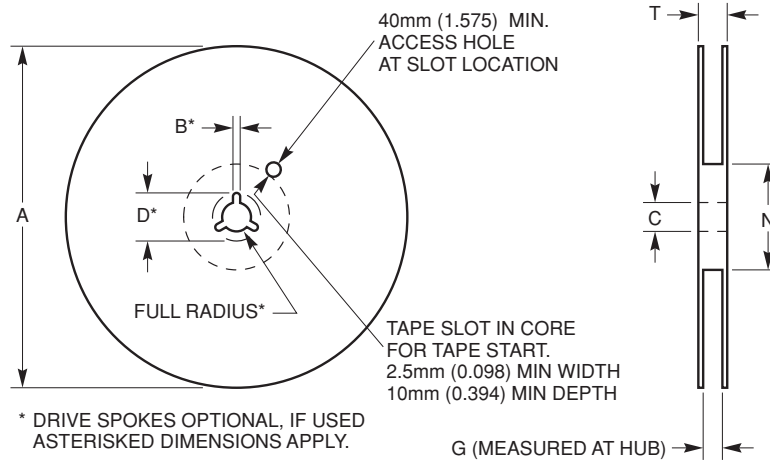
### Direction of Feed



### Device Orientation



### Reel Dimensions<sup>(1)</sup>



### Embossed Carrier Dimensions

TAPE SIZE	A		B MIN	C	D* MIN	N MIN	G	T MAX
	MAX	QTY/REEL						
12MM	330 (13.00)	3000	1.5 (0.059)	12.80 (0.504) 13.20 (0.5200)	20.2 (0.795)	50 (1.969)	12.4 (0.488) 14.4 (0.558)	18.4 (0.724)

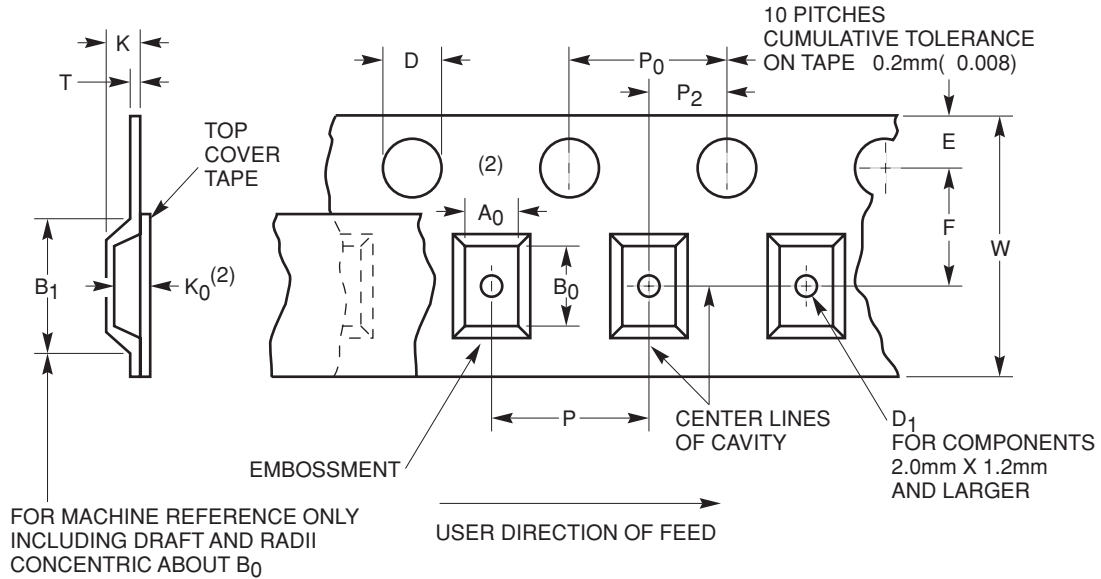
### Component/Tape Size Cross-Reference

Component	Package Type	Tape Size (W)	Part Pitch (P)
8L SOIC	S, V	12mm	8mm

Notes:

(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

**Embossed Carrier Dimensions (12 Page Only)**



**Embossed Tape—Constant Dimensions<sup>(1)</sup>**

Tape Sizes	D	E	P <sub>0</sub>	T Max.	D1 Min.	A <sub>0</sub> B <sub>0</sub> K <sub>0</sub> <sup>(2)</sup>
12mm	<u>1.5 (0.059)</u>	<u>1.65 (0.065)</u>	<u>3.9 (0.153)</u>	400 (0.016)	1.5 (0.059)	
	1.6 (0.063)	1.85 (0.073)	4.1 (0.161)			

**Embossed Tape—Variable Dimensions<sup>(1)</sup>**

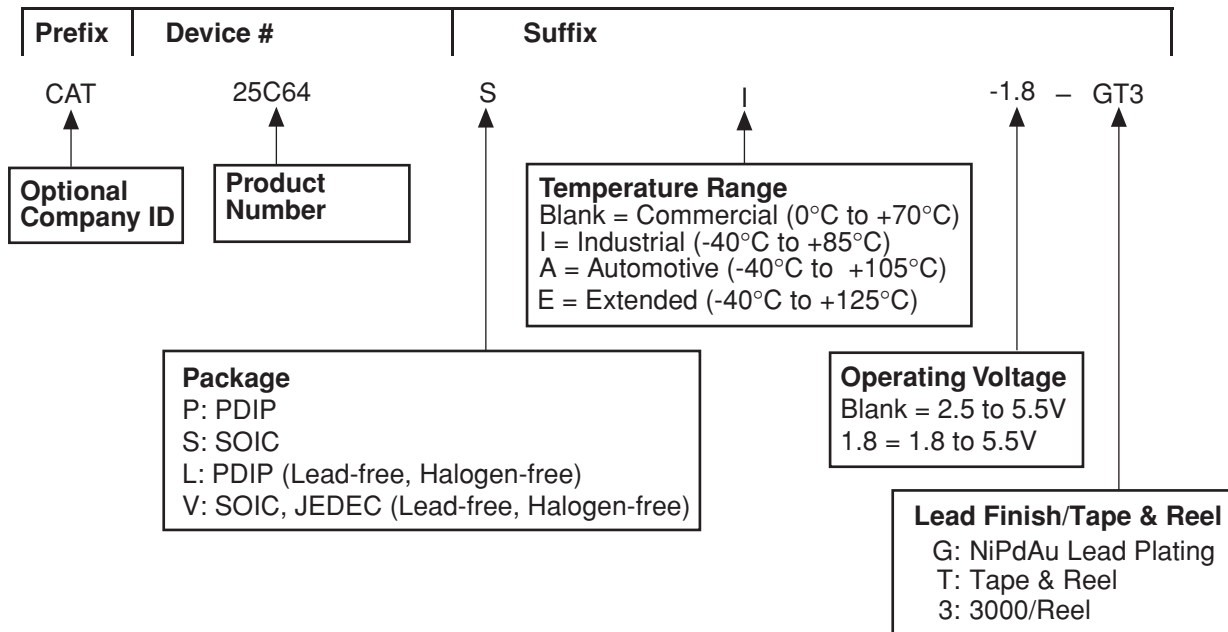
Tape Sizes	B <sub>1</sub> Max.	F	K Max.	P <sub>2</sub>	R Min.	W	P
12mm	8.2 (0.0323)	<u>5.45 (0.0215)</u>	4.5 (0.177)	<u>1.95 (0.077)</u>	30 (1.181)	<u>11.7 (0.460)</u>	<u>7.9 (0.275)</u>
		5.55 (0.0219)		2.05 (0.081)		12.3 (0.484)	8.1 (0.355)

Note:

(1) Metric dimensions will govern; English measurements rounded, for reference only and in parentheses.

(2) A<sub>0</sub> B<sub>0</sub> K<sub>0</sub> are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape, and 0.05 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation.

**ORDERING INFORMATION**

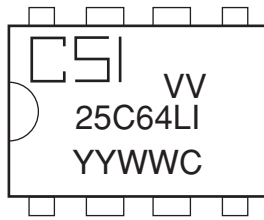


**Notes:**

- (1) The device used in the above example is a 25C64SI-1.8GT3 (SOIC, Industrial Temperature, 1.8 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

## PACKAGE MARKING

### 8-Lead PDIP



CSI = Catalyst Semiconductor, Inc.  
 VV = Voltage Range  
     1.8V - 5.5V = 18  
     2.5V - 5.5V = Blank  
 25C64L = Device Code  
 I = Temperature Range  
 YY = Production Year  
 WW = Production Week  
 C = Product Revision

### 8-Lead SOIC



CSI = Catalyst Semiconductor, Inc.  
 VV = Voltage Range  
     1.8V - 5.5V = 18  
     2.5V - 5.5V = Blank  
 25C64V = Device Code  
 I = Temperature Range  
 YY = Production Year  
 WW = Production Week  
 C = Product Revision



## REVISION HISTORY

Date	Rev.	Reason
12/22/2005	A	Initial Issue
03/21/06	B	Update D.C. Operating Characteristics Update A.C. Characteristics Update Pin Description

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