2N5460, 2N5461, 2N5462

JFET Amplifier

P−Channel − Depletion

ON Semiconductor®

http://onsemi.com

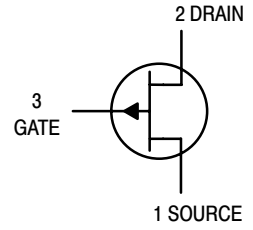
Features

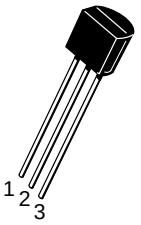
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain − Gate Voltage	V_{DG}	40	Vdc
Reverse Gate − Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	$I_{G(f)}$	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	−65 to +135	°C
Storage Channel Temperature Range	T_{stg}	−65 to +150	°C

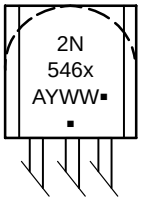
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.





TO−92
CASE 29
STYLE 7

MARKING DIAGRAM



2N546x = Device Code
x = 0, 1, or 2
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate−Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	$V_{(BR)GSS}$	40	−	−	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) (V_{GS} = 30 Vdc, V_{DS} = 0)	2N5460, 2N5461, 2N5462	I_{GSS}	−	−	5.0	nAdc
(V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C) (V_{GS} = 30 Vdc, V_{DS} = 0, T_A = 100°C)	2N5460, 2N5461, 2N5462		−	−	1.0	μAdc
Gate−Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	2N5460 2N5461 2N5462	$V_{GS(off)}$	0.75 1.0 1.8	− − −	6.0 7.5 9.0	Vdc
Gate−Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc) (V_{DS} = 15 Vdc, I_D = 0.2 mAdc) (V_{DS} = 15 Vdc, I_D = 0.4 mAdc)	2N5460 2N5461 2N5462	V_{GS}	0.5 0.8 1.5	− − −	4.0 4.5 6.0	Vdc
ON CHARACTERISTICS						
Zero−Gate−Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460 2N5461 2N5462	I_{DSS}	−1.0 −2.0 −4.0	− − −	−5.0 −9.0 −16	mAdc
SMALL−SIGNAL CHARACTERISTICS						
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	2N5460 2N5461 2N5462	$\|y_{fs}\|$	1000 1500 2000	− − −	4000 5000 6000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)		$\|y_{os}\|$	−	−	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	−	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	−	1.0	2.0	pF
FUNCTIONAL CHARACTERISTICS						
Equivalent Short−Circuit Input Noise Voltage (V_{DS} = 15 Vdc, V_{GS} = 0, f = 100 Hz, BW = 1.0 Hz)		e_n	−	60	115	$nV/\sqrt{Hz}$

ORDERING INFORMATION

Device	Package	Shipping†
2N5460	TO−92	1000 Units / Box
2N5460G	TO−92 (Pb−Free)	
2N5461	TO−92	
2N5461G	TO−92 (Pb−Free)	
2N5461RLRA	TO−92	2000 / Tape & Reel
2N5461RLRAG	TO−92 (Pb−Free)	
2N5462	TO−92	1000 Units / Box
2N5462G	TO−92 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DRAIN CURRENT versus GATE SOURCE VOLTAGE

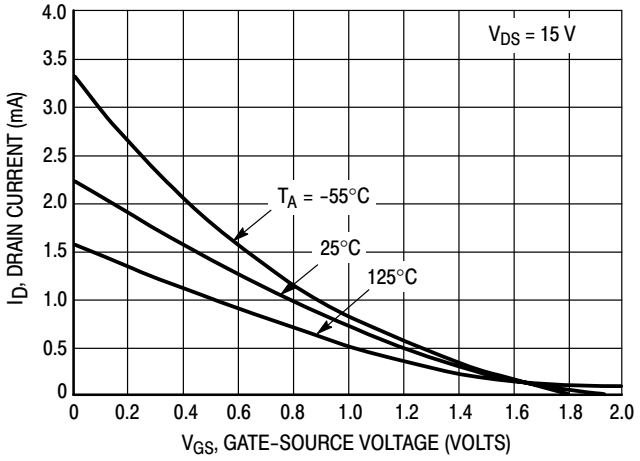


Figure 1. $V_{GS(off)}$ = 2.0 V

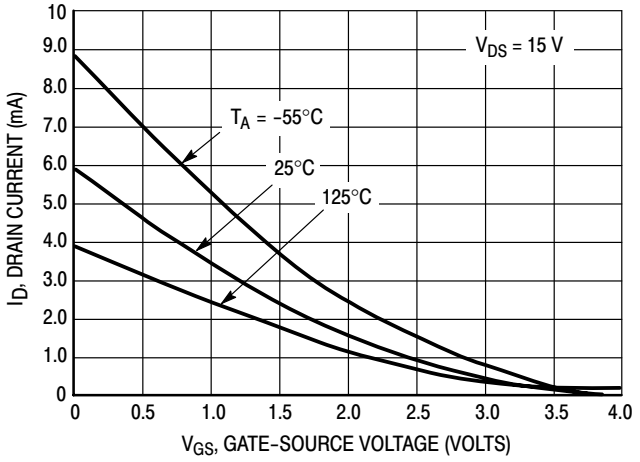


Figure 2. $V_{GS(off)}$ = 4.0 V

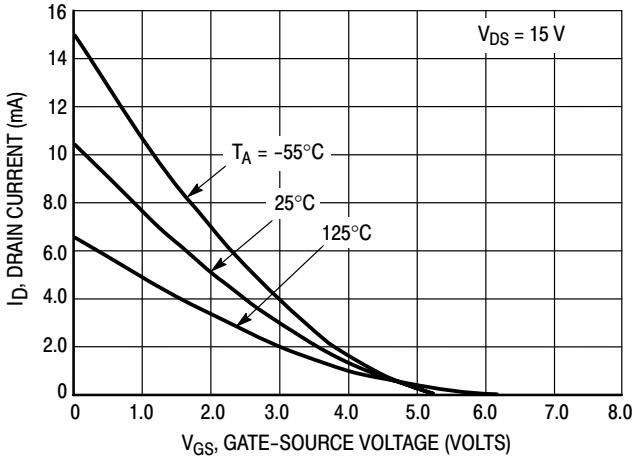


Figure 3. $V_{GS(off)}$ = 5.0 V

FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

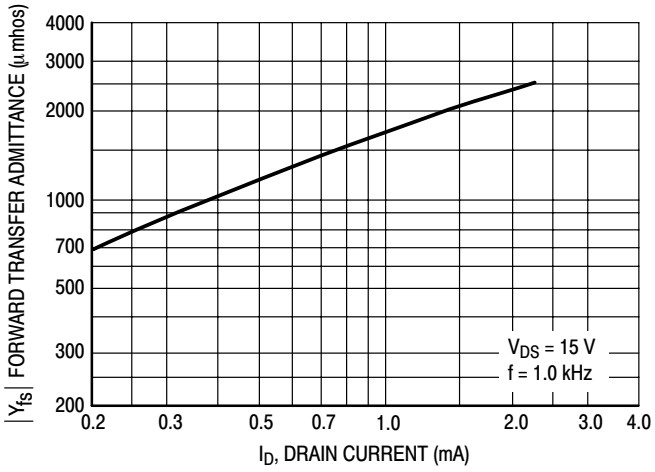


Figure 4. $V_{GS(off)}$ = 2.0 V

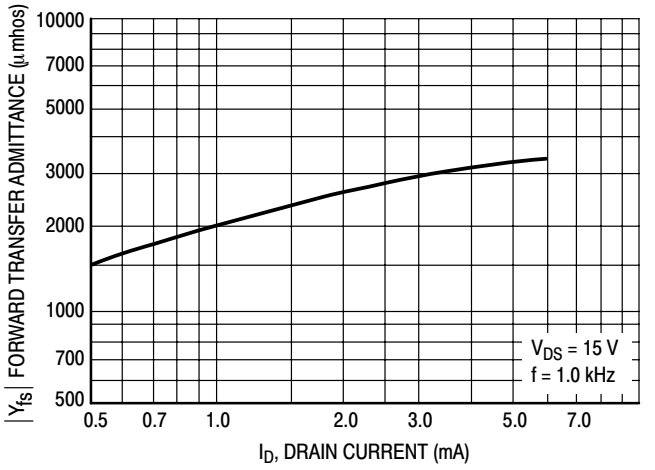


Figure 5. $V_{GS(off)}$ = 4.0 V

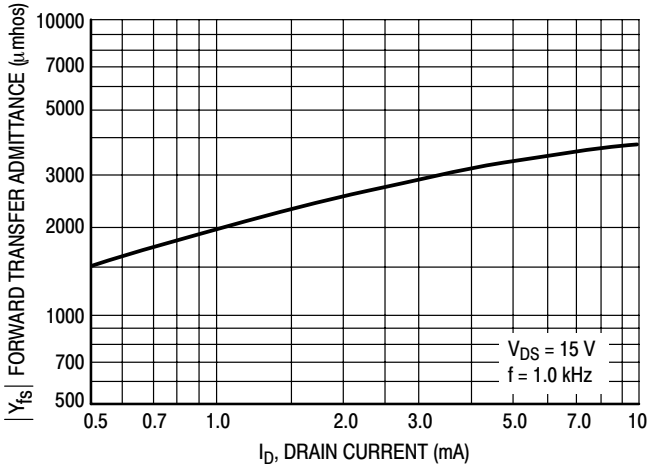


Figure 6. $V_{GS(off)}$ = 5.0 V

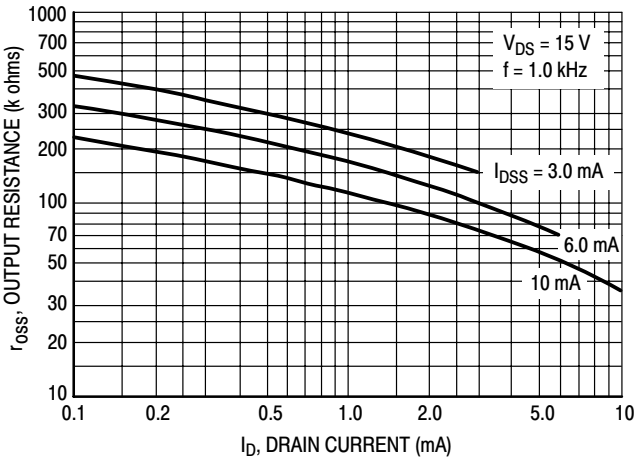


Figure 7. Output Resistance versus Drain Current

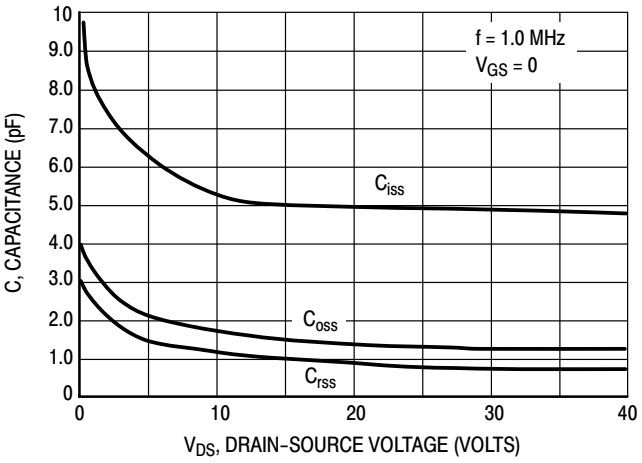


Figure 8. Capacitance versus Drain−Source Voltage

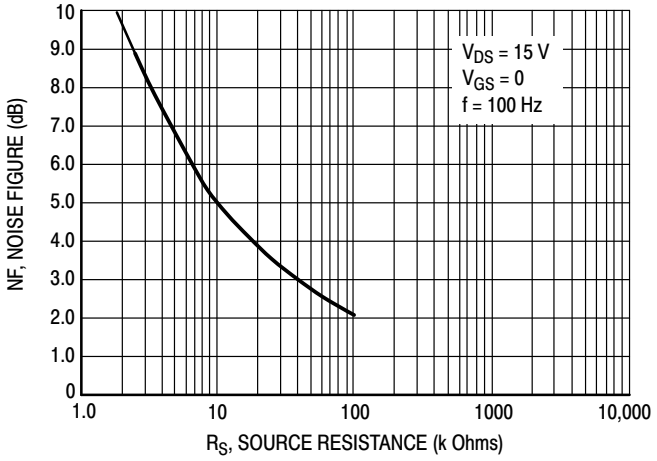
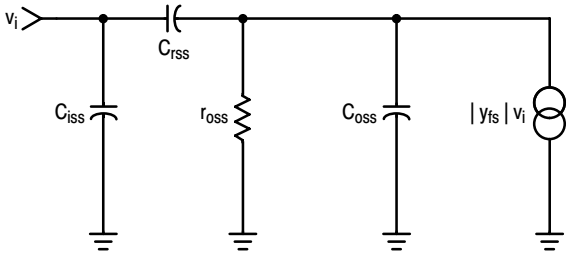


Figure 9. Noise Figure versus Source Resistance



COMMON SOURCE
y PARAMETERS FOR FREQUENCIES
BELOW 30 MHz

$y_{is} = j\Omega\ C_{iss}$
$y_{os} = j\Omega\ C_{osp}$ * + $1/r_{oss}$
$y_{fs} = y_{fs}|$
$y_{rs} = -j\Omega\ C_{rss}$

*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

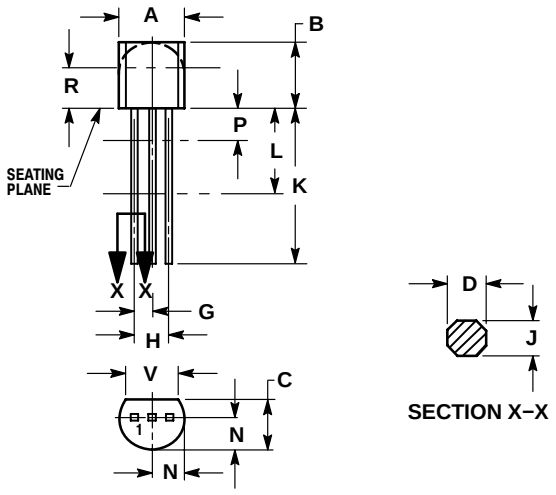
NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

Figure 10. Equivalent Low Frequency Circuit

PACKAGE DIMENSIONS

TO−92
CASE 29−11
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

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