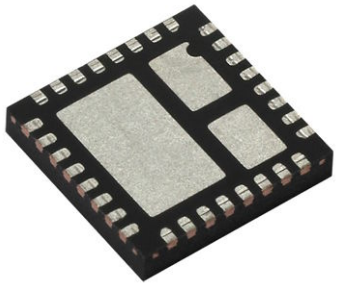
6 A microBUCK® SiC403A/B
Integrated Buck Regulator with Programmable LDO



DESCRIPTION

The Vishay Siliconix SiC403A/B an advanced stand-alone synchronous buck regulator featuring integrated power MOSFETs, bootstrap switch, and a programmable LDO in a space-saving PowerPAK® MLP32-55G pin packages.

The SiC403A/B is capable of operating with all ceramic solutions and switching frequencies up to 1 MHz. The programmable frequency, synchronous operation and selectable power-save allow operation at high efficiency across the full range of load current. The internal LDO may be used to supply 5 V for the gate drive circuits or it may be bypassed with an external 5 V for optimum efficiency.

Additional features include cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown and selectable power-save. The Vishay Siliconix SiC403A/B also provides an enable input and a power good output.

PRIMARY CHARACTERISTICS	
Input voltage range	3 V to 28 V
Output voltage range [a]	0.6 V to V_{IN} x 0.75
Operating frequency	200 kHz to 1 MHz
Continuous output current	6 A
Peak efficiency	93 %
Package	PowerPAK MLP32-55G

Note

a. See “High Output Voltage Operation” section

FEATURES

RoHS COMPLIANT
HALOGEN FREE

- High efficiency > 93 %
- 6 A continuous output current capability
- Integrated bootstrap switch
- Programmable 200 mA LDO with bypass logic
- Temperature compensated current limit
- All ceramic solution enabled
- Pseudo fixed-frequency adaptive on-time control
- Programmable input UVLO threshold
- Independent enable pin for switcher and LDO
- Selectable ultra-sonic power-save mode (SiC403A)
- Selectable power-save mode (SiC403B)
- Programmable soft-start
- 1 % internal reference voltage
- Power good output
- Over-voltage and under-voltage protections
- PowerCAD Simulation software available at www.vishay.com/power-ics/powercad-list/
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Notebook, desktop, and server computers
- Digital HDTV and digital consumer applications
- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Embedded applications
- Point of load power supplies

For technical questions, contact: powerictechsupport@vishay.com

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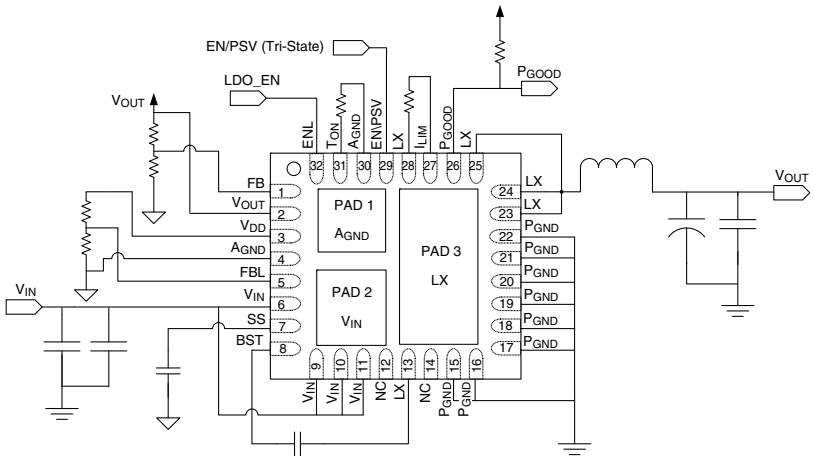
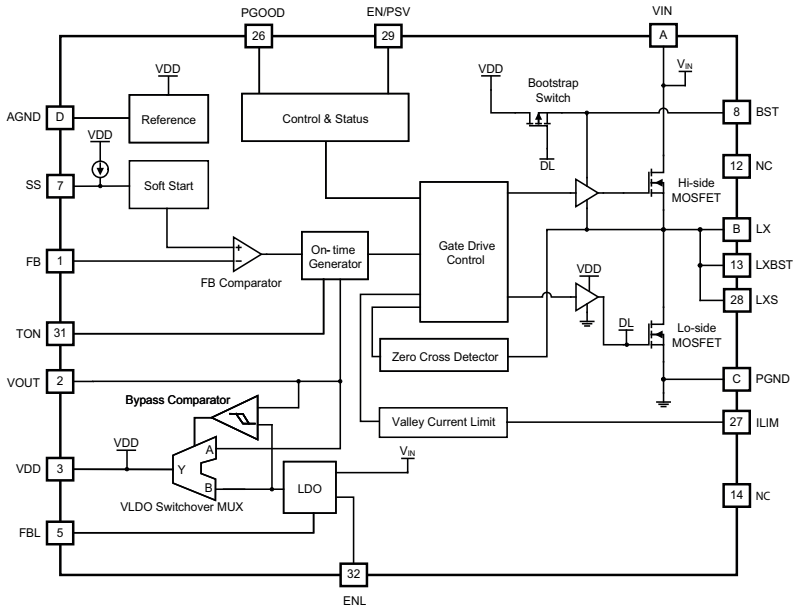
TYPICAL APPLICATION CIRCUIT AND PACKAGE OPTIONS



Typical Application Circuit for SiC403A/B (PowerPAK MLP32-55G)

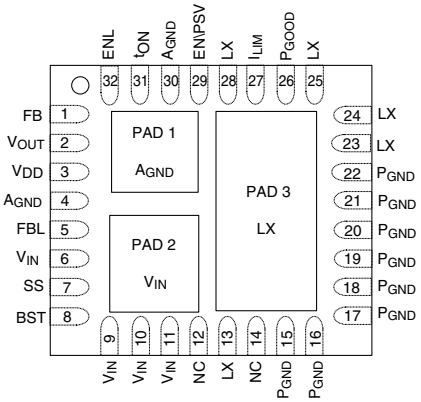
FUNCTIONAL BLOCK DIAGRAM



A = connected to pins 6, 9-11, PAD 2
B = connected to pins 23-25, PAD 3
C = connected to pins 15-22
D = connect to pins 4, 30, PAD 1

SiC403A/B Functional Block Diagram

PIN CONFIGURATION



SiC403A/B Pin Configuration (Top View)

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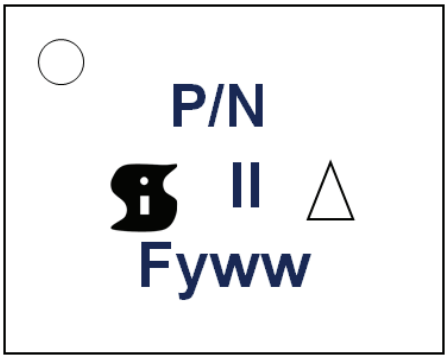
PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	FB	Feedback input for switching regulator used to program the output voltage - connect to an external resistor divider from V_{OUT} to A_{GND}.
2	V_{OUT}	Switcher output voltage sense pin - also the input to the internal switch-over between V_{OUT} and V_{LDO}. The voltage at this pin must be less than or equal to the voltage at the V_{DD} pin.
3	V_{DD}	Bias supply for the IC - when using the internal LDO as a bias power supply, V_{DD} is the LDO output. When using an external power supply as the bias for the IC, the LDO output should be disabled.
4, 30, PAD 1	A_{GND}	Analog ground
5	FBL	Feedback input for the internal LDO - used to program the LDO output. Connect to an external resistor divider from V_{DD} to A_{GND}.
6, 9 to 11, PAD 2	V_{IN}	Input supply voltage
7	SS	The soft start ramp will be programmed by an internal current source charging a capacitor on this pin.
8	BST	Bootstrap pin - connect a capacitor of at least 100 nF from BST to LX to develop the floating supply for the high-side gate drive.
12, 14	NC	No connection
13	LXBST	LX Boost - connect to the BST capacitor.
23 to 25, PAD3	LX	Switching (phase) node
15 to 22	P_{GND}	Power ground
26	P_{GOOD}	Open-drain power good indicator - high impedance indicates power is good. An external pull-up resistor is required.
27	I_{LIM}	Current limit sense pin - used to program the current limit by connecting a resistor from I_{LIM} to LXS.
28	LXS	LX sense - connects to R_{ILIM}
29	EN/PSV	Enable/power save input for the switching regulator - connect to A_{GND} to disable the switching regulator, connect to V_{DD} to operate with power-save mode and float to operate in forced continuous mode.
31	t_{ON}	On-time programming input - set the on-time by connecting through a resistor to A_{GND}
32	ENL	Enable input for the LDO - connect ENL to A_{GND} to disable the LDO. Drive with logic signal for logic control, or program the V_{IN} UVLO with a resistor divider between V_{IN}, ENL, and A_{GND}.

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING (LINE 1: P/N)
SiC403ACD-T1-GE3	PowerPAK MLP32-55G	SiC403A
SiC403BCD-T1-GE3	PowerPAK MLP32-55G	SiC403B
SiC403DB	Reference board	



Format:

Line 1: P/N

Line 2: Siliconix logo and lot code and ESD symbol

Line 3: factory code and year code and work week code

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ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMITS**	**UNIT**
V_{IN}	to P_{GND}	-0.3 to 30	V
V_{IN}	to V_{DD}	-0.4 max.	
LX	to P_{GND}	-0.3 to 30	
LX (transient < 100 ns)	to P_{GND}	-2 to 30	
V_{DD}	to P_{GND}	-0.3 to 6	
EN/PSV, P_{GOOD}, I_{LIM}, SS, V_{OUT}, FB, FBL	Reference to A_{GND}	-0.3 to + (V_{DD} + 0.3)	
t_{ON}	to P_{GND}	-0.3 to + (V_{DD} - 1.5)	
BST	to LX	-0.3 to+6	
	to P_{GND}	-0.3 to 35	
ENL		-0.3 to V_{IN}	
A_{GND} to P_{GND}		-0.3 to 0.3	
Temperature			
Maximum junction temperature		150	°C
Storage temperature		-65 to +150	
Power Dissipation			
Junction to ambient thermal impedance (R_{thJA}) [b]	IC section	50	°C/W
Maximum power dissipation	Ambient temperature = 25 °C	3.4	W
	Ambient temperature = 100 °C	1.3	
ESD Protection			
	HBM	2	kV
	CDM	1	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability

.

RECOMMENDED OPERATING CONDITIONS (all voltages referenced to GND = 0 V)					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input voltage	V_{IN}	3		28	V
V_{DD} to P_{GND}		3		5.5	
Output voltage	V_{OUT}	0.6		V_{IN} x 0.75	
Temperature					
Ambient temperature	-40 to +85				°C

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ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 12 V, V_{DD} = 5 V, T_A = +25 °C for typ., -40 °C to +85 °C for min. and max., T_J = < 125 °C, typical application circuit	MIN.	TYP.	MAX.	UNIT
Input Power Supplies						
Input supply voltage	V_{IN}		3	-	28	V
V_{DD}	V_{DD}		3	-	5.5	
V_{IN} UVLO threshold [a]	V_{UVLO}	Sensed at ENL pin, rising	2.4	2.6	2.95	
		Sensed at ENL pin, falling	2.23	2.4	2.57	
V_{IN} UVLO hysteresis	$V_{UVLO, HYS}$		-	0.25	-	
V_{DD} UVLO threshold	V_{UVLO}	Measured at V_{DD} pin, rising	2.5	-	3	
		Measured at V_{DD} pin, falling	2.4	-	2.9	
V_{DD} UVLO hysteresis	$V_{UVLO, HYS}$		-	0.2	-	
V_{IN} supply current	I_{IN}	ENL, EN/PSV = 0 V, V_{IN} = 28 V	-	12	20	µA
		Standby mode; ENL = V_{DD}, EN/PSV = 0 V	-	160	-	
V_{DD} supply current	I_{DD}	ENL, EN/PSV = 0 V	-	190	300	
		SiC403A, EN/PSV = V_{DD}, no load (f_{SW} = 25 kHz), V_{FB} > 0.6 V [b]	-	0.3	-	mA
		SiC403B, EN/PSV = V_{DD}, no load, V_{FB} > 0.6 V [b]	-	0.7	-	
		V_{DD} = 5 V, f_{SW} = 250 kHz, EN/PSV = floating, no load [b]	-	8	-	
		V_{DD} = 3 V, f_{SW} = 250 kHz, EN/PSV = floating, no load [b]	-	5	-	
FB on-time threshold		Static V_{IN} and load	0.594	0.600	0.606	V
Frequency range	f_{SW}	Continuous mode operation	-	-	1000	kHz
		Minimum f_{SW}, (SiC403A only)	-	25	-	
Bootstrap switch resistance			-	10	-	Ω
Timing						
On-time	t_{ON}	Continuous mode operation V_{IN} = 12 V, V_{OUT} = 5 V, f_{SW} = 300 kHz, R_{ton} = 133 kΩ	999	1110	1220	ns
Minimum on-time [b]	$t_{ON, min.}$		-	80	-	
Minimum off-time [b]	$t_{OFF, min.}$	V_{DD} = 5 V	-	250	-	
		V_{DD} = 3 V	-	370	-	
Soft Start						
Soft start current [b]	I_{SS}		-	3	-	µA
Soft start voltage [b]	V_{SS}	When V_{OUT} reaches regulation	-	1.5	-	V
Analog Inputs/Outputs						
V_{OUT} input resistance	R_{O-IN}		-	500	-	kΩ
Current Sense						
Zero-crossing detector threshold voltage	$V_{Sense-th}$	LX-P_{GND}	-3	-	+3	mV
Power Good						
Power good threshold	PG_V_{TH_UPPER}	Upper limit, V_{FB} > internal 600 mV reference	-	+20	-	%
	PG_V_{TH_LOWER}	Lower limit, V_{FB} < internal 600 mV reference	-	-10	-	
Start-up delay time (between PWM enable and P_{GOOD} high)	PG_T_d	V_{DD} = 5 V, C_{SS} = 10 nF	-	12	-	ms
		V_{DD} = 3 V, C_{SS} = 10 nF	-	7	-	
Fault (noise-immunity) delay time [b]	PG_I_{CC}		-	5	-	µs
Leakage current	PG_I_{LK}		-	-	1	µA
Power good on-resistance	PG_R_{DS_ON}		-	10	-	Ω

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ELECTRICAL SPECIFICATIONS						
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS SPECIFIED** V_{IN} = 12 V, V_{DD} = 5 V, T_A = +25 °C for typ., -40 °C to +85 °C for min. and max., T_J = < 125 °C, typical application circuit	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Fault Protection						
Valley current Limit	I_{LIM}	V_{DD} = 5 V, R_{ILIM} = 4750, T_J = 0 °C to +125 °C	4.8	6	7.2	A
		V_{DD} = 3.3 V, R_{ILIM} = 4750	-	5.1	-	
I_{LIM} source current			-	10	-	µA
I_{LIM} comparator offset voltage	V_{ILM-LK}	With respect to A_{GND}	-10	0	+10	mV
Output under-voltage fault	V_{OUT_Fault}	V_{FB} with respect to Internal 600 mV reference, 8 consecutive clocks	-	-25	-	%
Smart power-save protection threshold voltage [b]	P_{Save_VTH}	V_{FB} with respect to internal 600 mV	-	+10	-	
Over-voltage protection threshold		V_{FB} with respect to internal 600 mV	-	+20	-	
Over-voltage fault delay [b]	$t_{OV-Delay}$		-	5	-	µs
Over temperature shutdown [b]	TShut	10 °C hysteresis	-	150	-	°C
Logic Inputs/Outputs						
Logic input high voltage	V_{IH}		1	-	-	V
Logic input low voltage	V_{IL}		-	-	0.4	
EN/PSV input for P-Save operation [b]		V_{DD} = 5 V	2.2	-	5	
EN/PSV input for forced continuous operation [b]			1	-	2	
EN/PSV input for disabling switcher			0	-	0.4	
EN/PSV input bias current	I_{EN}	EN/PSV = V_{DD} or GND	-10	-	+10	µA
ENL Input bias current	I_{ENL}	ENL = V_{IN} = 28 V	-	11	18	
FBL, FB input bias current	FBL_I_{LK}	FBL, FB = V_{DD} or GND	-1	-	+1	
Linear Dropout Regulator						
FBL [b]	$V_{LDO\ ACC}$		-	0.75	-	V
LDO current limit	LDO_I_{LIM}	Short-circuit protection, V_{IN} = 12 V, V_{DD} < 0.75 V	-	65	-	mA
		Start-up and foldback, V_{IN} = 12 V, 0.75 < V_{DD} < 90 % of final V_{DD} value	-	115	-	
		Operating current limit, V_{IN} = 12 V, V_{DD} > 90 % of final V_{DD} value	135	200	-	
V_{LDO} to V_{OUT} switch-over threshold [d]	$V_{LDO-BPS}$		-130	-	+130	mV
V_{LDO} to V_{OUT} non-switch-over threshold [d]	$V_{LDO-NBPS}$		-500	-	+500	
V_{LDO} to V_{OUT} switch-over resistance	R_{LDO}	V_{OUT} = 5 V	-	2	-	Ω
LDO drop out voltage [e]		From V_{IN} to V_{DD}, V_{DD} = +5 V, I_{VLDO} = 100 mA	-	1.2	-	V

Notes

a. V_{IN} UVLO is programmable using a resistor divider from V_{IN} to ENL to A_{GND}. The ENL voltage is compared to an internal reference

b. Typical value measured on standard evaluation board

c. SiC403A/B has first order temperature compensation for over current. Results vary based upon the PCB thermal layout

d. The switch-over threshold is the maximum voltage differential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will internally switch-over to V_{OUT}. The non-switch-over threshold is the minimum voltage differential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will not switch-over to V_{OUT}

e. The LDO drop out voltage is the voltage at which the LDO output drops 2 % below the nominal regulation point

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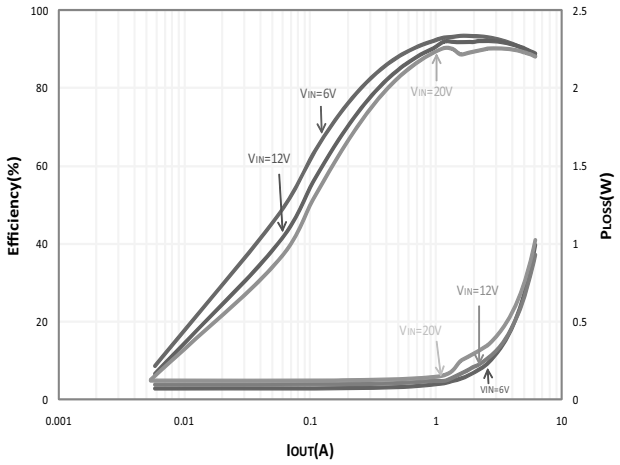
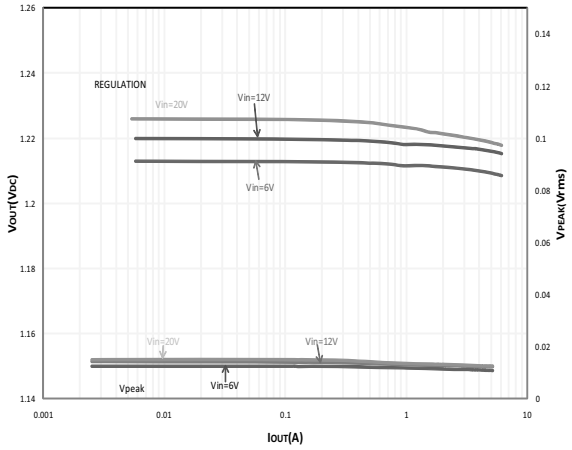


Efficiency vs. Load-Forced Continuous Mode
V_{OUT} = 1.2 V, V_{DD} = 5 V, EN/PSV is Floating, External Bias, SiC403B



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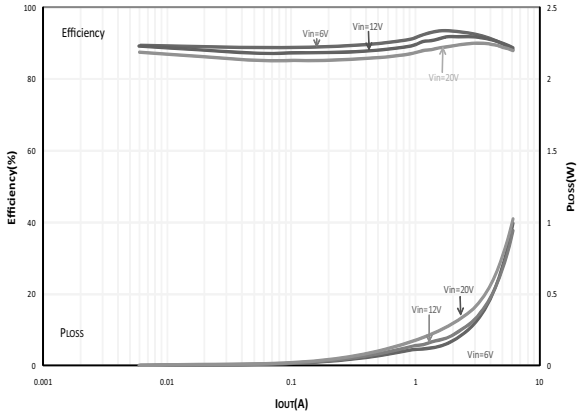
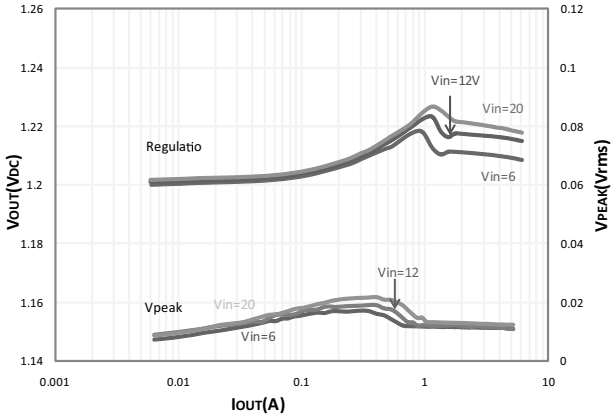
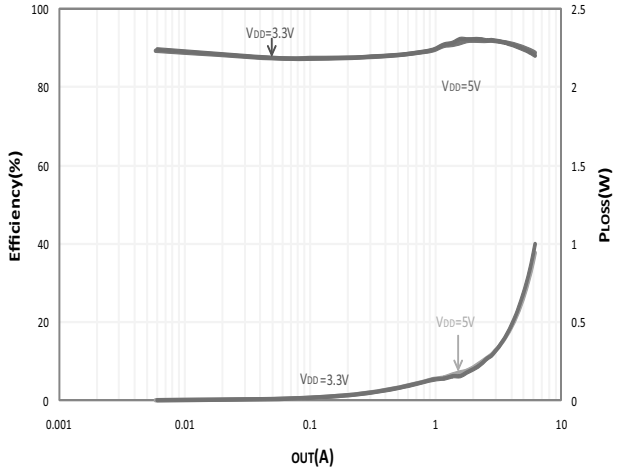


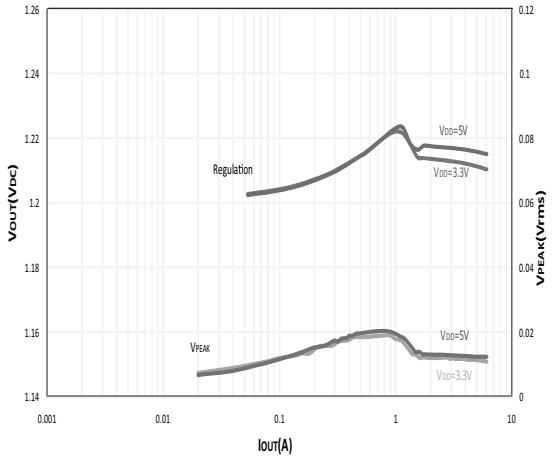
Efficiency vs. Load-PSAVE Mode
V_{OUT}T = 1.2 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403B



V_{OUT} vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403B



Efficiency vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{IN} = 12 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403B



V_{OUT} vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{IN} = 12 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403B

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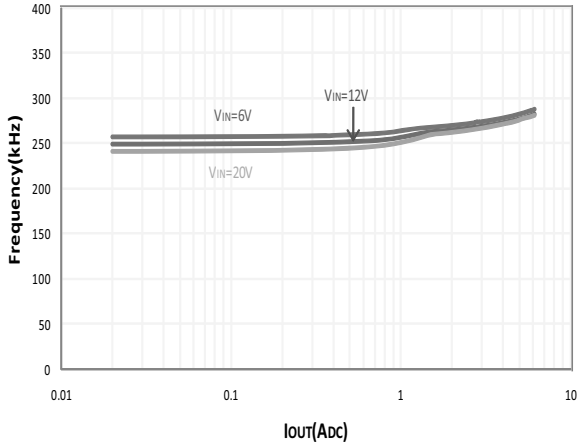
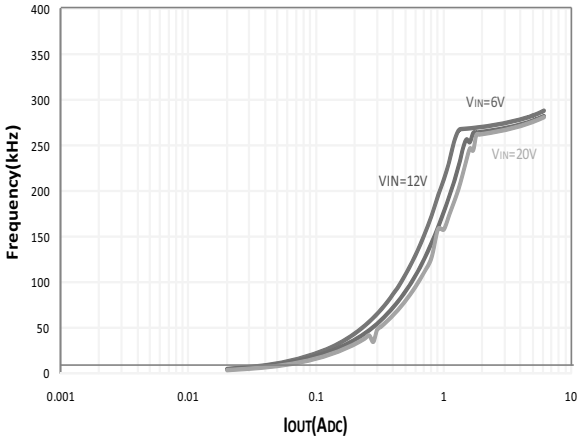
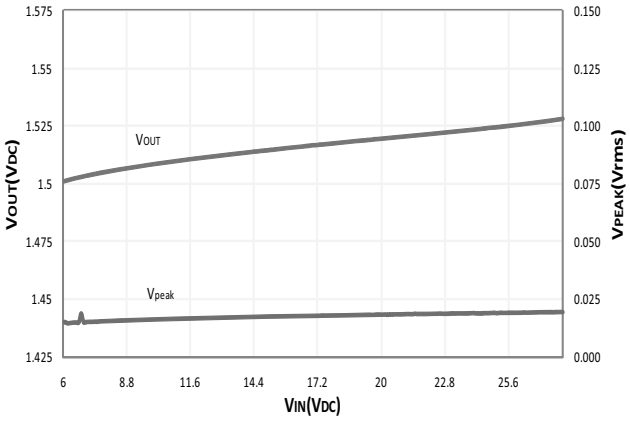


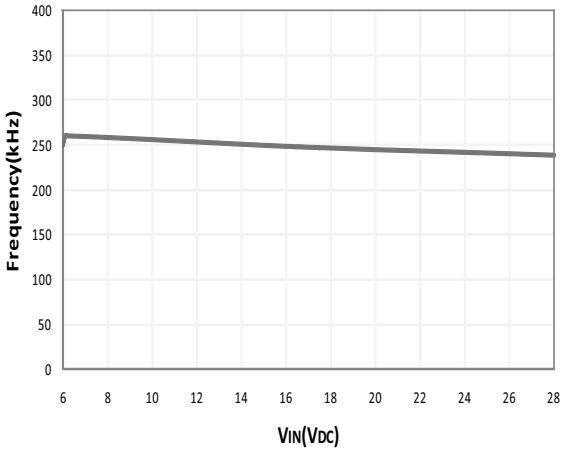
Frequency vs. Load-Forced Continuous Mode
V_{OUT} = 1.2 V, V_{DD} = 5 V, EN/PSV is Floating, External Bias, SiC403B



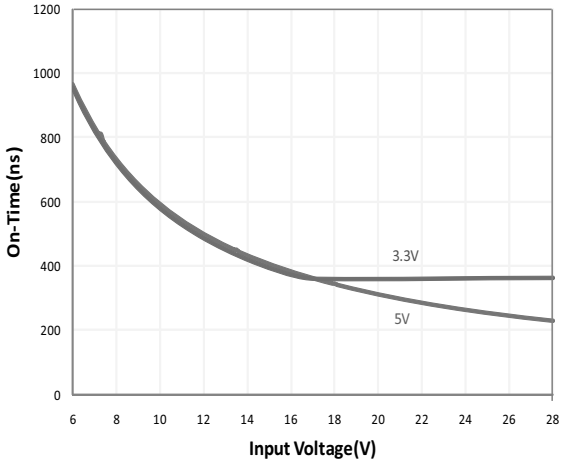
Frequency vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403B



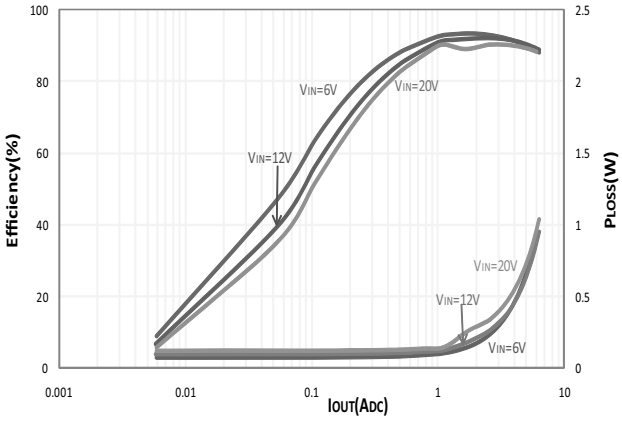
V_{OUT} vs. Line-Forced Continuous Mode
V_{OUT} = 1.5 V, V_{LDO} = V_{DD} = ENL = 5 V, EN/PSV is Floating, SiC403B



Frequency vs. Line-FCM Mode
V_{OUT} = 1.5 V, V_{LDO} = V_{DD} = ENL = 5 V, EN/PSV is Floating, SiC403B



On Time vs. Line
V_{OUT} = 1.5 V, V_{LDO} = V_{DD} = ENL = 5 V, I_{OUT} = 0 A, SiC403B



Efficiency vs. Load-Forced Continuous Mode
V_{OUT} = 1.2 V, V_{DD} = 5 V, EN/PSV is Floating, External Bias, SiC403A

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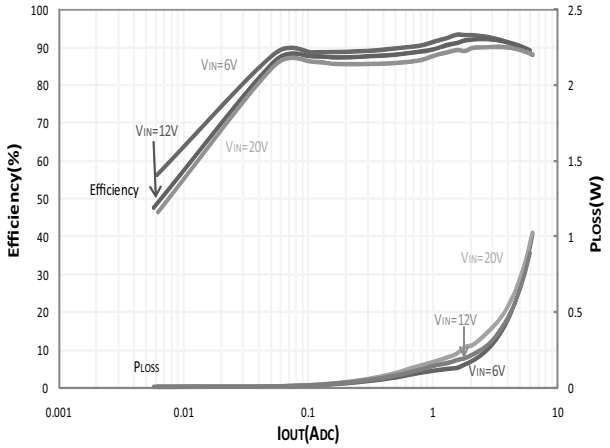
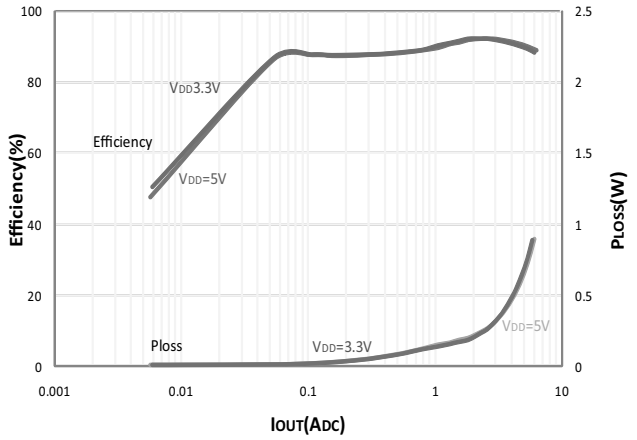
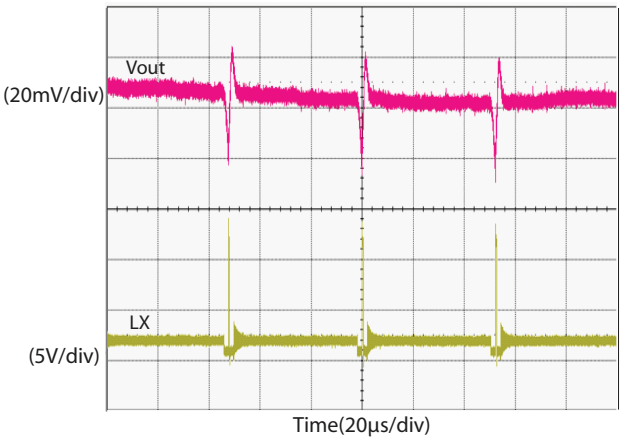


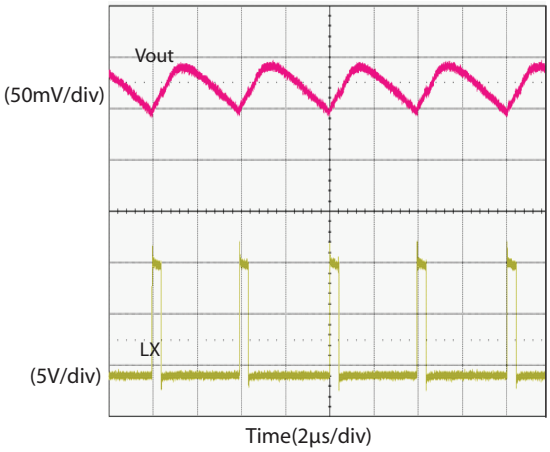
Efficiency vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{DD} = 5 V = EN/PSV, External Bias, SiC403A



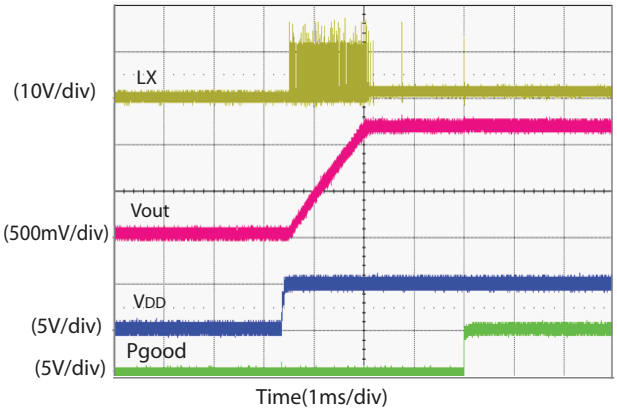
Efficiency vs. Load-PSAVE Mode
V_{OUT} = 1.2 V, V_{IN} = 12 V, V_{DD} = EN/PSV = 5 V, External Bias, SiC403A



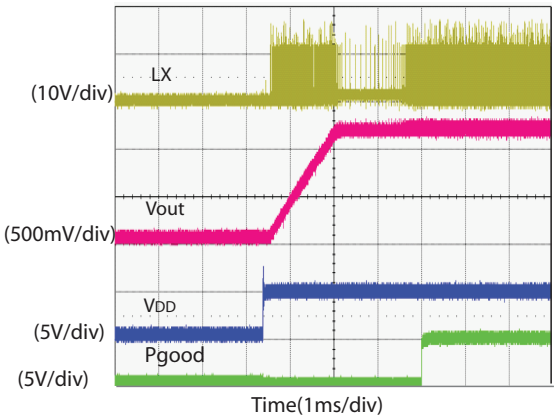
Powersave Mode - No Load
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, V_{DD} = EN/PSV = ENL = 5 V, SiC403A



Forced Continuous Mode - No Load
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, V_{DD} = EN/PSV = ENL = 5 V



Self-Biased Start-Up - Power Good True
V_{IN} = 12 V step, V_{OUT} = 1.2 V, I_{OUT} = 0 A, V_{DD} = EN/PSV = ENL = 5 V



Enable Start-Up - Power Good True
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 1 A, V_{DD} = EN/PSV= 5 V

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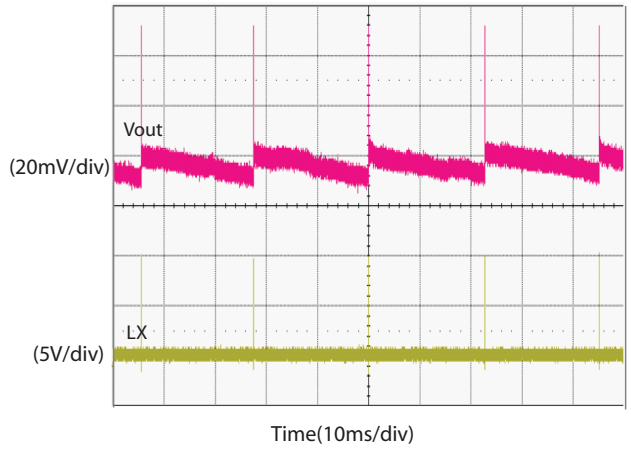
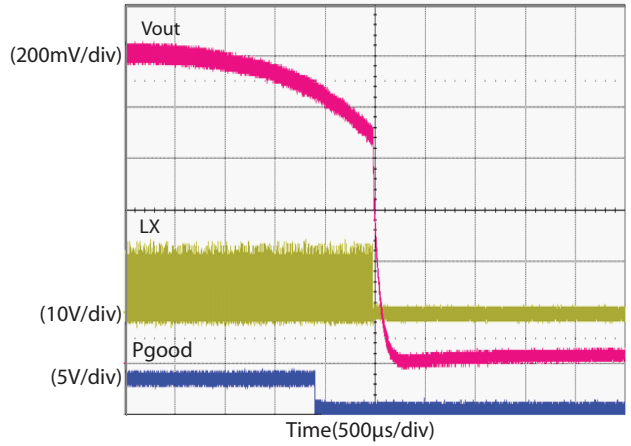
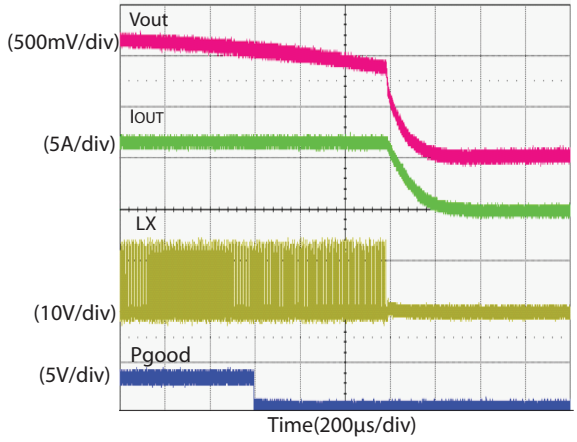


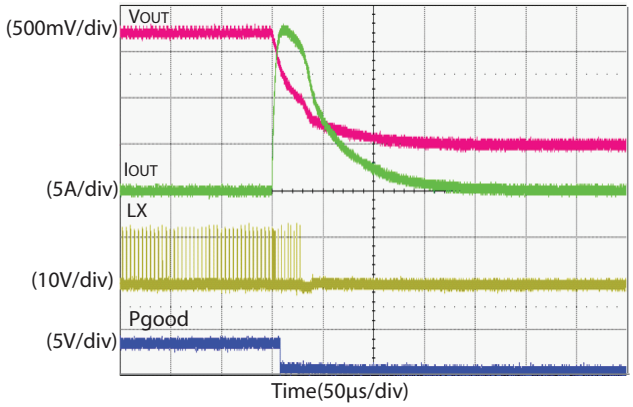
Powersave Mode - No Load
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, V_{DD} = EN/PSV = ENL = 5 V, SiC403B



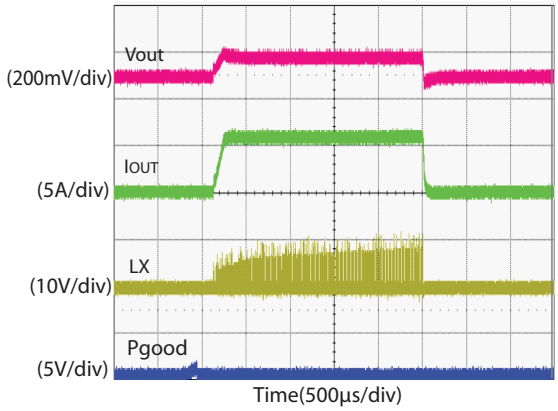
Output Under-Voltage Response
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, V_{DD} = ENL = 3.3 V, EN/PSV is floating



Output Over-Current Response
V_{IN} = 12 V, V_{OUT} = 1.2 V, V_{DD} = ENL = 3.3 V, EN/PSV is floating



Short Output Response
V_{IN} = 12 V, V_{OUT} = 1.2 V, V_{DD} = ENL = 3.3 V, EN/PSV is floating



Shorted Output Response at Soft-Start Operation
V_{IN} = 12 V, V_{OUT} = 1.2 V, V_{DD} = ENL = 3.3 V, EN/PSV is floating

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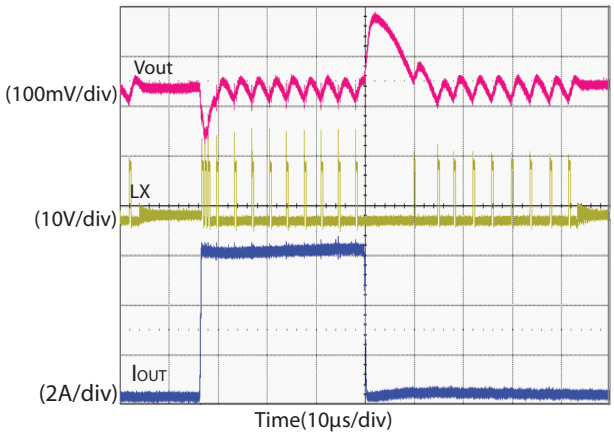
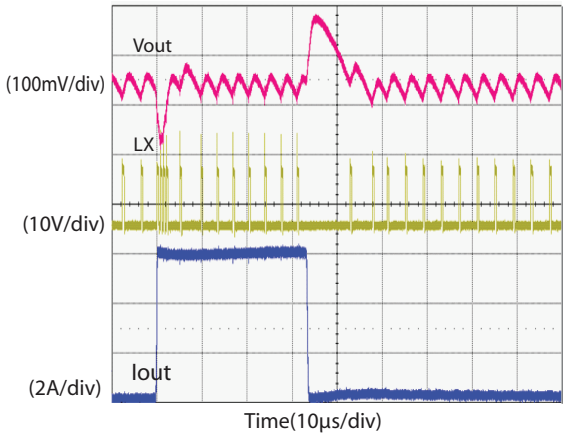


Transient Response in Power Saving Mode
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A to 6 A, V_{DD} = EN/PSV = 5 V



Transient Response in Forced Continuous Mode
V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A to 6 A, V_{DD} = EN/PSV = 5 V

OPERATIONAL DESCRIPTION

Device Overview

The SiC403A/B is a step down synchronous DC/DC buck converter with integrated power MOSFETs and a 200 mA capable programmable LDO. The device is capable of 6 A operation at very high efficiency. A space saving 5 x 5 (mm) 32-pin package is used. The programmable operating frequency of up to 1 MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This control method allows fast transient igponse which permits the use of smaller output capacitors.

Input Voltage Requirements

The SiC403A/B requires two input supplies for normal operation: V_{IN} and V_{DD}. V_{IN} operates over a wide range from 3 V to 28 V. V_{DD} requires a 3 V to 5.5 V supply input that can be an external source or the internal LDO configured to supply 3 V to 5.5 V from V_{IN}.

Power Up Sequence

When the SiC403A/B uses an external power source at the V_{DD} pin, the switching regulator initiates the start up when V_{IN}, V_{DD}, and EN/PSV are above their respective thresholds. When EN/PSV is at logic high, V_{DD} needs to be applied after V_{IN} rises. It is also recommended to use a 10 Ω resistor between an external power source and the V_{DD} pin. To start up by using the EN/PSV pin when both V_{DD} and V_{IN} are above their respective thresholds, apply EN/PSV to enable the start-up process. For SiC403A/B in self-biased mode, refer to the LDO section for a full description.

Shutdown

The SiC403A/B can be shut-down by pulling either V_{DD} or EN/PSV below its threshold. When using an external power source, it is recommended that the V_{DD} voltage ramps down before the V_{IN} voltage. When V_{DD} is active and EN/PSV at logic low, the output voltage discharges into the V_{OUT} pin through an internal FET.

Pseudo-Fixed Frequency Adaptive On-Time Control

The PWM control method used by the SiC403A/B is pseudo- fixed frequency, adaptive on-time, as shown in Fig. 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

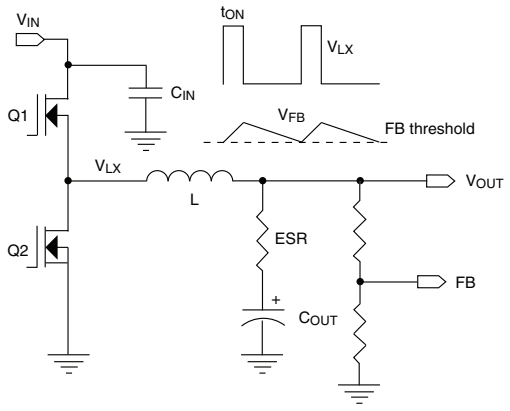


Fig. 1 - Output Ripple and PWM Control Method

The adaptive on-time is determined by an internal one- shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high- side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

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The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response - the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response.

One-Shot Timer and Operating Frequency

The one-shot timer operates as shown in Fig. 2. The FB comparator output goes high when V_{FB} is less than the internal 600 mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

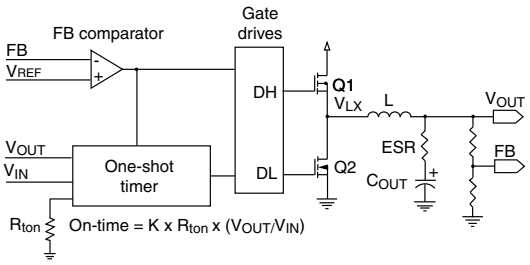

Fig. 2 - On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{t_{ON} \times V_{IN}}$$

The SiC403A/B uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency from 200 kHz to 1 MHz using a resistor between the t_{ON} pin and ground. The resistor value is selected by the following equation.

$$R_{ton} = \frac{k}{25\ pF \times f_{SW}}$$

The constant, k, equals 1, when V_{DD} is greater than 3.6 V. If V_{DD} is less than 3.6 V and V_{IN} is greater than (V_{DD} -1.75) x 10, k is shown by the following equation.

$$k = \frac{(V_{DD} - 1.75) \times 10}{V_{IN}}$$

The maximum R_{tON} value allowed is shown by the following equation

$$R_{ton} = \frac{(t_{on} - 10\ ns) \times V_{IN}}{25\ pF \times V_{OUT}}$$

Immediately after the on-time, the DL (drive signal for the low side FET) output drives high to turn on the low-side MOSFET. DL has a minimum high time of ~320 ns, after which DL continues to stay high until one of the following occurs:

- V_{FB} falls below the reference
- The zero cross detector senses that the voltage on the LX node is below ground. Power save is activated eight switching cycles after a zero crossing is detected.

t_{ON} Limitations and V_{DD} Supply Voltage

For V_{DD} below 4.5 V, the t_{ON} accuracy may be limited by the input voltage.

The original R_{tON} equation is accurate if V_{IN} satisfies the relationship over the entire V_{IN} range, as follows.

$V_{IN} < (V_{DD} - 1.6\ V) \times 10$

If V_{IN} exceeds (V_{DD} - 1.6 V) x 10, for all or part of the V_{IN} range, the R_{tON} equation is not accurate. In all cases where $V_{IN} > (V_{DD} - 1.6\ V) \times 10$, the R_{tON} equation must be modified, as follows.

$$R_{ton} = \frac{(t_{on} - 10\ ns) \times (V_{DD} - 1.6\ V) \times 10}{25\ pF \times V_{OUT}}$$

Note that when $V_{IN} > (V_{DD} - 1.6\ V) \times 10$, the actual on-time is fixed and does not vary with V_{IN}. When operating in this condition, the switching frequency will vary inversely with V_{IN} rather than approximating a fixed frequency.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 600 mV reference voltage, see Fig. 3.

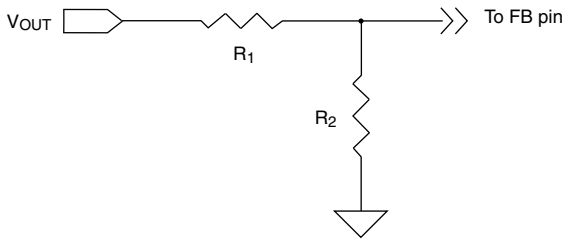

Fig. 3 - Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC output voltage V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

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When a large capacitor is placed in parallel with R_1 (C_{TOP}) V_{OUT} is shown by the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

Enable and Power-Save Inputs

The EN/PSV input is used to enable or disable the switching regulator. When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15 Ω internal resistor via the V_{OUT} pin. When EN/PSV is allowed to float, the pin voltage will float to 33 % of the voltage at V_{DD}. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 44 % of the voltage at V_{DD}), the switching regulator turns on with power-save enabled. The SiC403A/B P-Save operation reduces the switching frequency according to the load for increased efficiency at light load conditions.

Forced Continuous Mode Operation

The SiC403A/B operates the switcher in FCM (forced continuous mode) by floating the EN/PSV pin (see Fig. 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs. DH is gate signal to drive upper MOSFET. DL is lower gate signal to drive lower MOSFET.

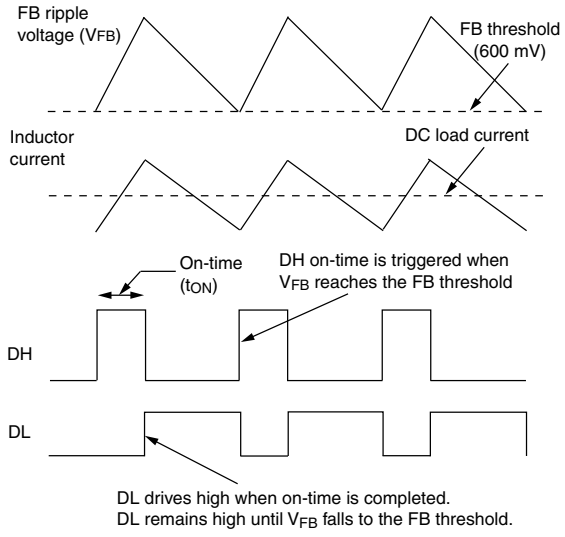

Fig. 4 - Forced Continuous Mode Operation

Ultrasonic Power-Save Operation (SiC403A)

The SiC403A provides ultrasonic power-save operation at light loads, with the minimum operating frequency fixed at slightly under 25 kHz. This is accomplished by using an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds 40 µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 600 mV threshold, the next DH (the drive signal for the high side FET) on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

Because the on-times are forced to occur at intervals no greater than 40 µs, the frequency will not fall far below 25 kHz. Fig. 5 shows ultrasonic power-save operation.

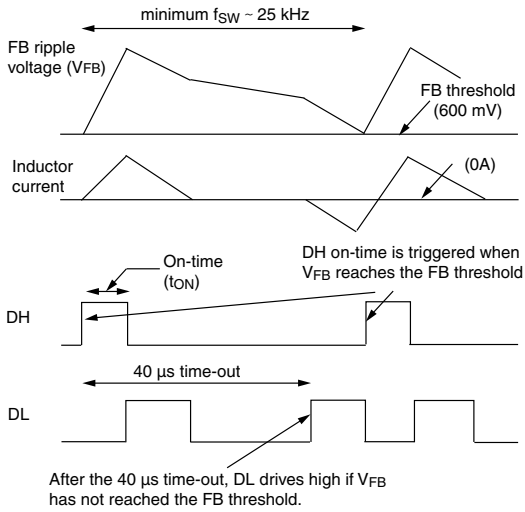

Fig. 5 - Ultrasonic Power-Save Operation

Power-Save Operation (SiC403B)

The SiC403B provides power-save operation at light loads with no minimum operating frequency. With power-save enabled, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters MOSFET on each subsequent cycle provided that the power-save operation. It will turn off the low-side MOSFET on each subsequent cycle provided that the current crosses zero. At this time both MOSFETs remain off until V_{FB} drops to the 600 mV threshold. Because the MOSFETs are off, the load is supplied by the output capacitor.

If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode.

Fig. 6 shows power-save operation at light loads.

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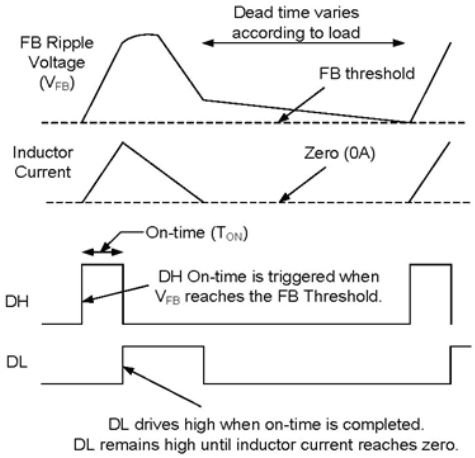

Fig. 6 - Power-Save Mode

Smart Power-Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shut-down. Smart power-save prevents this condition. When the FB voltage exceeds 10 % above nominal, the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 600 mV trip point, a normal t_{ON} switching cycle begins. This method prevents a hard OVP shut-down and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Fig. 7 shows typical waveforms for the Smart Power Save feature.

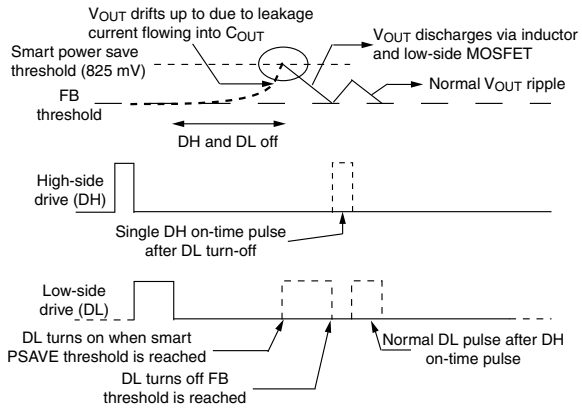

Fig. 7 - Smart Power-Save

SmartDrive™

For each DH pulse, the DH driver initially turns on the high side MOSFET at a lower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5 V above P_{GND}, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching losses while maintaining high efficiency and also avoids the need for snubbers for the power MOSFETs.

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the $R_{DS\text{-}on}$ of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the I_{LIM} pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~ 10 µA current flows from the I_{LIM} pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $R_{DS\text{-}on}$. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the I_{LIM} pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the I_{LIM} voltage back up to zero. This method regulates the inductor valley current at the level shown by I_{LIM} in Fig. 8.

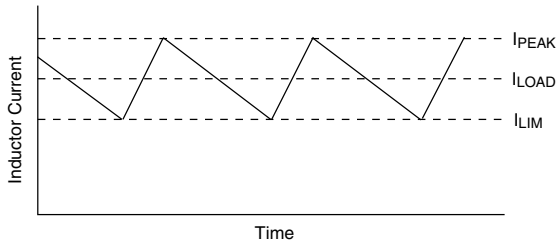

Fig. 8 - Valley Current Limit

Setting the valley current limit to 6 A results in a peak inductor current of 6 A plus peak ripple current. In this situation, the average (load) current through the inductor is 6 A plus one-half the peak-to-peak ripple current.

The internal 10 µA current source is temperature compensated at 4100 ppm in order to provide tracking with the $R_{DS\text{-}on}$.

The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 792 \times I_{LIM} \times [0.101 \times (5\ V - V_{DD}) + 1]$$

When selecting a value for R_{ILIM} be sure not to exceed the absolute maximum voltage value for the I_{LIM} pin. Note that because the low-side MOSFET with low $R_{DS\text{-}on}$ is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 28).

Soft-Start of PWM Regulator

SiC403A/B has a programmable soft-start time that is controlled by an external capacitor at the SS pin. After the controller meets both UVLO and EN/PSV thresholds, the controller has an internal current source of 3 µA flowing through the SS pin to charge the capacitor. During the start

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up process (Fig. 9), 50 % of the voltage at the SS pin is used as the reference for the FB comparator. The PWM comparator issues an on-time pulse when the voltage at the FB pin is less than 40 % of the SS pin. As a result, the output voltage follows the SS voltage. The output voltage reaches and maintains regulation when the soft start voltage is ≥1.5 V. The time between the first LX pulse and V_{OUT} reaching regulation is the soft-start time (t_{SS}). The calculation for the soft-start time is shown by the following equation.

$$t_{SS} = C_{SS} \times \frac{1.5\ V}{3\ \mu A}$$

The voltage at the SS pin continues to ramp up and eventually equals 64 % of V_{DD}. After the soft start completes, the FB pin voltage is compared to an internal reference of 0.6 V. The delay time between the V_{OUT} regulation point and P_{GOOD} going high is shown by the following equation.

$$t_{PGOOD\text{-}DELAY} = \frac{C_{SS} \times (0.64 \times V_{DD} - 1.5\ V)}{3\ \mu A}$$

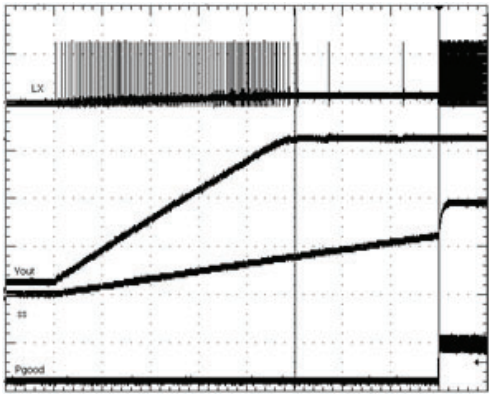

Fig. 9 - Soft-start Timing Diagram

Pre-Bias Start-Up

The SiC403A/B can start up normally even when there is an existing output voltage present. The soft start time is still the same as normal start up (when the output voltage starts from zero). The output voltage starts to ramp up when 40 % of the voltage at SS pin meets the existing FB voltage level. Pre-bias startup is achieved by turning off the lower gate when the inductor current falls below zero. This method prevents the output voltage from discharging.

Power Good Output

The P_{GOOD} (power good) output is an open-drain output which requires a pull-up resistor. When the voltage at the FB pin is 10 % below the nominal voltage, P_{GOOD} is pulled low. It is held low until the output voltage returns above -8 % of nominal.

P_{GOOD} will transition low if the V_{FB} pin exceeds +20 % of nominal, which is also the over-voltage shutdown threshold.

P_{GOOD} also pulls low if the EN/PSV pin is low when V_{DD} is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 600 mV + 20 % (720 mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off, until the EN/PSV input is toggled or V_{DD} is cycled. There is a 5 µs delay built into the OVP detector to prevent false transitions. P_{GOOD} is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25 % below its nominal voltage (falls to 450 mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tristate the MOSFETs. The controller stays off until EN/PSV is toggled or V_{DD} is cycled.

V_{DD} UVLO, and POR

UVLO (Under-Voltage Lock-Out) circuitry inhibits switching and tri-states the DH/DL drivers until V_{DD} rises above 3 V. An internal POR (Power-On Reset) occurs when V_{DD} exceeds 3 V, which resets the fault latch and a soft-start counter cycle begins which prepares for soft-start. The SiC403A/B then begins a soft-start cycle. The PWM will shut off if V_{DD} falls below 2.4 V.

LDO Regulator

SiC403A/B has an option to bias the switcher by using an internal LDO from V_{IN}. The LDO output is connected to V_{DD} internally. The output of the LDO is programmable by using external resistors from the V_{DD} pin to A_{GND} (see Fig. 10). The feedback pin (FBL) for the LDO is regulated to 750 mV.

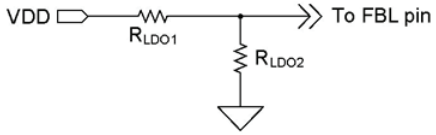

Fig. 10 - LDO Output Voltage Selection

The LDO output voltage is set by the following equation.

$$V_{LDO} = 750\ mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum capacitance of 1 µF referenced to A_{GND} is normally required at the output of the LDO for stability.

Note that if the LDO voltage is set lower than 4.5 V, the minimum output capacitance for the LDO is 10 µF.

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LDO ENL Functions

The ENL input is used to enable/disable the internal LDO. When ENL is a logic low, the LDO is off. When ENL is above the V_{IN} UVLO threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV and V_{DD} are above their threshold. The table below summarizes the function of ENL and EN/PSV pins.

EN/PSV	ENL	LDO	SWITCHER
Disabled	Low, < 0.4 V	Off	Off
Enabled	Low, < 0.4 V	Off	On
Disabled	1 V < high < 2.6 V	On	Off
Enabled	1 V < high < 2.6 V	On	Off
Disabled	High, > 2.6 V	On	Off
Enabled	High, > 2.6 V	On	On

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. When SiC403A/B is self-biased from the LDO and runs from the V_{IN} power source only, the V_{IN} UVLO feature can be used to prevent false UV faults for the PWM output by programming with a resistor divider at the V_{IN}, ENL and A_{GND} pins. When SiC403A/B has an external bias voltage at V_{DD} and the ENL pin is used to program the V_{IN} UVLO feature, the voltage at FBL needs to be higher than 750 mV to force the LDO off.

Timing is important when driving ENL with logic and not implementing V_{IN} UVLO. The ENL pin must transition from high to low within 2 switching cycles to avoid the PWM output turning off. If ENL goes below the V_{IN} UVLO threshold and stays above 1 V, then the switcher will turn off but the LDO will remain on.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. V_{LDO} output

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the V_{DD} voltage (which is the LDO output voltage) is less than 0.75 V, the LDO initiates a current-limited start-up (typically 65 mA) to charge the output capacitors while protecting from a short circuit event. When V_{DD} is greater than 0.75 V but still less than 90 % of its final value (as sensed at the FBL pin), the LDO current limit is increased to ~115 mA. When V_{DD} has reached 90 % of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~200 mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator. It is recommended that during LDO start-up to hold the PWM switching off until the LDO has reached 90 % of the final value. This prevents overloading the current-limited LDO output during the LDO start-up.

Due to the initial current limitations on the LDO during power up (Fig. 11), any external load attached to the V_{DD} pin must be limited to less than the start up current before the LDO has reached 90 % of its final regulation value.

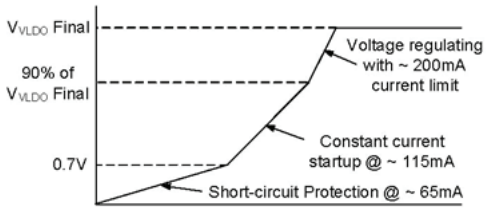

Fig. 11 - LDO Start-Up

LDO Switch-Over Operation

The SiC403A/B includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient DC/DC converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the V_{DD} pin directly to the V_{OUT} pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SiC403A/B, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over starts 32 switching cycles after P_{GOOD} output goes high. The voltages at the V_{DD} and V_{OUT} pins are then compared; if the two voltages are within ± 300 mV of each other, the V_{DD} pin connects to the V_{OUT} pin using an internal switch, and the LDO is turned off. To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{DD} should be ± 500 mV.

It is not recommended to use the switch-over feature for an output voltage less than V_{DD} UVLO threshold since the SiC403A/B is not operational below that threshold.

Switch-Over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in Fig. 12. If the voltage at the V_{OUT} pin is higher than V_{DD}, then the respective diode will turn on and the current will flow through this diode. This has the potential of damaging the device. Therefore, V_{OUT} must be less than V_{DD} to prevent damaging the device.

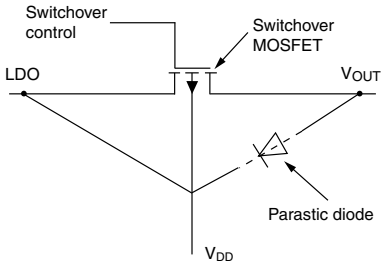

Fig. 12 - Switch-over MOSFET Parasitic Diodes

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Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage ($V_{IN\ max.}$) is the highest specified input voltage. The minimum input voltage ($V_{IN\ min.}$) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design:

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate - continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design:

- V_{IN} = 12 V ± 10 %
- V_{OUT} = 1.5 V ± 4 %
- f_{SW} = 300 kHz
- Load = 6 A max.

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 300 kHz which results from using component selected for optimum size and cost.

A resistor (R_{tON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{ton} = \frac{(t_{on} - 10\ ns) \times V_{IN}}{25\ pF \times V_{OUT}}$$

To select R_{tON}, use the maximum value for V_{IN}, and for t_{ON} use the value associated with maximum V_{IN}.

$$t_{ON} = \frac{V_{OUT}}{V_{INmax.} \times f_{SW}}$$

Substituting for R_{tON} results in the following solution.

R_{tON} = 129.9 kΩ, use R_{tON} = 130 kΩ.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for P_{Save} operation. The switching will typically enter P_{Save} mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4 A then P_{Save} operation will typically start for loads less than 2 A. If ripple current is set at 40 % of maximum load current, then P_{Save} will start for loads less than 20 % of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50 % of the maximum load current. Thus ripple current will be 50 % x 6 A or 3 A. To find the minimum inductance needed, use the V_{IN} and t_{ON} values that correspond to $V_{INmax.}$.

$$L = \frac{(13.2 - 1.5) \times 379\ ns}{3\ A} = 1.48\ \mu H$$

A slightly larger value of 1.5 µH is selected. This will decrease the maximum I_{RIPPLE} to 2.7 A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$t_{ON_VINmin.} = \frac{25\ pF \times R_{tON} \times V_{OUT}}{V_{INmin.}} + 10\ ns = 461\ ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L}$$

$$I_{RIPPLE_min.} = \frac{(10.8\ V - 1.5\ V) \times 461\ ns}{1.5\ \mu H \times (1 + 0.2)} = 2.38\ A$$

$$I_{RIPPLE_max.} = \frac{(10.8\ V - 1.5\ V) \times 379\ ns}{1.5\ \mu H \times (1 - 0.2)} = 3.7\ A$$

Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple.

A change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal for output voltage ripple is 4 % of 1.5 V or 60 mV. The maximum ESR value allowed is shown by the following equations.

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$$ESR_{max.} = \frac{V_{RIPPLE}}{I_{RIPPLEmax.}} = \frac{60\ mV}{3.7\ A}$$

$$ESR_{max.} = 16.2\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1 µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$C_{OUT_min.} = \frac{L\ (I_{OUT} + \frac{1}{2} x\ I_{RIPPLEmax.})^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.6 V (150 mV rise upon load release), and a 6 A load release, the required capacitance is shown by the next equation.

$$C_{OUT_min.} = \frac{1.5\ \mu H\ x\ (6 + \frac{1}{2}\ x\ 3.7)^2}{(1.6)^2 - (1.5)^2}$$

$$C_{OUT_min.} = 298\ \mu F$$

During the load release time, the voltage cross the inductor is approximately - V_{OUT}. This causes a down-slope or falling di/dt in the inductor. If the load dI/dt is not much faster than the dI/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor; therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

$I_{LPK} = I_{max.} + 1/2 \times I_{RIPPLEmax.}$

$I_{LPK} = 6 + 1/2 \times 3.7 = 7.9\ A$

$$\text{Rate of change of load current} = \frac{dI_{LOAD}}{dt}$$

$I_{max.}$ = maximum load release = 6 A

$$C_{OUT} = I_{LPK} x \frac{L x \frac{I_{LPK}}{V_{OUT}} - \frac{I_{max.}}{dI_{LOAD}} x\ dt}{2\ (V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2\ A}{1\ \mu s}$$

This would cause the output current to move from 6 A to 0 A in 3 µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 7.9 x \frac{1.5\ \mu H\ x\ \frac{7.9}{1.5} - \frac{6}{2}\ x\ 1\ \mu s}{2\ (1.6 - 1.5)}$$

$$C_{OUT} = 194\ \mu F$$

Note that C_{OUT} is much smaller in this example, 194 µF compared to 298 µF based on a worst case load release. To meet the two design criteria of minimum 298 µF and maximum 16 mΩ ESR, select one capacitor of 330 µF and 9 mΩ ESR.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250 ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10 mV_{p-p}, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small (~10 pF) capacitor across the upper feedback resistor, as shown in Fig. 13. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

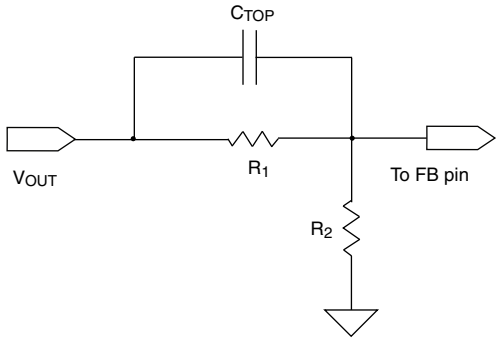

Fig. 13 - Capacitor Coupling to FB P_{IN}

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

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ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10 mV_{p-p} at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{min.} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{SW}}$$

Using Ceramic Output Capacitors

When the system is using high ESR value capacitors, the feedback voltage ripple lags the phase node voltage by 90°. Therefore, the converter is easily stabilized. When the system is using ceramic output capacitors, the ESR value is normally too small to meet the above ESR criteria. As a result, the feedback voltage ripple is 180° from the phase node and behaves in an unstable manner. In this application it is necessary to add a small virtual ESR network that is composed of two capacitors and one resistor, as shown in Fig. 14.

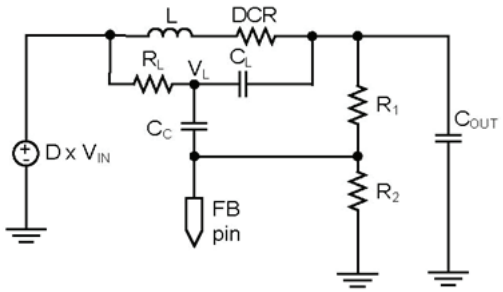

Fig. 14 - Virtual ESR Ramp Current

The ripple voltage at FB is a superposition of two voltage sources: the voltage across C_L and output ripple voltage.

They are defined in the following equations.

$$V_{CL} = \frac{I_L \times DCR\ (s \times L/DCR + 1)}{S \times R_L \times C_L + 1}$$

$$\Delta V_{OUT} = \frac{\Delta I_L}{8C \times f_{SW}}$$

Fig. 15 shows the magnitude of the ripple contribution due to C_L at the FB pin.

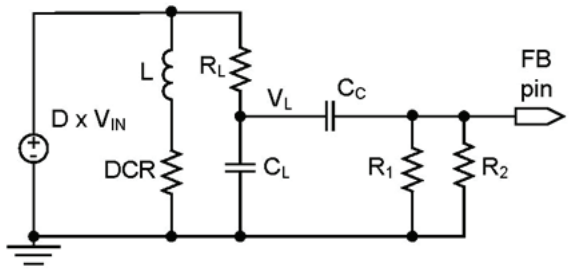

Fig. 15 - FB Voltage by CL Voltage

It is shown by the following equation.

$$VFB_{CL} = V_{CL} \times \frac{(R_1//R_2) \times S \times C_C}{(R_1//R_2) \times S \times C_C + 1}$$

It is recommended that R_2 be set to 1K.

Fig. 16 shows the magnitude of the ripple contribution due to the output voltage ripple at the FB pin.

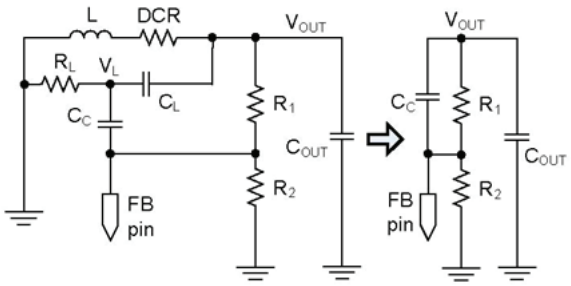

Fig. 16 - FB Voltage by Output Voltage

It is shown by the following equation.

$$V_{FB}\Delta V_{OUT} = \Delta V_{OUT} \times \frac{R_2}{R_1//\frac{1}{S \times C_C} + R_2}$$

The purpose of this network is to couple the inductor current ripple information into the feedback voltage such that the feedback voltage has 90° phase lag to the switching node similar to the case of using standard high ESR capacitors. This is illustrated in Fig. 17.

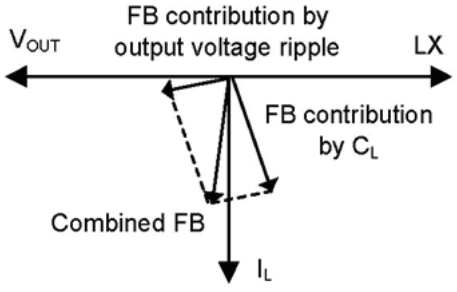

Fig. 17 - FB Voltage in Phasor Diagram

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The magnitude of the feedback ripple voltage, which is dominated by the contribution from C_L, is controlled by the value of R_1, R_2 and C_C. If the corner frequency of (R_1//R_2) x C_C is too high, the ripple magnitude at the FB pin will be smaller, which can lead to double-pulsing. Conversely, if the corner frequency of (R_1//R_2) x C_C is too low, the ripple magnitude at FB pin will be higher. Since the SiC403A/B regulates to the valley of the ripple voltage at the FB pin, a high ripple magnitude is undesirable as it significantly impacts the output voltage regulation. As a result, it is desirable to select a corner frequency for (R_1//R_2) x C_C to achieve enough, but not excessive, ripple magnitude and phase margin. The component values for R_1, R_2, and C_C should be calculated using the following procedure.

Select C_L (typical 10 nF) and R_L to match with L and DCR time constant using the following equation.

$$R_L = \frac{L}{DCR \times C_L}$$

Select C_C by using the following equation.

$$C_C \approx \frac{1}{R_1//R_2} \times \frac{3}{2 \times \pi \times f_{SW}}$$

The resistor values (R_1 and R_2) in the voltage divider circuit set the V_{OUT} for the switcher. The typical value for CC is from 10 pF to 1 nF.

Dropout Performance

The output voltage adjustment range for continuous conduction operation is limited by the fixed 250 ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{t_{ON(min.)}}{t_{ON(min.)} \times t_{OFF(max.)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 600 mV, 1 %.

The on-time pulse from the SiC403A/B in the design example is calculated to give a pseudo-fixed frequency of 300 kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50 mV with V_{IN} = 6 V, then the measured DC output will be 25 mV above the comparator trip point.

If the ripple increases to 80 mV with V_{IN} = 28 V, then the measured DC output will be 40 mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

The use of 1 % feedback resistors may result in up to 1 % error. If tighter DC accuracy is required, 0.1 % resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variation

The switching frequency varies with load current as a result of the power losses in the MOSFETs and DCR of the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. An adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the offtime will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

HIGH OUTPUT VOLTAGE OPERATION

For the SiC40X family the recommended maximum output voltage of no more than 75 % of V_{IN}.

For applications where an output voltage greater than 5 V is required a resistive network should be used to step down the output voltage in order to provide the V_{OUT_PIN} with 4.5 V.

$$R_1 = \frac{R_2 (V_{OUT} - V_{OUT_PIN})}{V_{OUT_PIN}}$$

For example, if an output voltage of V_{OUT} = 8.5 V is required, setting R_2 = 10 kΩ and V_{OUT_PIN} = 4.5 V results in R_1 = 8870 Ω.

The switching frequency will also need recalculating using a V_{OUT_PIN} magnitude of 4.5 V.

$$f_{sw} = \frac{V_{OUT_PIN}}{t_{ON} \times V_{IN}}$$

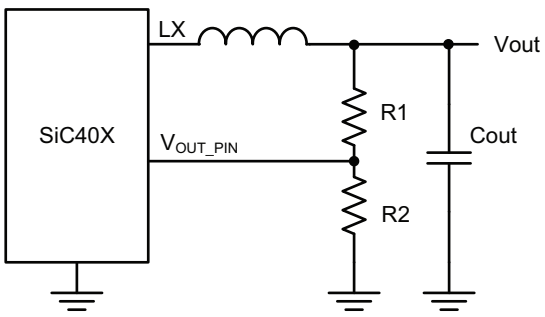

Fig. 18 - Resistor Divider Network allows 4.5 V at the V_{OUT} Pin

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LAYOUT CONSIDERATIONS

The SiC40x family of footprint compatible 15 A, 10 A, and 6 A products offers the designer a scalable buck regulator solution. If the below layout recommendations are followed, the same layout can be used to cover a wide range of output currents and voltages without any changes to the board design and only minor changes to the component values in the schematic.

The reference design has a majority of the components placed on the top layer. This allows for easy assembly and straightforward layout.

Fig. 19 outlines the pointers for the layout considerations and the explanations follow.

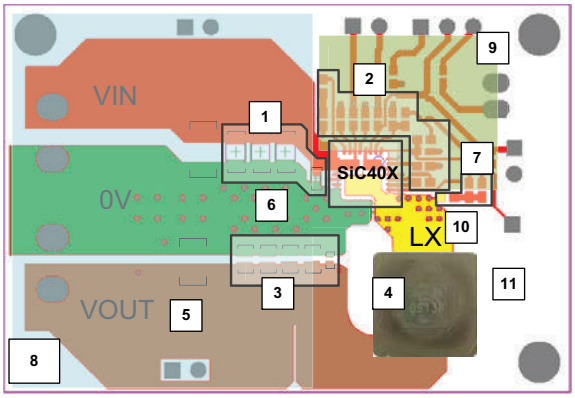

Fig. 19 - Reference Design Pointers

1. Place input ceramic capacitors close to the voltage input pins with a small 10 nF/100 nF placed as close as the design rules will allow. This will help reduce the size of the input high frequency current loop and consequently reduce the high frequency ripple noise seen at the input and the LX node.
2. Place the setup and control passive devices logically around the IC with the intention of placing a quiet ground plane beneath them on a secondary layer.
3. It is advisable to use ceramic capacitors at the output to reduce impedance. Place these as close to the IC P_{GND} and output voltage node as design will allow. Place a small 10 nF/100 nF ceramic capacitor closest to the IC and inductor loop.
4. The loop between LX, V_{OUT} and the IC GND should be as compact as possible. This will lower series resistance and also make the current loop smaller enabling the high frequency response of the output capacitors to take effect.
5. The output impedance should be small when high current is required; use high current traces, multiple layers can be used with many vias.
6. Use many vias when multiple layers are involved. This will have the effect of lowering the resistance between layers and reducing the via inductance of the PCB nets.
7. If a voltage injection network is needed then place it near to the inductor LX node.
8. P_{GND} can be used on internal layers if the resistance of the PCB is to be small; this will also help remove heat. Use extra vias if needed but be mindful to allow a path between the vias.
9. A quiet plane should be employed for the A_{GND}, this is placed under the small signal passives. This can be placed on multiple layers if needed for heat removal. This should be connected to the P_{GND} plane near to the input GND at one connection only of at least 1 mm width.
10. The LX copper can also be used on multiple layers, use a number of vias.
11. The copper area beneath the inductor has been removed (on all layers) in this design to reduce the inductive coupling that occurs between the inductor and the GND trace. No other voltage planes should be placed under this area.

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PCB LAYOUT

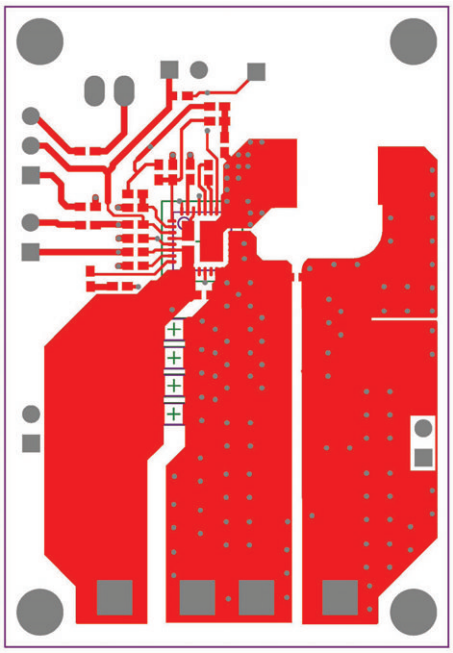

Fig. 20 - Top Layer

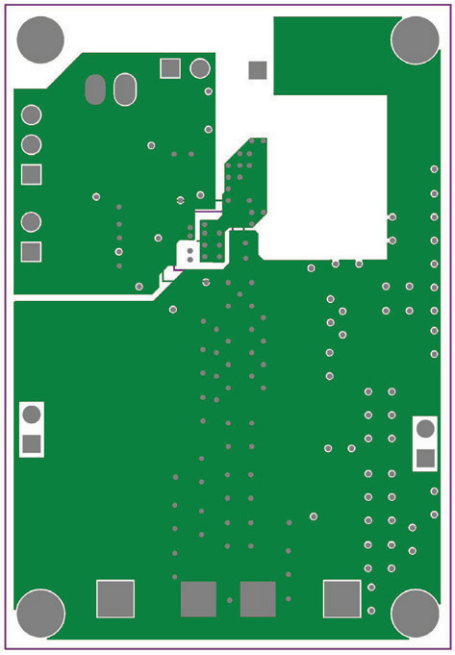

Fig. 22 - Inner Layer 2

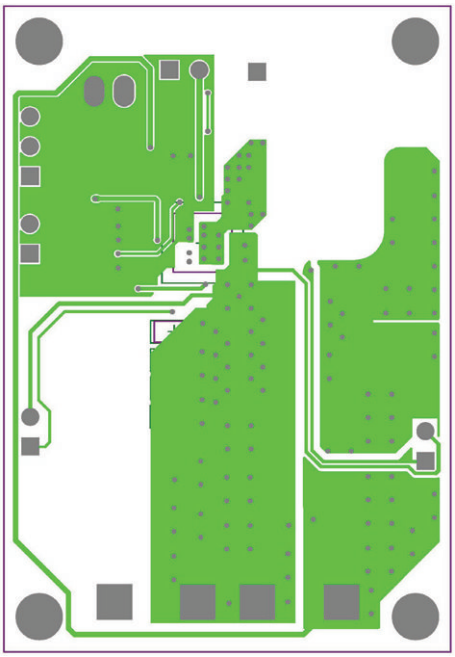

Fig. 21 - Inner Layer 1

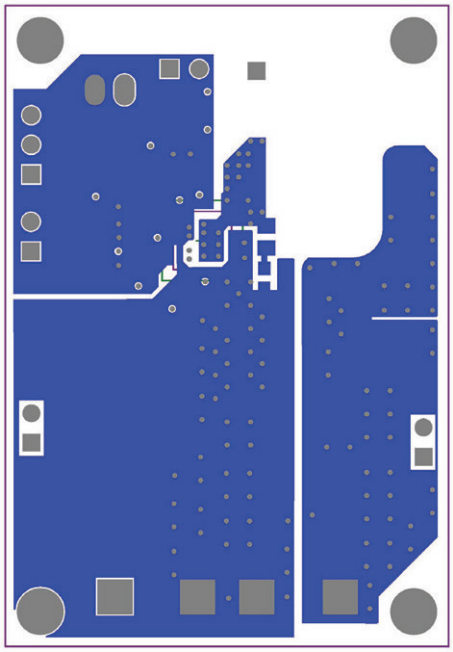

Fig. 23 - Bottom Layer

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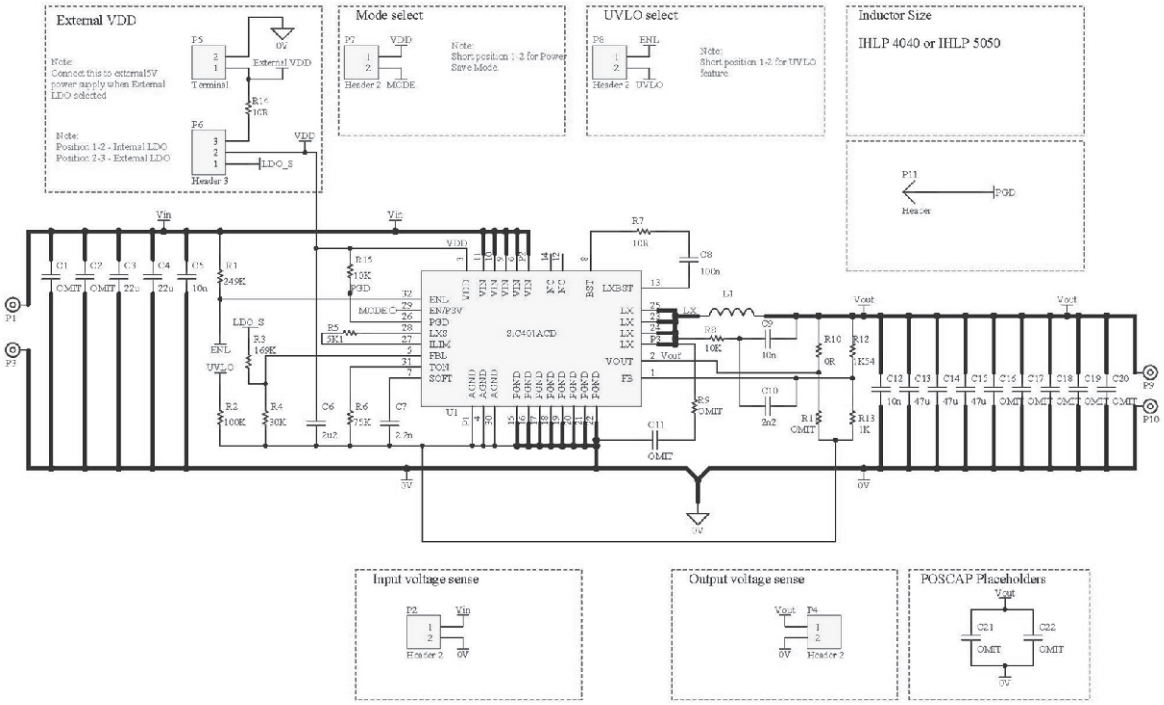
SCHEMATIC



Note

- If OUT voltage setting ≥ 5 V_{DC}, please change R10 and R11 value based on “High Output Voltage Operation” formula calculation

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BILL OF MATERIALS (V_{IN} = 12 V, V_{OUT} = 1.5 V, F_{sw} = 500 kHz)

ITEM	QTY	REFERENCE	PCB FOOTPRINT	VALUE	VOLTAGE	PART NUMBER	MANUFACTURER
1	3	C1, C2, C3	1206	Omit	35 V	C3216X5R1V226M160AC	TDK
2	1	C4	1206	22 µF	35 V	C3216X5R1V226M160AC	TDK
3	3	C5, C9, C12	0402	10 nF	50 V	GRM155R71H103KA88D	Murata
4	1	C6	0402	2.2 µF	10 V	C0402C225M8PACTU	Kemet
5	2	C7, C10	0402	1 nF	50 V	GRM155R71H102KA01D	Murata
6	1	C8	0402	100 nF	35 V	CGA2B3X7R1V104K050BB	Vishay
7	2	C13, C14	1206	47 µF	10 V	GRM31CR61A476ME15L	Murata
8	6	C15, C16, C17 C18, C19, C20	1206	Omit	10 V	GRM31CR61A476ME15L	Murate
9	2	C21, C22	7343	Omit	-	-	-
10	4	P1, P3, P9, P10	Banana Jack	-	-	575-4K-ND	Keystone
11	5	P2, P4, P5, P7, P8	Header-2	-	-	826926-2	AMP (TE)
12	1	P6	Header-3	-	-	HTSW-103-08-T-S	Samtec
13	1	L1	IHLP3232	2.2 µH	-	IHLP3232DZER2R2	Vishay
14	1	R1	0402	249K	-	CRCW0402249KFKED	Vishay
15	1	R2	0402	100K	-	CRCW0402100KFKED	Vishay
16	1	R3	0402	169K	-	CRCW0402169KFKED	Vishay
17	1	R4	0402	30K	-	CRCW040230K0FKED	Vishay
18	1	R5	0402	5K11	-	CRCW04025K11FKED	Vishay
19	1	R6	0402	76K8	-	CRCW040276K8FKED	Vishay
20	1	R7	0402	10R	-	CRCW040210R0FKEA	Vishay
21	1	R8	0402	10K	-	CRCW040210K0FKED	Vishay
22	1	R9	0805	Omit	-	-	Vishay
23	1	R10	0402	0R	-	CRCW04020000Z0ED	Vishay
24	1	R11	0402	Omit	-	-	Vishay
25	1	R12	0402	1K54	-	CRCW04021K54FKED	Vishay
26	1	R13	0402	1K	-	CRCW0402249KFKED	Vishay
27	1	R14	0402	10R	-	CRCW040210R0FKEA	Vishay
28	1	R15	0402	10K	-	CRCW040210K0FKED	Vishay
29	1	U1	MLP55-33	SIC403	-	-	-

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PRODUCT SUMMARY		
Part number	SiC403A	SiC403B
Description	6 A, 3 V to 28 V input, scalable synchronous buck regulator, ultrasonic mode	6 A, 3 V to 28 V input, scalable synchronous buck regulator, powersave mode
Input voltage min. (V)	3	3
Input voltage max. (V)	28	28
Output voltage min. (V)	0.6	0.6
Output voltage max. (V)	5.5	5.5
Continuous current (A)	6	6
Switch frequency min. (kHz)	200	200
Switch frequency max. (kHz)	1000	1000
Pre-bias operation (yes / no)	Yes	Yes
Internal bias reg. (yes / no)	Yes	Yes
Compensation	Not required	Not required
Enable (yes / no)	Yes	Yes
P_{GOOD} (yes / no)	Yes	Yes
Overcurrent protection	Programmable	Programmable
Protection	OVP, OCP, UVP/SCP, OTP, UVLO	OVP, OCP, UVP/SCP, OTP, UVLO
Light load mode	Ultrasonic	Powersave
Peak efficiency (%)	93	93
Package type	PowerPAK MLP32-55G	PowerPAK MLP32-55G
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.85	5 x 5 x 0.85
Status code	2	2
Product type	microBUCK (step down regulator)	microBUCK (step down regulator)
Applications	Computing, consumer, networking, industrial, healthcare	Computing, consumer, networking, industrial, healthcare

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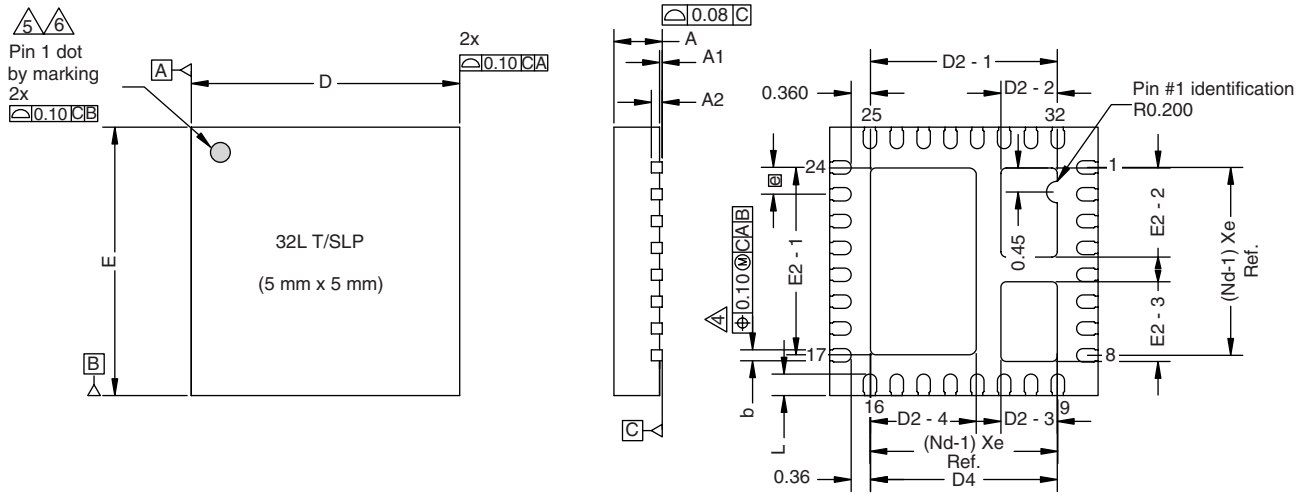
PowerPAK® MLP55-32L CASE OUTLINE



Top View Side View Bottom View

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1[8]	0.00	-	0.05	0.000	-	0.002
A2		0.20 REF.			0.008 REF.	
b[4]	0.20	0.25	0.30	0.078	0.098	0.011
D		5.00 BSC			0.196 BSC	
e		0.50 BSC			0.019 BSC	
E		5.00 BSC			0.196 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N[3]		32			32	
Nd[3]		8			8	
Ne[3]		8			8	
D2 - 1	3.43	3.48	3.53	0.135	0.137	0.139
D2 - 2	1.00	1.05	1.10	0.039	0.041	0.043
D2 - 3	1.00	1.05	1.10	0.039	0.041	0.043
D2 - 4	1.92	1.97	2.02	0.075	0.077	0.079
E2 - 1	3.43	3.48	3.53	0.135	0.137	0.139
E2 - 2	1.61	1.66	1.71	0.063	0.065	0.067
E2 - 3	1.43	1.48	1.53	0.056	0.058	0.060
ECN: T-08957-Rev. A, 29-Dec-08 DWG: 5983						

Notes

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

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