

Nonvolatile DACPOT™ Electronic Potentiometer With Up/Down Counter Interface

FEATURES

- Digitally Controlled Electronic Potentiometer
- 7-Bit Digital-to-Analog Converter (DAC)
 - Independent Reference Inputs
 - Differential Non-Linearity - $\pm 0.5\text{LSB}$
 - Integral Non-Linearity - $\pm 1\text{LSB}$
- V_{OUT} Value in EEPROM for Power-On Recall
 - Equivalent to 128-Step Potentiometer
- Unity Gain Op Amp Drives $\pm 100\mu\text{A}$
- Simple Trimming Adjustment
 - Up/Down Counter Style Operation
- Low Noise Operation
- “Clickless” Transitions between DAC Steps
- No Mechanical Wearout Problem
 - 1,000,000 Stores (typical)
 - 100 Year Data Retention
- Operation from +2.7V to +5.5V Supply
- Ultra-Low Power, 0.5mW max at +5V

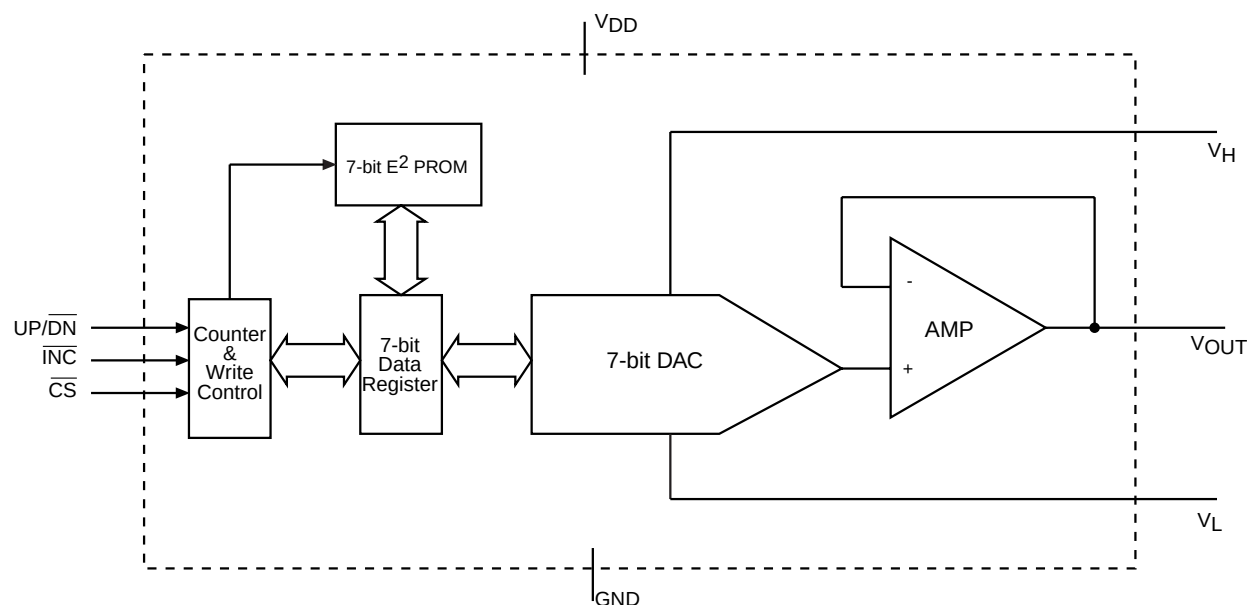
OVERVIEW

The SMP9317 DACPOT™ trimmer is a 7-bit nonvolatile DAC designed to replace mechanical potentiometers. The SMP9317 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The SMP9317's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the V_{OUT} voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The SMP9317 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The SMP9317 offers higher resolution than these devices and provides 'clickless' transitions of V_{OUT} .

FUNCTIONAL BLOCK DIAGRAM



2031 ILL2.0



PIN NAMES

Symbol	Description
$\overline{\text{INC}}$	Increment Input, High to Low Edge Trigger
$\text{UP}/\overline{\text{DN}}$	Up/Down Input controlling relative V_{OUT} movement
V_{H}	V+ reference input
GND	Analog and Digital Ground
V_{OUT}	Trimmed Voltage Output
V_{L}	V- reference input
$\overline{\text{CS}}$	Active low chip select input
V_{DD}	Supply Voltage (2.7V to 5.5V)

Analog Section

The SMP9317 is a 7-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts a 7-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_{L} and V_{H} inputs sets the full-scale output voltage range. V_{L} must be equal to or greater than ground (i.e. a positive voltage). V_{H} must be greater than V_{L} and less than or equal to V_{DD} . See table on page 3 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is from a precision unity-gain follower that can slew up to 1V/ μs .

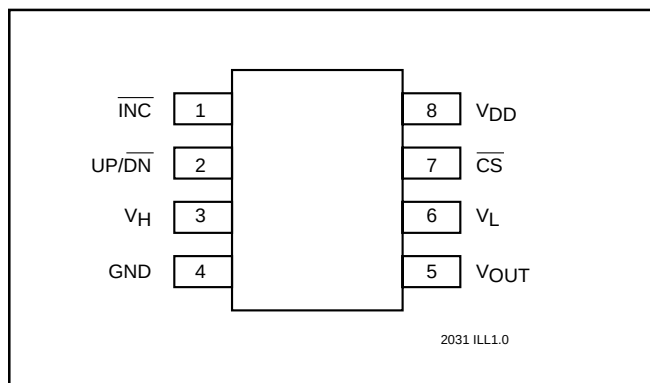
Digital Interface

The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

Chip Select ($\overline{\text{CS}}$) is an active low input. Whenever $\overline{\text{CS}}$ is high the SMP9317 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When $\overline{\text{CS}}$ is low the SMP9317 will recognize transitions on the $\overline{\text{INC}}$ input and will move the V_{OUT} either toward the V_{H} reference or toward the V_{L} reference depending upon the state of the $\text{UP}/\overline{\text{DN}}$ input.

The host may exit an adjustment routine in two ways: deselecting the SMP9317 while $\overline{\text{INC}}$ is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the SMP9317 while $\overline{\text{INC}}$ is high will store the current V_{OUT} setting into non-volatile memory.

PINOUT



Increment ($\overline{\text{INC}}$) is an edge triggered input. Whenever $\overline{\text{CS}}$ is low and a high to low transition occurs on the $\overline{\text{INC}}$ input, the V_{OUT} voltage will either move toward V_{H} or V_{L} depending upon the state of the $\text{UP}/\overline{\text{DN}}$ input.

UP/Down ($\text{UP}/\overline{\text{DN}}$) is an input that will determine the V_{OUT} movement relative to V_{H} and V_{L} . When $\overline{\text{CS}}$ is low, $\text{UP}/\overline{\text{DN}}$ is high and there is a high to low transition on $\overline{\text{INC}}$, the V_{OUT} voltage will move $(1/128^{\text{th}} \times V_{\text{H}} - V_{\text{L}})$ toward V_{H} . When $\overline{\text{CS}}$ and $\text{UP}/\overline{\text{DN}}$ are low, and there is a high to low transition on $\overline{\text{INC}}$, the V_{OUT} will move $(1/128^{\text{th}} \times V_{\text{H}} - V_{\text{L}})$ toward V_{L} .

Power-Up/Power-Down Conditions

On power-up the SMP9317 loads the value of EEPROM memory into the wiper position register. The value in the register is changed using the $\overline{\text{CS}}$, $\overline{\text{INC}}$, and $\text{UP}/\overline{\text{DN}}$ pins. The new data in the register will be lost at power-down unless $\overline{\text{CS}}$ was brought high, with $\overline{\text{INC}}$ high, to initiate a store operation after the last increment or decrement. On the next device power-up, the value of EEPROM memory will be loaded into the wiper position register. During power-up the SMP9317 is write-protected in two ways:

- 1) A power-on reset, that trips at approximately 2.5V, holds $\overline{\text{CS}}$ and $\overline{\text{INC}}$ high internally.
- 2) Resistor pull-ups on all logic inputs prevent data change if the inputs are floating.

Data Retention

The SMP9317 is guaranteed to perform at least 1,000,000 writes to EEPROM before a wear-out condition can occur. After EEPROM wearout, the SMP9317 continues to function as a volatile digital-potentiometer. The wiper position can be changed during powered conditions using the digital interface. However, on power-up the wiper-position will be indeterminate.

On shipment from the factory, Summit Microelectronics does not specify any EEPROM memory value. The value must be set by the customer as needed.

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on pins with reference to GND:	
Analog Inputs	-0.5V to V _{DD} +0.5V
Digital Inputs	-0.5V to V _{DD} +0.5V
Analog Outputs	-0.5V to V _{DD} +0.5V
Digital Outputs	-0.5V to V _{DD} +0.5V
Lead Solder Temperature (10 secs)	300°C

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V _{DD}	+2.7V	+5.5V

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DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Accuracy	INL	Integral Non-Linearity	I _{LOAD} = 50μA, T _R = C T _R = I	-	0.6	±1	LSB
			I _{LOAD} = 100μA, T _R = C T _R = I	-	1.2	-	LSB
	DNL	Differential Non-Linearity	I _{LOAD} = 50μA, T _R = C T _R = I	-	0.25	±0.5	LSB
			I _{LOAD} = 100μA, T _R = C T _R = I	-	0.5	-	LSB
References	V _H	V _{refH} Input Voltage		2.5	-	V _{DD}	V
	V _L	V _{refL} Input Voltage	V _H ≥ V _L	Gnd	-	V _{DD} -2.5	V
	R _{IN}	V _{refH} to V _{refL} Resistance		-	38K	-	Ω
	TCR _{IN}	Temperature Coefficient of R _{IN}	V _{refH} to V _{refL}	-	700	-	ppm/°C
Analog Output	GEFS	Full-Scale Gain Error	DATA = 7F	-	-	±1	LSB
	V _{OUTZS}	Zero-Scale Output Voltage	DATA = 00	0		20	mV
	TCV _{OUT}	V _{OUT} Temperature Coefficient, note 3	V _{DD} = +5, I _{LOAD} = 50μA, V _{refH} = +5V, V _{refL} = 0V	-	-	200	μV/°C
	I _L	Amplifier Output Load Current				100	μA
	R _{OUT}	Amplifier Output Resistance	I _L = 100μA +5V +3V	- -	10 20		Ω Ω
	PSRR	Power Supply Rejection	I _{LOAD} = 10μA	-	-	1	LSB/V
	e _N	Amplifier Output Noise	f = 1KHz, V _{DD} = +5V	-	90	-	nV/√Hz
	THD	Total Harmonic Distortion	V _{IN} = 1V rms, f = 1KHz	-	0.08	-	%
	BW	Bandwidth - 3dB	V _{IN} = 100mV rms	-	1,000	-	kHz

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**RELIABILITY CHARACTERISTICS (over recommended operating conditions unless otherwise specified)**

Symbol	Parameter	Min	Max	Unit	Test Method
V _{ZAP}	ESD Susceptibility	2000		V	MS-883, TM 3015
I _{LTH}	Latch-Up	100		mA	JEDEC Standard 17
T _{DR}	Data Retention	100		Years	MS-883, TM 1008
N _{END}	Endurance	1,000,000		Stores	MS-883, TM 1033

2031 PGM T2.0

DC ELECTRICAL CHARACTERISTICSV_{DD} = +2.7V to +5.5V, V_H = V_{DD}, V_L = 0V, T_A = -40°C to +85°C, Unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{DD}	Supply Current during store, note 1	CS = V _{IL} to V _{IH} W/ $\overline{\text{INC}}$ HI		1.0		mA
I _{SB}	Supply Standby Current	CS = V _{IH}			100	μA
I _{IH}	Input Leakage Current	V _{IN} = V _{DD}			10	μA
I _{IL}	Input Leakage Current, note 2	V _{IN} = 0V			-25	μA
V _{IH}	High Level Input Voltage		2		V _{DD}	V
V _{IL}	Low Level Input Voltage	V _{DD} ≥ 4.5V	0		0.8	V

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Notes:

1. I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
2. $\overline{\text{CS}}$, UP/ $\overline{\text{DN}}$ and $\overline{\text{INC}}$ have internal pull-up resistors of approximately 200kΩ. When the input is pulled to ground the resulting output current will be V_{DD}/200kΩ.
3. TCV_{OUT} is guaranteed but not tested.



OPERATIONAL TRUTH TABLE

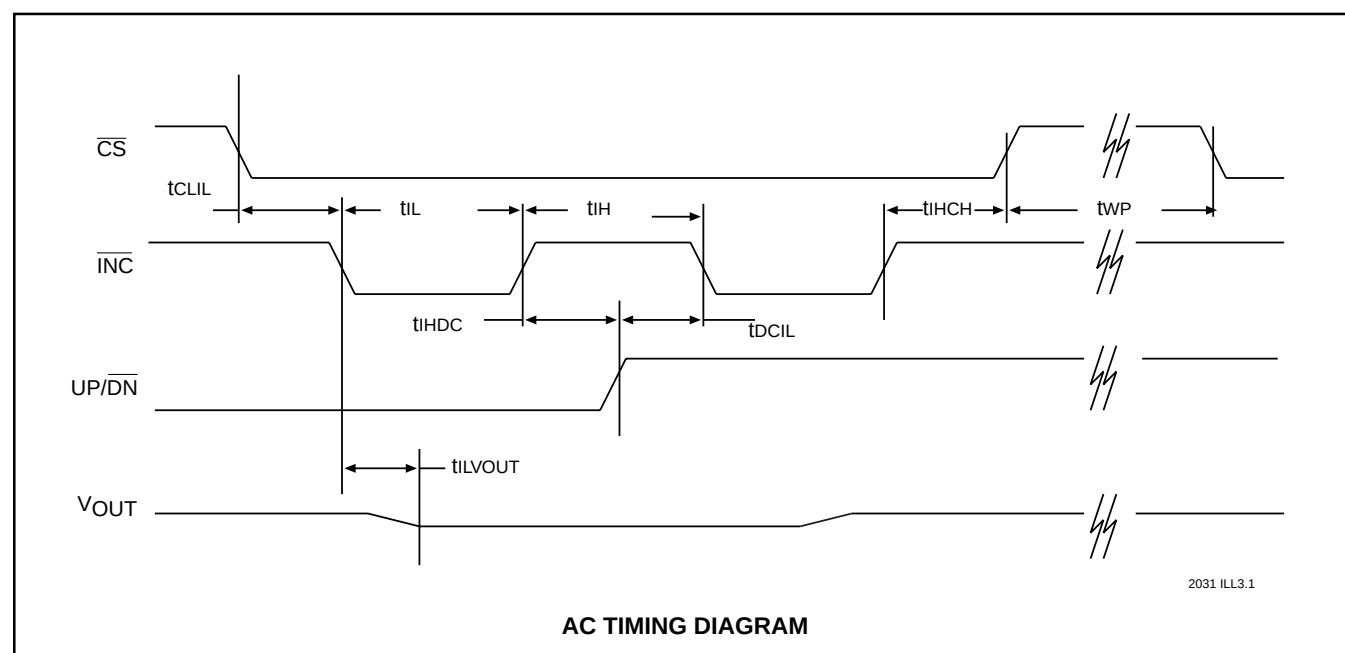
$\overline{\text{INC}}$	$\overline{\text{CS}}$	UP/DN	Operation
HI _{TO} LO	L	H	V _{OUT} toward V _H
HI _{TO} LO	L	L	V _{OUT} toward V _L
H	LO _{TO} HI	X	Store Setting
L	LO _{TO} HI	X	Maintain Setting, NO Store
X	H	X	Standby, note 1

Notes: 1. The Standby or operating current will be lowest with $\overline{\text{INC}}$ and UP/DN pins at H as there are weak internal pull-ups that draw current when connected LO. 2031 PGM T5.1

AC TIMING CHARACTERISTICS

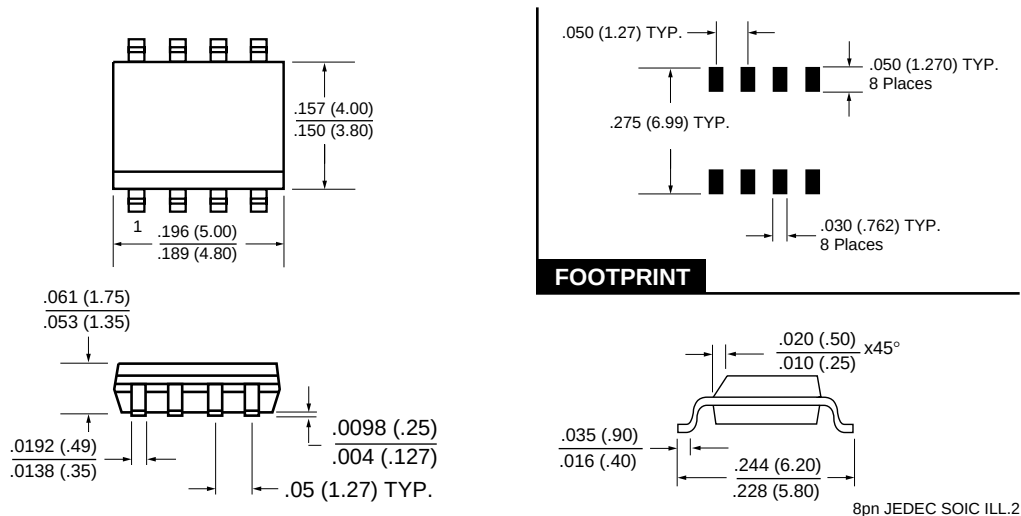
Symbol	Parameter	Min	Max	Units
t _{CLIL}	$\overline{\text{CS}}$ to $\overline{\text{INC}}$ Setup	100		ns
t _{IHDC}	$\overline{\text{INC}}$ High to UP/DN Change	100		ns
t _{DCIL}	UP/DN to $\overline{\text{INC}}$ Setup	100		ns
t _{IL}	$\overline{\text{INC}}$ Low Period	200		ns
t _{IH}	$\overline{\text{INC}}$ High Period	200		ns
t _{IHCH}	$\overline{\text{INC}}$ Inactive to $\overline{\text{CS}}$ Inactive	100		ns
t _{WP}	Write Cycle Time		5	ms
t _{ILVOUT}	$\overline{\text{INC}}$ to V _{OUT} Delay		5	μs

2031 PGM T6.0

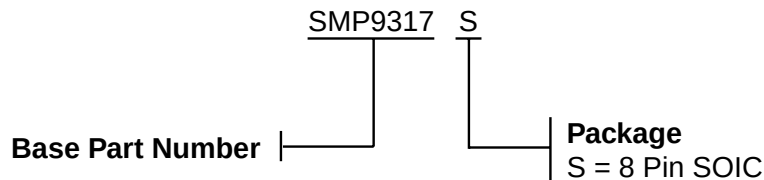




8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



ORDERING INFORMATION



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