HIP4083

80V, 300mA
Three Phase High Side Driver

July 1996

Features

- **Independently Drives Three High Side N-Channel MOSFETs in Three Phase Bridge Configuration**
- **Bootstrap Supply Max Voltage to 95VDC**
- **Bias Supply Operation from 7V to 15V**
- **Drives 1000pF Load with Typical Rise Times of 35ns and Fall Times of 30ns**
- **CMOS/TTL Compatible Inputs**
- **Programmable Undervoltage Protection**

Applications

- **Brushless Motors**
- **High Side Switches**
- **AC Motor Drives**
- **Switched Reluctance Motor Drives**

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HIP4083AB	-40 to 105	16 Ld SOIC	M16.15
HIP4083AP	-40 to 105	16 Ld PDIP	E16.3

Description

The HIP4083 is a three phase high side N-channel MOSFET driver, specifically targeted for PWM motor control. Two HIP4083 may be used together for 3 phase full bridge applications (see application block diagram). Alternatively, the lower gates may be controlled directly from a buffered microprocessor output.

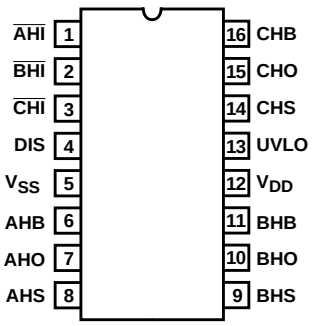
Unlike other members of the HIP408x family, the HIP4083 has no built in turn-on delay. Each output (AHO, BHO, and CHO) will turn-on 65ns after its input is switched low. Likewise, each output will turn-off 60ns after its input is switched high. Very short and very long dead times are possible when two HIP4083 are used to drive a full bridge. This dead time is controlled by the input signal timing.

The HIP4083 does not have a built in charge pump. Therefore, the bootstrap capacitors must be recharged on a periodic basis by initiating a short refresh pulse. In most bridge applications, this will happen automatically every time the lower FETs turn-on and the upper FETs turn-off. However, it is still possible to use the HIP4083 in applications that require the high side FETs to be on for extended periods of time. This can be easily accomplished by sending a short refresh pulse to the DIS pin.

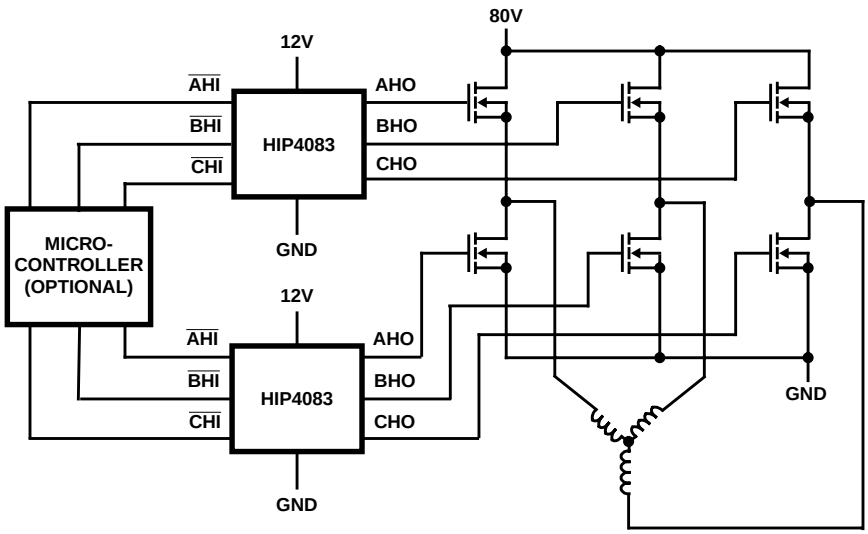
The HIP4083 has reduced drive current compared to the HIP4086 making it ideal for low to moderate power applications. The HIP4083 is optimized for applications where size and cost are important. For high power applications driving large power FETs, the HIP4086 is recommended.

Pinout

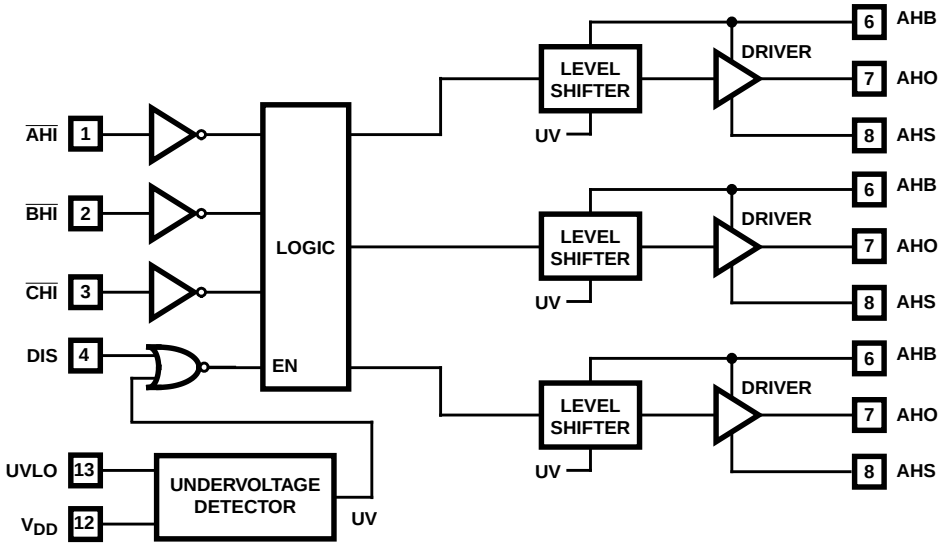
HIP4083
PDIP, SOIC
TOP VIEW



Application Block Diagram



Functional Block Diagram

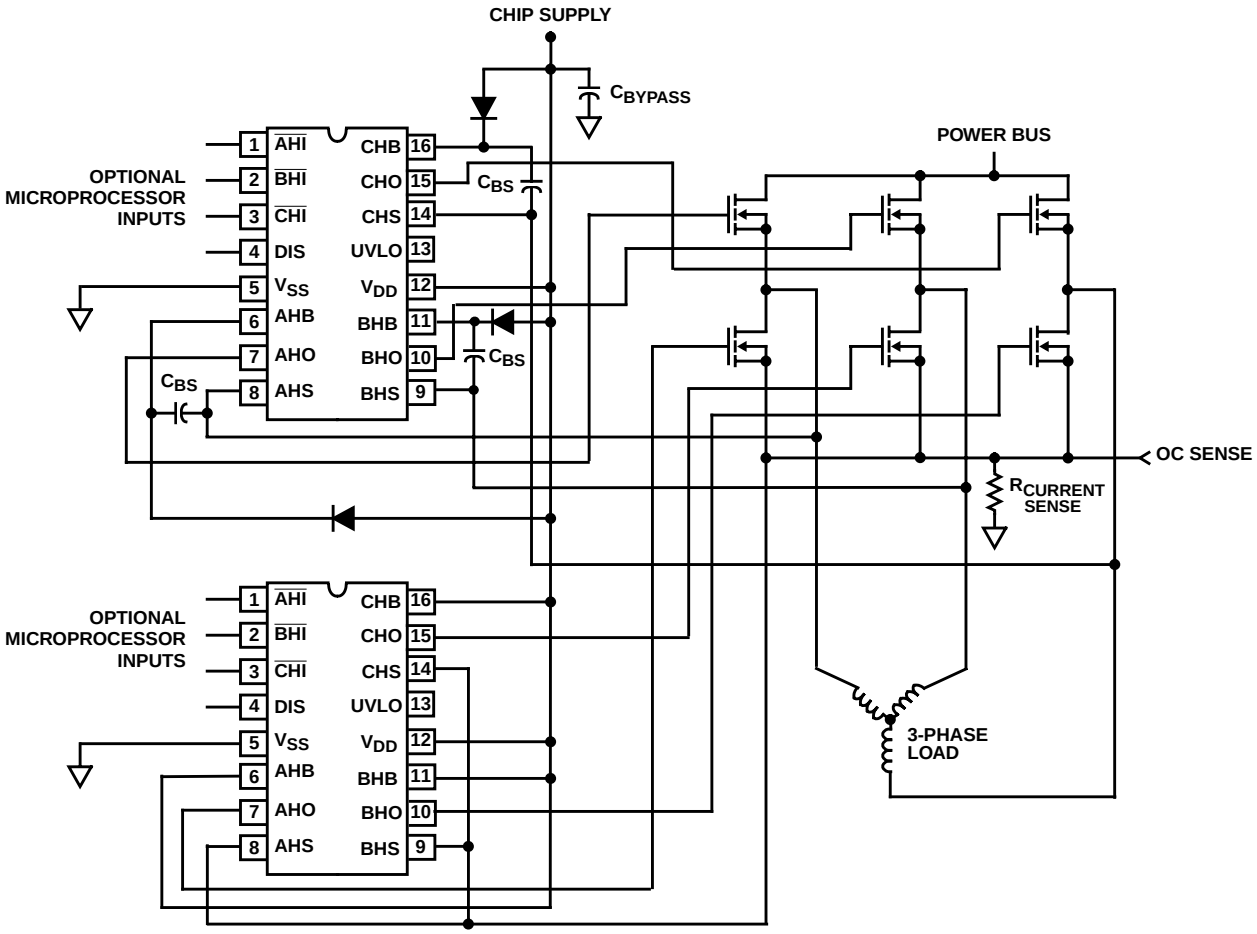


TRUTH TABLE

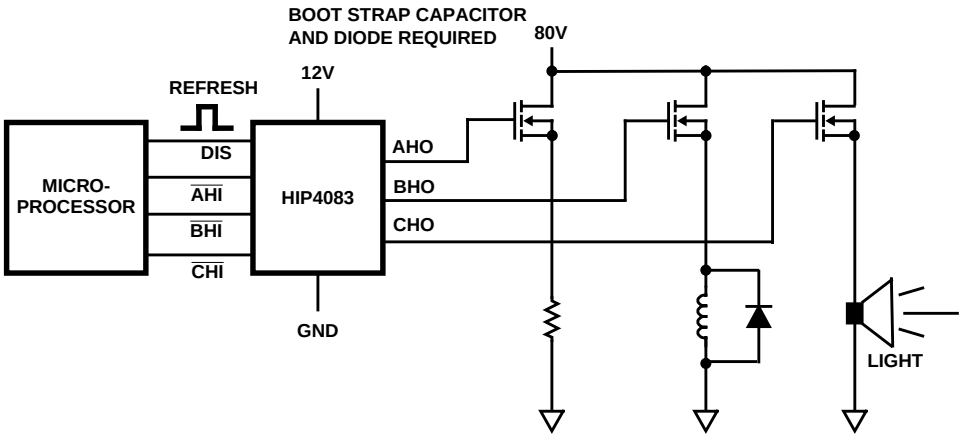
INPUT			OUTPUT
$\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$	UV	DIS	AHO, BHO, CHO
X	1	X	0
X	X	1	0
1	0	0	0
0	0	0	1

NOTE: X signifies that input can be either a “1” or “0”.

Typical Application: Three Phase Bridge Driver with Programmable Dead Time



Typical Application: High Side Switch



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
6 11 16	AHB BHB CHB (xHB)	Gate driver supplies. One external bootstrap diode and one capacitor are required for each. The bootstrap diode and capacitor may be omitted when the HIP4083 is used to drive the lower gates in three phase full bridge applications. In this case, tie all three xHB pins to V_{DD} and tie the xHS pins to the sources of the lower FETs. In full bridge applications, the lower FETs must be turned on first at start up to refresh the bootstrap capacitors. In high side switch applications, the load will keep xHS low and refresh should happen automatically at start up.
1 2 3	AHI BHI CHI ($\overline{xHI}$)	Logic level inputs. Logic at these three pins controls the three output drivers, AHO, BHO and CHO. When $\overline{xHI}$ is low, xHO is high. When $\overline{xHI}$ is high, xHO is low. DIS (Disable) overrides all input signals. $\overline{xHI}$ can be driven by signal levels of 0V to 15V (no greater than V_{DD}). If these pins are not driven, an internal 100µA current source pulls them high.
5	V_{SS}	Chip ground.
13	UVLO	Undervoltage setting. A resistor can be connected between this pin and V_{SS} to program the under voltage set point - see Figure 7. With this pin not connected the undervoltage set point is typically 7V. When this pin is tied to V_{DD}, the undervoltage set point is typically 6.2V.
4	DIS	Disable input. Logic level input that when taken high sets all three outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. DIS can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up holds DIS high when this pin is not driven.
7 10 15	AHO BHO CHO (xHO)	Gate connections. Connect to the gates of the power MOSFETs in each phase.
8 9 14	AHS BHS CHS (xHS)	MOSFET source connection. Connect the sources of the power MOSFETs and the negative side of the bootstrap capacitors to these pins. In high side switch applications, 2mA of current will flow out of these pins into the load when the upper FETs are off. This current is necessary to guarantee that the upper FETs stay off. This current tends to pull xHS high. For proper refresh, the load must pull the voltage on xHS down to at least 7V below V_{DD}. For example, when V_{DD} = 12V, xHS must be pulled down to 5V. Therefore, the minimum load necessary for proper refresh is given by the following equation: R_{MIN} = 5V/2mA = 2.5kΩ. So in this case, if the load has an impedance less than 5kΩ, refresh will happen automatically at start up.
12	V_{DD}	Positive supply rail. Bypass this pin to V_{SS} with a capacitor ≥1µF. In applications where the bus voltage and chip V_{DD} are at the same potential, it is a good idea to run a separate line from the supply to each. This greatly simplifies the filtering requirements.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{DD} . . . . . -0.3V to 16V
Logic I/O Voltages . . . . . -0.3V to V_{DD} +0.3V
Voltage on xHS . . . . . -6V (Transient) to 85V (-40°C to 150°C)
Voltage on xHB . . . . . V_{xHS} -0.3V to V_{xHS} +V_{DD}
Voltage on xLO . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Voltage on xHO . . . . . V_{xHS} -0.3V to V_{xHB} +0.3V
Phase Slew Rate 20V/ns

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	100
DIP Package	80

Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Supply Voltage, V_{DD} . . . . . +7.0V to +15V
Voltage on xHS . . . . . .0V to 80V
Voltage on xHB . . . . . V_{xHS} +V_{DD}
Operating Ambient Temperature Range . . . . . -40°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. All voltages are relative to V_{SS} unless otherwise specified.
3. x = A, B and C. For example, xHS refers to AHS, BHS and CHS.

Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, Gate Capacitance (C_{GATE}) = 1000pF, $R_{UV} = \infty$

PARAMETER	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 150^oC		UNITS
		MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND UNDER VOLTAGE PROTECTION							
V_{DD} Quiescent Current	$\overline{xHI}$ = 5V	0.5	1.5	2.25	0.25	2.3	mA
V_{DD} Operating Current	f = 20kHz, 50% Duty Cycle	1.0	2.0	2.5	0.75	3.0	mA
xHB On Quiescent Current	$\overline{xHI}$ = 0V	65	100	240	45	250	µA
xHB Off Quiescent Current	$\overline{xHI}$ = 5V	0.6	0.85	1.3	0.5	1.4	mA
xHB Operating Current	f = 20kHz, 50% Duty Cycle	0.6	0.85	1.2	0.5	1.3	mA
V_{DD} Rising Undervoltage Threshold	R_{UV} OPEN	6.2	7.0	8.0	6.1	8.1	V
V_{DD} Falling Undervoltage Threshold	R_{UV} OPEN	5.75	6.5	7.5	5.25	7.6	V
Minimum Undervoltage Threshold	$R_{UV} = V_{DD}$	5.0	6.2	6.9	4.5	7.0	V
INPUT PINS: AHI, BHI, CHI AND DIS							
Low Level Input Voltage		-	-	1.0	-	0.8	V
High Level Input Voltage		2.5	-	-	2.7	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	V_{IN} = 0V	-145	-100	-60	-150	-50	µA
High Level Input Current	V_{IN} = 5V	-1	-	+1	-10	+10	µA
GATE DRIVER OUTPUT PINS: AHO, BHO, AND CHO							
Average Turn-On Current	V_{OUT} 0V to 5V	100	240	400	50	500	mA
Average Turn-Off Current	V_{OUT} V_{DD} to 4V	150	300	450	100	550	mA

Switching Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $C_{GATE} = 1000pF$

PARAMETER	TEST CONDITIONS	$T_J = 25^oC$			$T_{JS} = -40^oC$ TO 150^oC		UNITS
		MIN	TYP	MAX	MIN	MAX	
Turn-Off Propagation Delay (xHI - xHO)	No Load	-	60	80		90	ns
Turn-On Propagation Delay (xHI - xHO)	No Load	-	65	90		100	ns
Rise Time (10 - 90%)	C_{GATE} = 1000pF	-	35	60	-	65	ns
Fall Time (90 - 10%)	C_{GATE} = 1000pF	-	30	50	-	55	ns
Disable Turn-Off Propagation Delay	No Load	-	65	-	-	100	ns
Disable to Output Enable (DIS - xHO)	No Load	-	70	-	-	100	ns

Typical Performance Curves

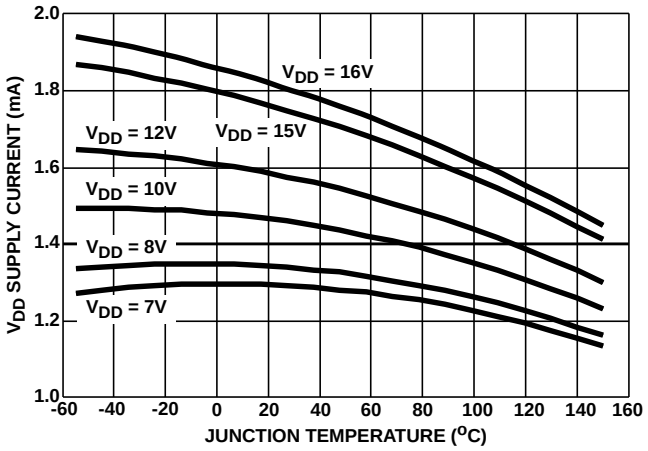


FIGURE 1. V_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

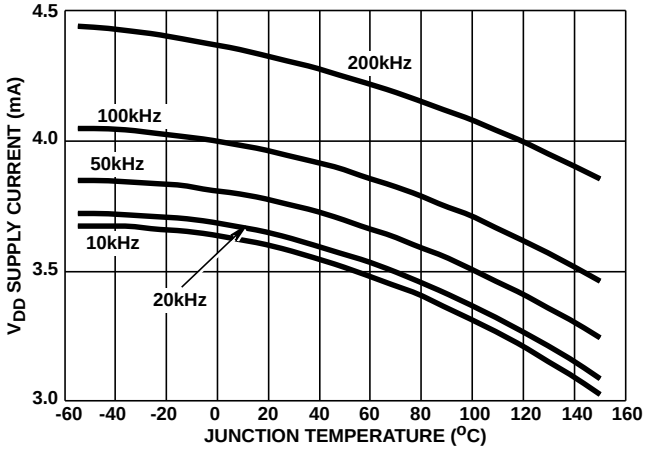


FIGURE 2. V_{DD} SUPPLY CURRENT vs SWITCHING FREQUENCY

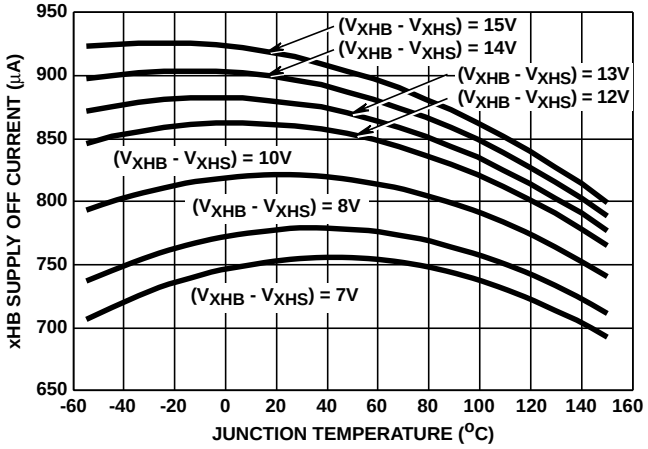


FIGURE 3. FLOATING SUPPLY OFF BIAS CURRENT

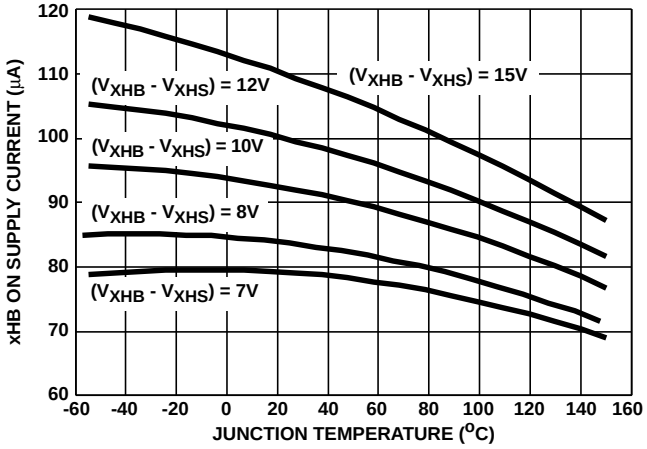


FIGURE 4. FLOATING SUPPLY ON BIAS CURRENT

Typical Performance Curves (Continued)

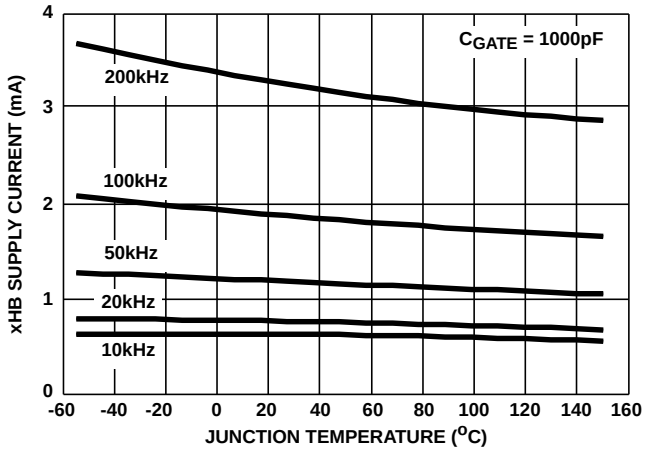


FIGURE 5. FLOATING SUPPLY SWITCHING BIAS CURRENT

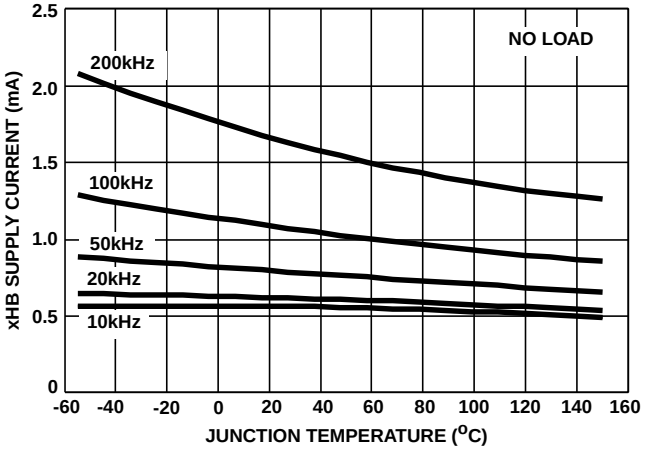


FIGURE 6. FLOATING SUPPLY SWITCHING BIAS CURRENT

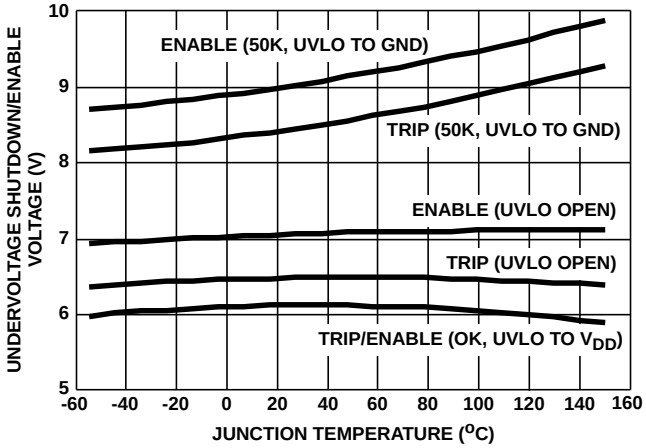


FIGURE 7. UNDERVOLTAGE THRESHOLD

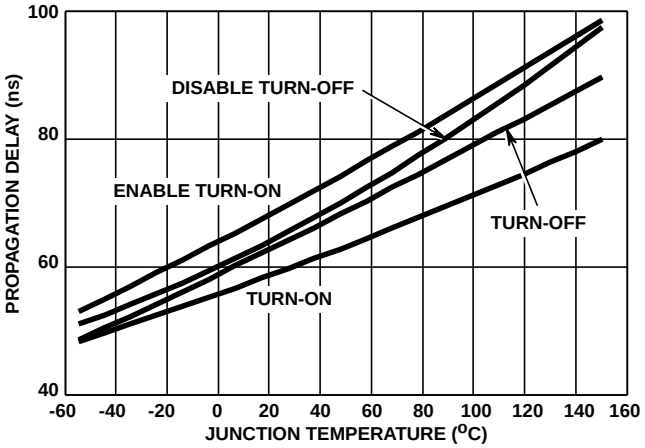


FIGURE 8. PROPAGATION DELAY

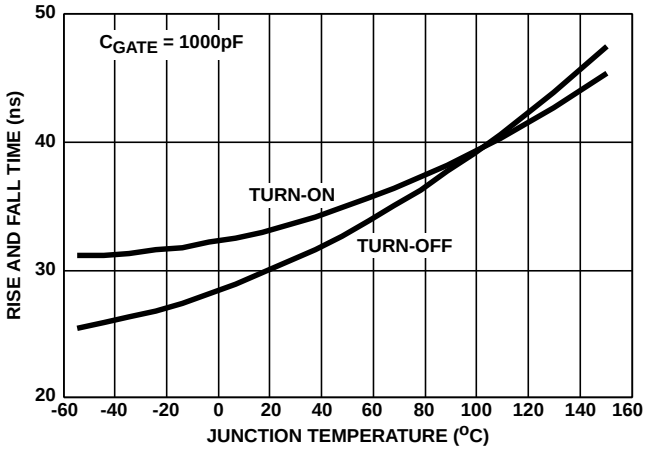


FIGURE 9. RISE AND FALL TIME (10-90%)

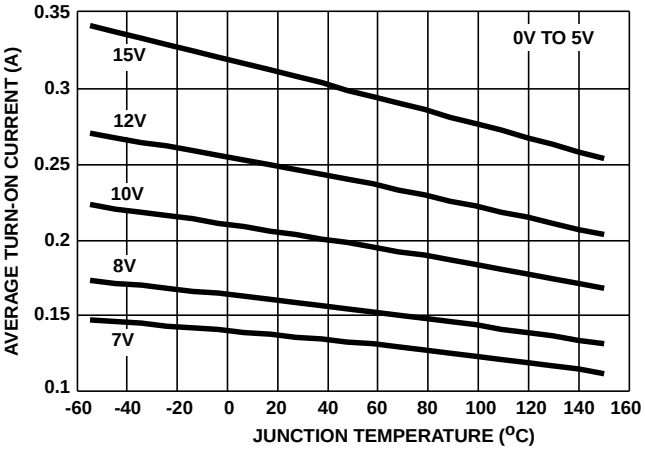


FIGURE 10. GATE DRIVER AVERAGE TURN-ON CURRENT

Typical Performance Curves (Continued)

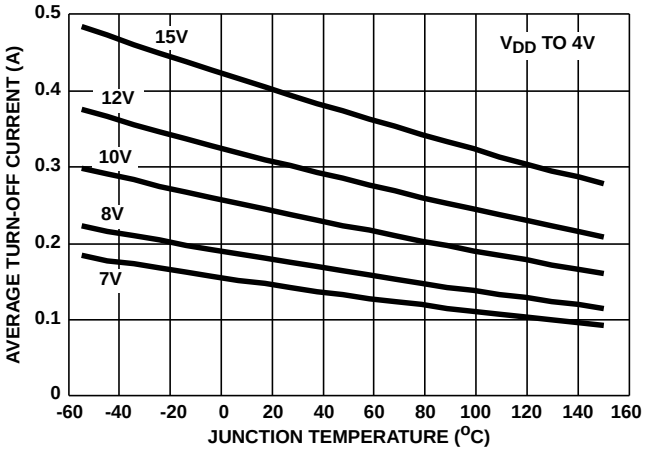


FIGURE 11. GATE DRIVER AVERAGE TURN-OFF CURRENT

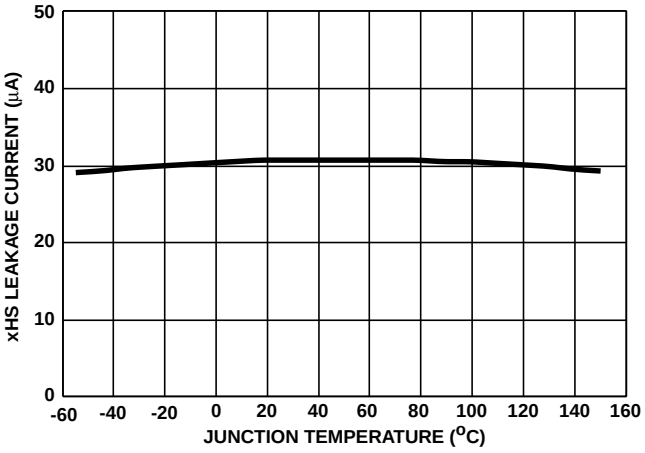
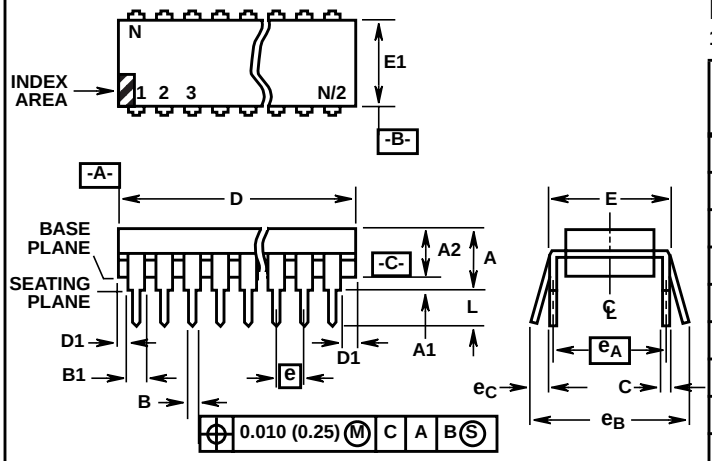


FIGURE 12. HIGH VOLTAGE LEAKAGE CURRENT

Dual-In-Line Plastic Packages (PDIP)



NOTES:

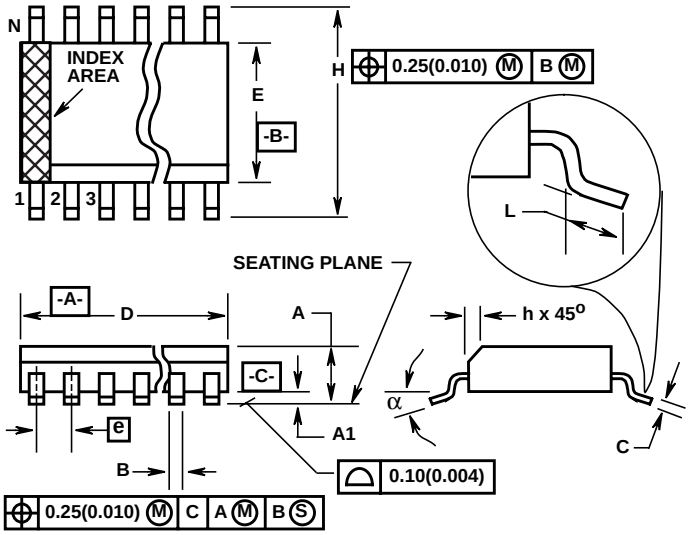
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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