NanoAmp Solutions, Inc.
670 N. McCarthy Blvd. Suite 220, Milpitas, CA 95035
ph: 408-935-7777, FAX: 408-935-7770
www.nanoamp.com

64Mb Ultra-Low Power Asynchronous CMOS PSRAM

4M × 16 Bits

Overview

The N64T1630C1B is an integrated memory device containing a 64 Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 4,194,304 words by 16 bits. It is designed to be compatible in operation and interface to standard 6T SRAMS. The device is designed for low standby and operating current and includes a power-down feature to automatically enter standby mode. The device includes a $\overline{ZZ}$ input for deep sleep as well as several other power saving modes: Partial Array Self Refresh mode where data is retained in a portion of the array and Temperature Compensated Refresh. Both these modes reduce standby current drain. The N64T1630C1B can be operated in a standard asynchronous mode and data can also be read in a 4-word page mode for fast access times. The die has separate power rails, VccQ and VssQ for the I/O to be run from a separate power supply from the device core.

Features

- **Dual voltage rails for optimum power & performance**
  Vcc - 2.7V - 3.3V
  Vccq - 2.7V to 3.3V
- **Fast Cycle Times**
  T_{ACC} < 70 nS (60ns future)
  T_{PACC} < 25 nS
- **Very low standby current**
  I_{SB} < 170µA
- **Very low operating current**
  Icc < 25mA
- **PASR (Partial Array Self Refresh)**
- **TCR (Temperature Compensated Refresh)**

Table 1: Product Family

Part Number	Package Type	Operating Temperature	Power Supply	I/O Supply	Speed	Standby Current (I_{SB}), Max
N64T1630C1BZ	BGA	-25°C to +85°C	2.7 - 3.3V	2.7 - 3.3V	70ns	170µA

Ball Congiguration

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	$\overline{ZZ}$
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	A_{21}	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	A_{19}	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	A_{20}

48 Pin BGA (top view)
6 x 8 mm

Ball Description

Pin Name	Pin Function
A_0-A_{21}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
$\overline{ZZ}$	Deep Sleep Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power I/O only
V_{SSQ}	Ground I/O only

Figure 1: Functional Block Diagram

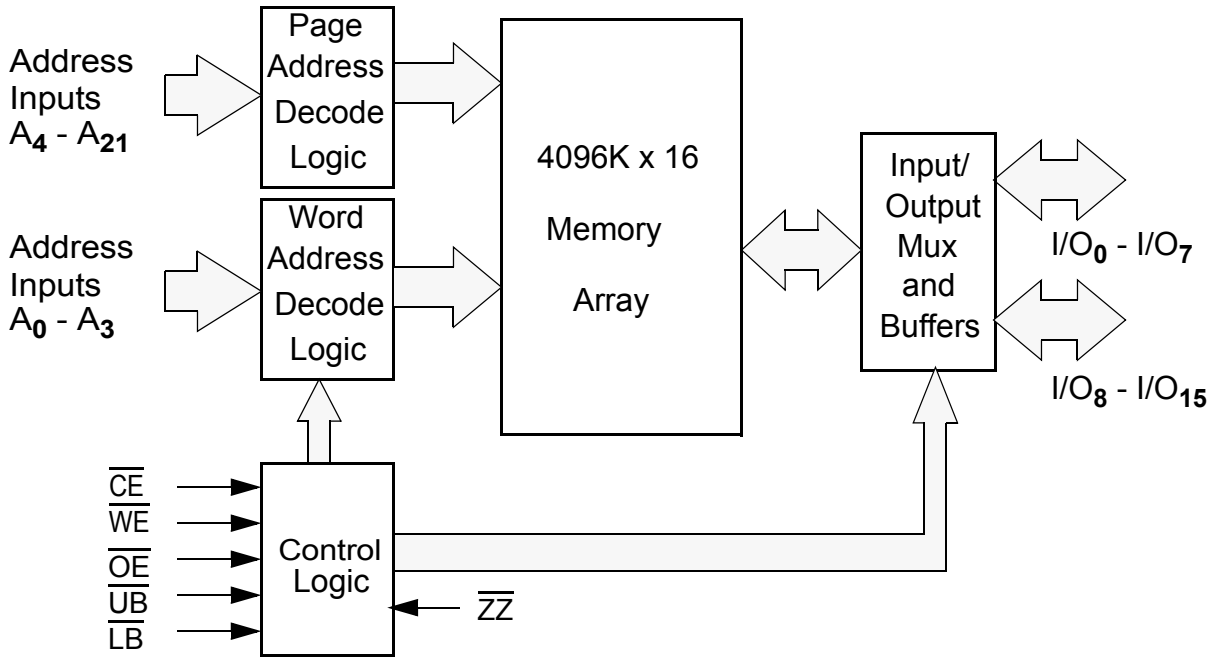


Table 2: Functional Description

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}/\overline{LB}$	$\overline{ZZ}$	I/O[1]	MODE	POWER
H	X	X	X	H	High Z	Standby[2]	Standby
L	L	X[3]	L[1]	H	Data In	Write	Active
L	H	L	L[1]	H	Data Out	Read	Active
L	H	H	L	H	High Z	Active	Standby[4]
L	L	X	X	L	High-Z	Set register	Active
H	X	X	X	L	High-Z	Deep Sleep	Deep Sleep

1. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.
2. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
3. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Table 3: Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	pF

1. These parameters are verified in device characterization and are not 100% tested

Table 4: Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.5 to V_{CCQ}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.2 to 3.6	V
Voltage on V_{CCQ} Supply Relative to V_{SS}	V_{CCQ}	–0.2 to 4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–55 to 150	^oC
Operating Temperature	T_A	-25 to +85	^oC

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5: Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Comments	Min.	Max.	Unit
Supply Voltage	V_{CC}		2.7	3.3	V
Supply Voltage for I/O	V_{CCQ}		Vcc	3.3	V
Input High Voltage	V_{IH}		$0.8V_{CCQ}$	V_{CCQ}+0.2	V
Input Low Voltage	V_{IL}		–0.2	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.2mA	$0.8V_{CCQ}$		V
Output Low Voltage	V_{OL}	I_{OL} = 0.2mA		$0.2V_{CCQ}$	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		1	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled		1	µA
Read/Write Operating Current[1]	I_{CC}	V_{IN}=V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0		25	mA
Page Mode Operating Current	I_{CCP}	V_{IN}=V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0		15	mA
Standby Current[2] V_{IN} = V_{CC} or 0V	I_{SB}	V_{IN} = V_{CC} or 0V Chip Disabled V_{CC} = V_{CC}MAX, t_A= 85^{o}C	100	170	µA

1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

2. This device assumes a standby mode if the chip is disabled ($\overline{CE}$ high). In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.

Table 6: Timing Test Conditions

Item	
Input Pulse Level	V_{SS} to V_{CCQ}
Input Rise and Fall Time (10% to 90%)	1.6ns
Input Timing Reference Levels	0.5 V_{CCQ}
Output Timing Reference Levels	0.5 V_{CCQ}
Operating Temperature	-25 °C to +85 °C

Figure 2: Output Load Circuit

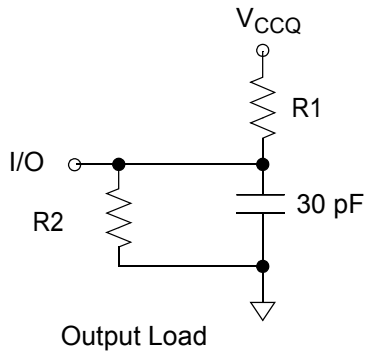


Table 7: Ouput Load

VCCQ	R1/R2
3.0V	4.5KΩ

Table 8: Timings

	Item	Symbol	-70		Unit
			Min	Max	
Read Cycle	Read Cycle Time	t_{RC}	70	20k	ns
	Page Mode Cycle Time	t_{PC}	25		ns
	Address Access Time	t_{AA}		70	ns
	Page Mode Access Time	t_{PA}		25	ns
	Chip Enable to Valid Output	t_{CO}		70	ns
	Output Enable to Valid Output	t_{OE}		20	ns
	Byte Select to Valid Output	t_{BO}		70	ns
	Chip Enable to Low-Z output	t_{LZ}	10		ns
	Output Enable to Low-Z Output	t_{OLZ}	5		ns
	Byte Select to Low-Z Output	t_{BLZ}	10		ns
	Chip Disable to High-Z Output	t_{HZ}	0	8	ns
	Output Disable to High-Z Output	t_{OHZ}	0	8	ns
	Byte Select Disable to High-Z Output	t_{BHZ}	0	8	ns
	Output Hold from Address Change	t_{OH}	5		ns
Write Cycle	Write Cycle Time	t_{WC}	70	20k	ns
	Page Mode Max Write Cycle	t_{PGMAX}		20k	ns
	Chip Enable Active Time	t_{CE}		20k	ns
	Chip Enable HIGH Time	t_{CEH}	5		ns
	Chip Enable to End of Write	t_{CW}	70		ns
	Address Valid to End of Write	t_{AW}	70		ns
	Byte Select to End of Write	t_{BW}	70		ns
	Chip Enable to Low-Z	t_{LZ}	10		ns
	Write Pulse Width	t_{WP}	45		ns
	Write Recovery Time	t_{WR}	0		ns
	Write to High-Z Output	t_{WHZ}	0	8	ns
	Address Setup Time	t_{AS}	0		ns
	Data to Write Time Overlap	t_{DW}	25		ns
	Data Hold from Write Time	t_{DH}	0		ns
	End Write to Low-Z Output	t_{OW}	5		ns
	WE High Time	t_{WEH}	7.5		ns
	Page Write Cycle Time	t_{PWC}	25		ns
	Page Mode Data to Write Time Overlap	t_{PDW}	20		ns
	Page Mode Data Hold From Write Time	t_{PDH}	0		ns

Figure 3: Timing of Read Cycle ($\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

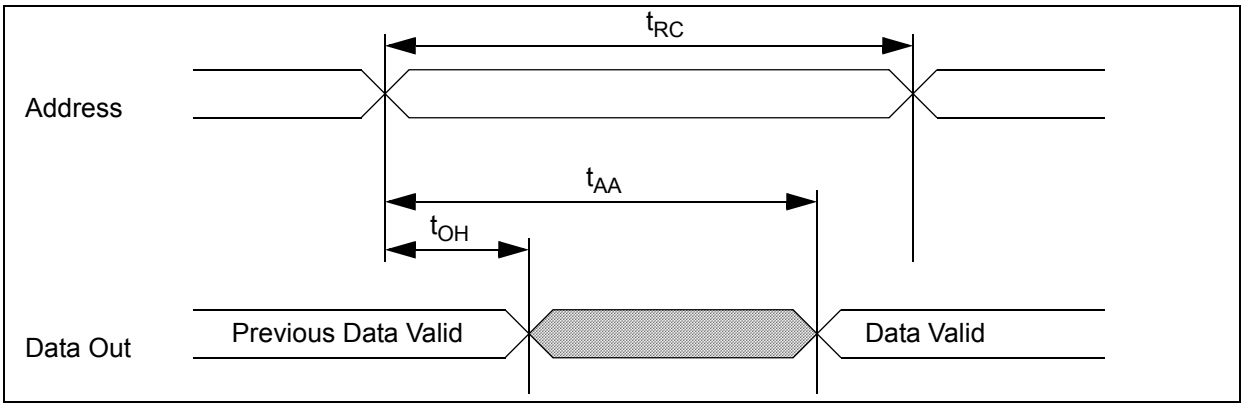


Figure 4: Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})

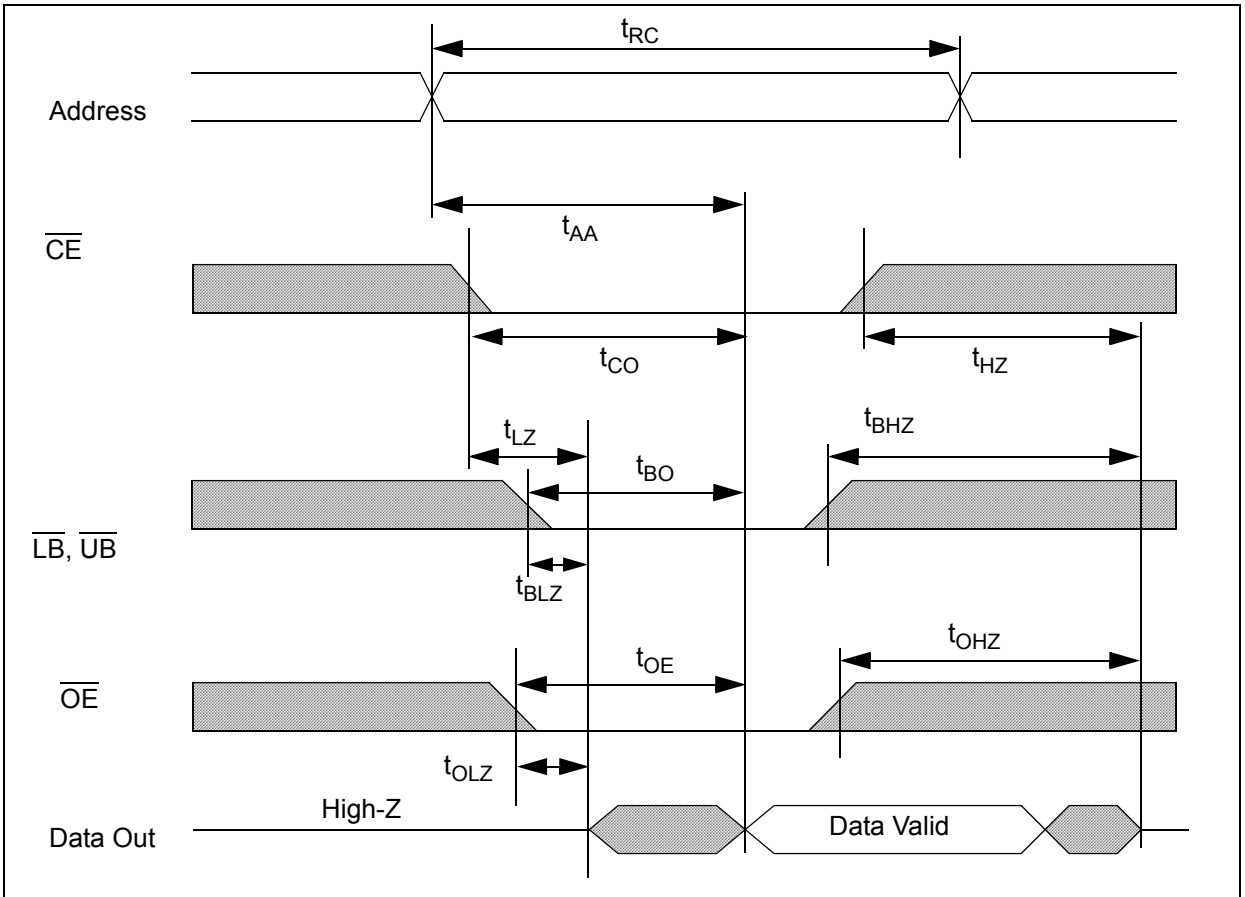


Figure 5: Timing Waveform of Page Mode Read Cycle ($\overline{WE}$=V_{IH})

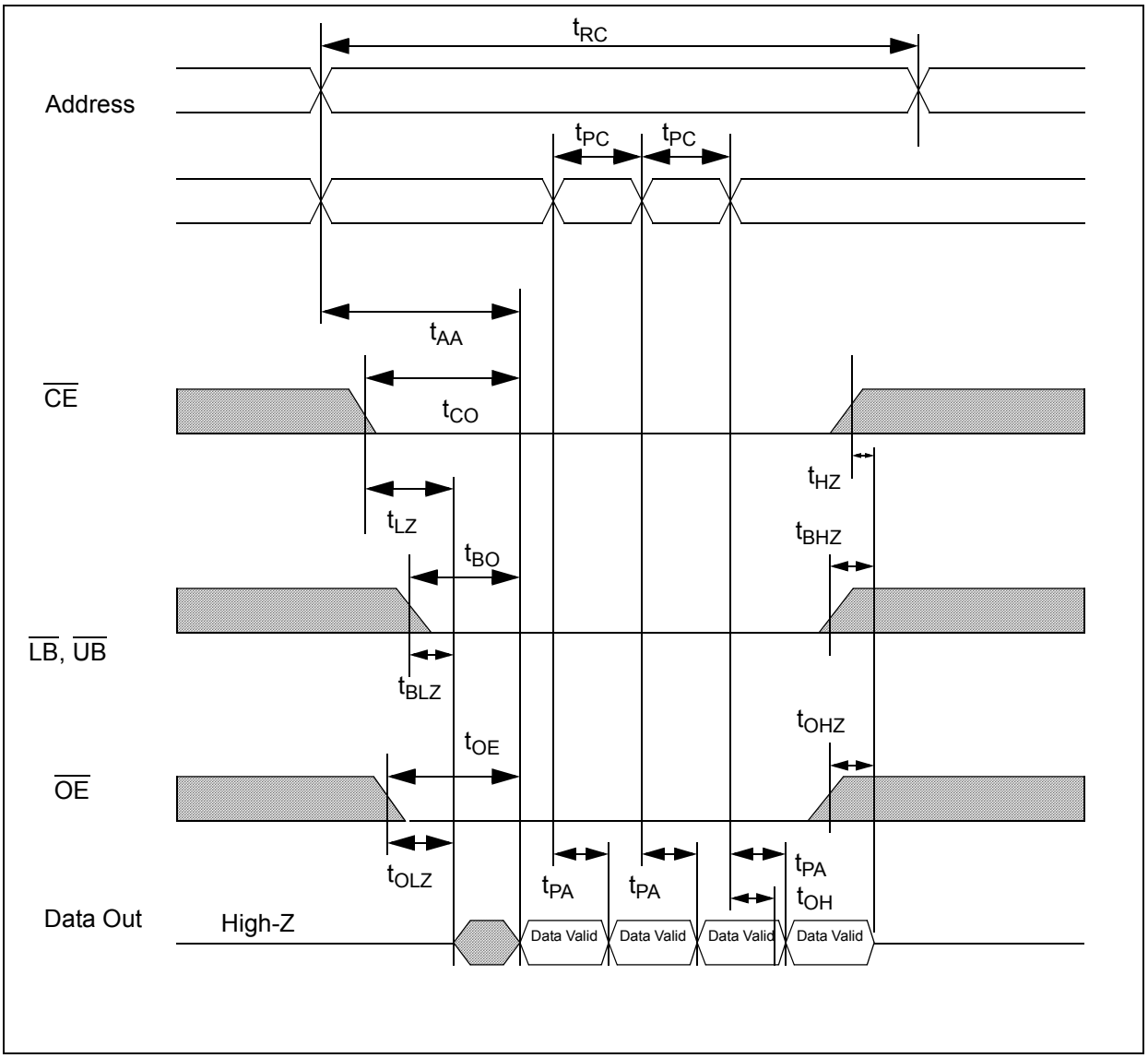


Figure 6: Timing Waveform of Write Cycle ($\overline{WE}$ control)

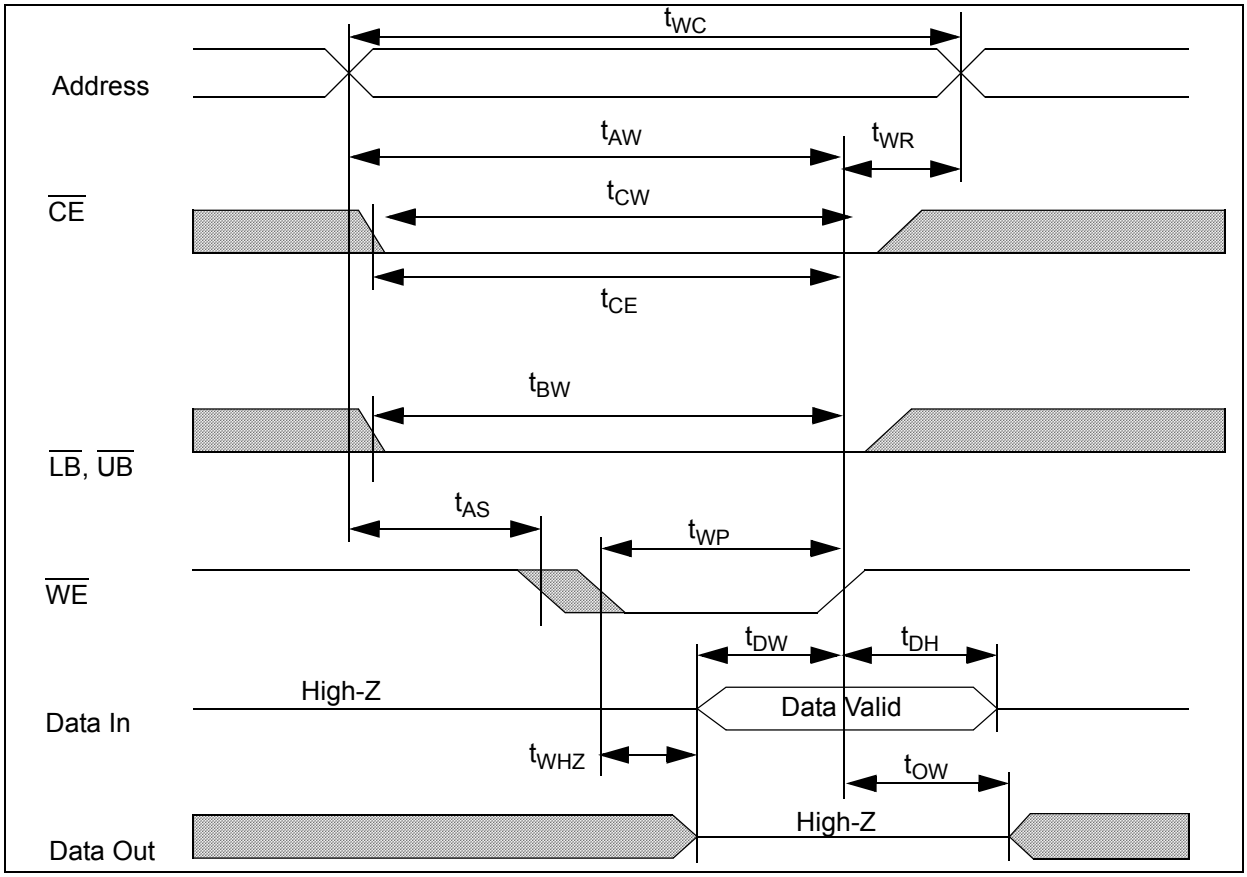


Figure 7: Timing Waveform of Write Cycle ($\overline{CE}$ Control)

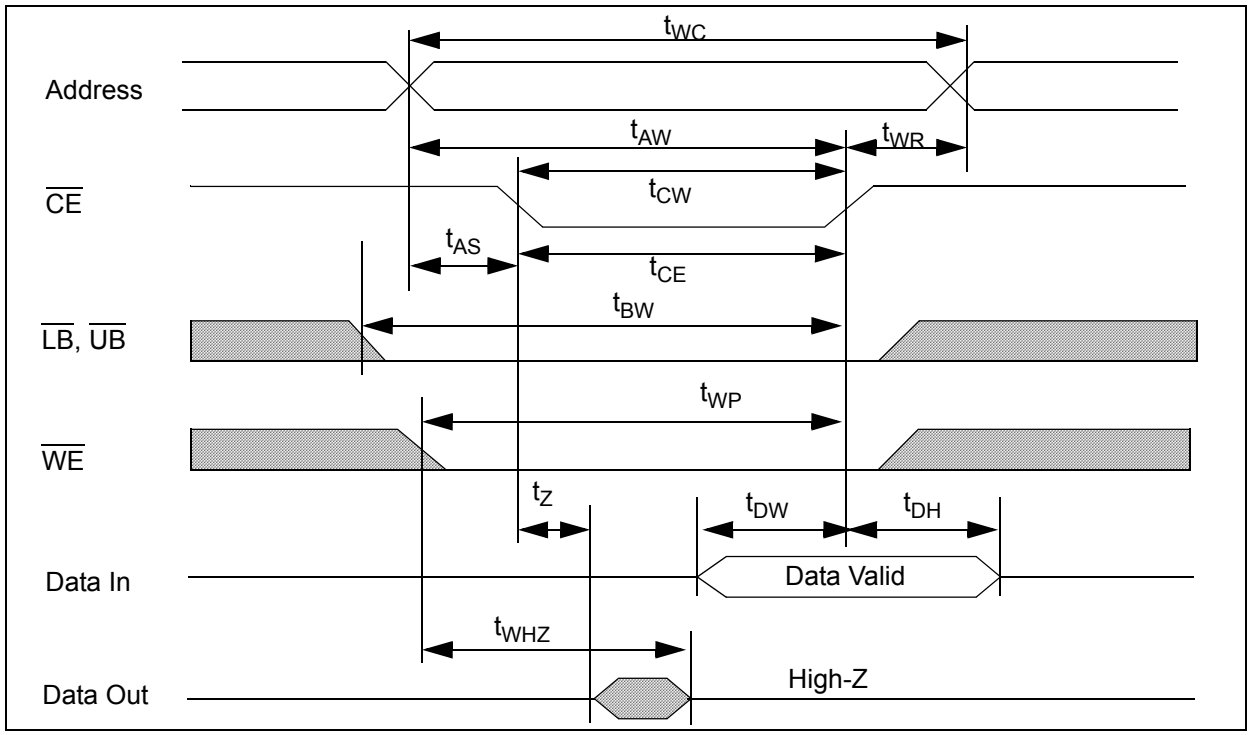


Figure 8: Timing Waveform of Write Cycle ($\overline{UB}$, $\overline{LB}$ control)

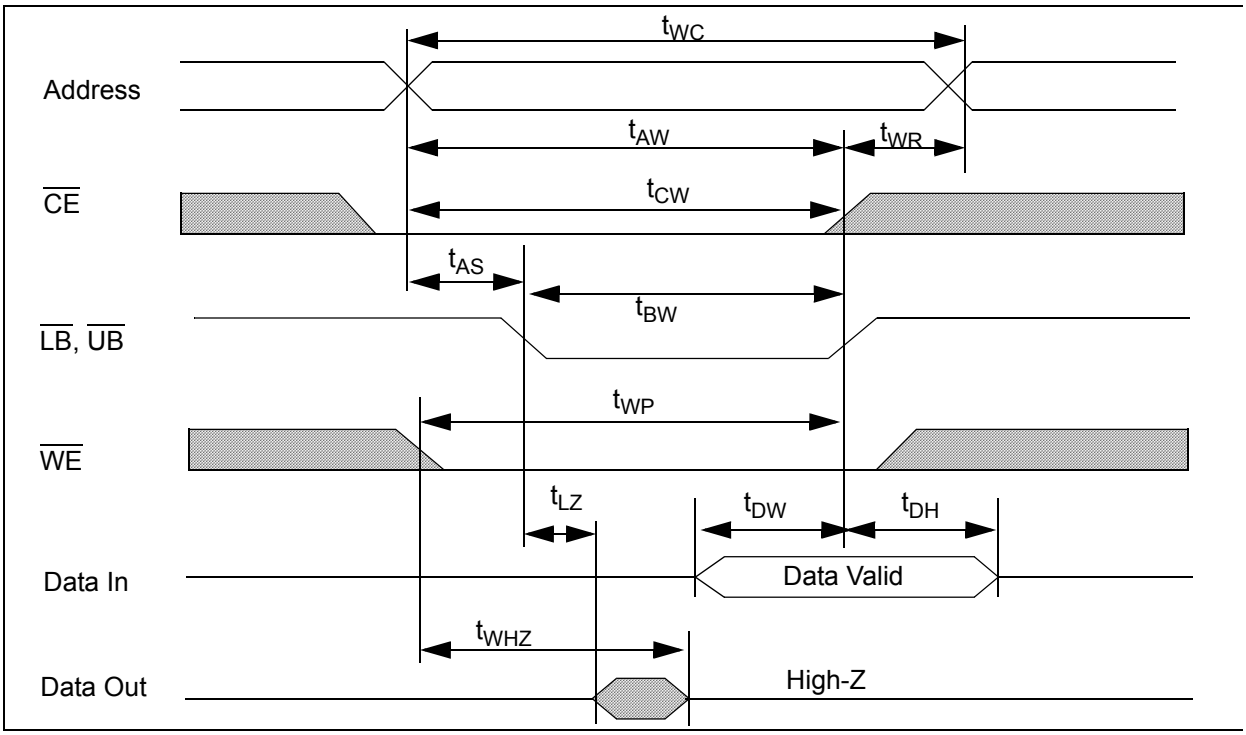


Figure 9: Timing Waveform for Sucessive WE Write Cycles

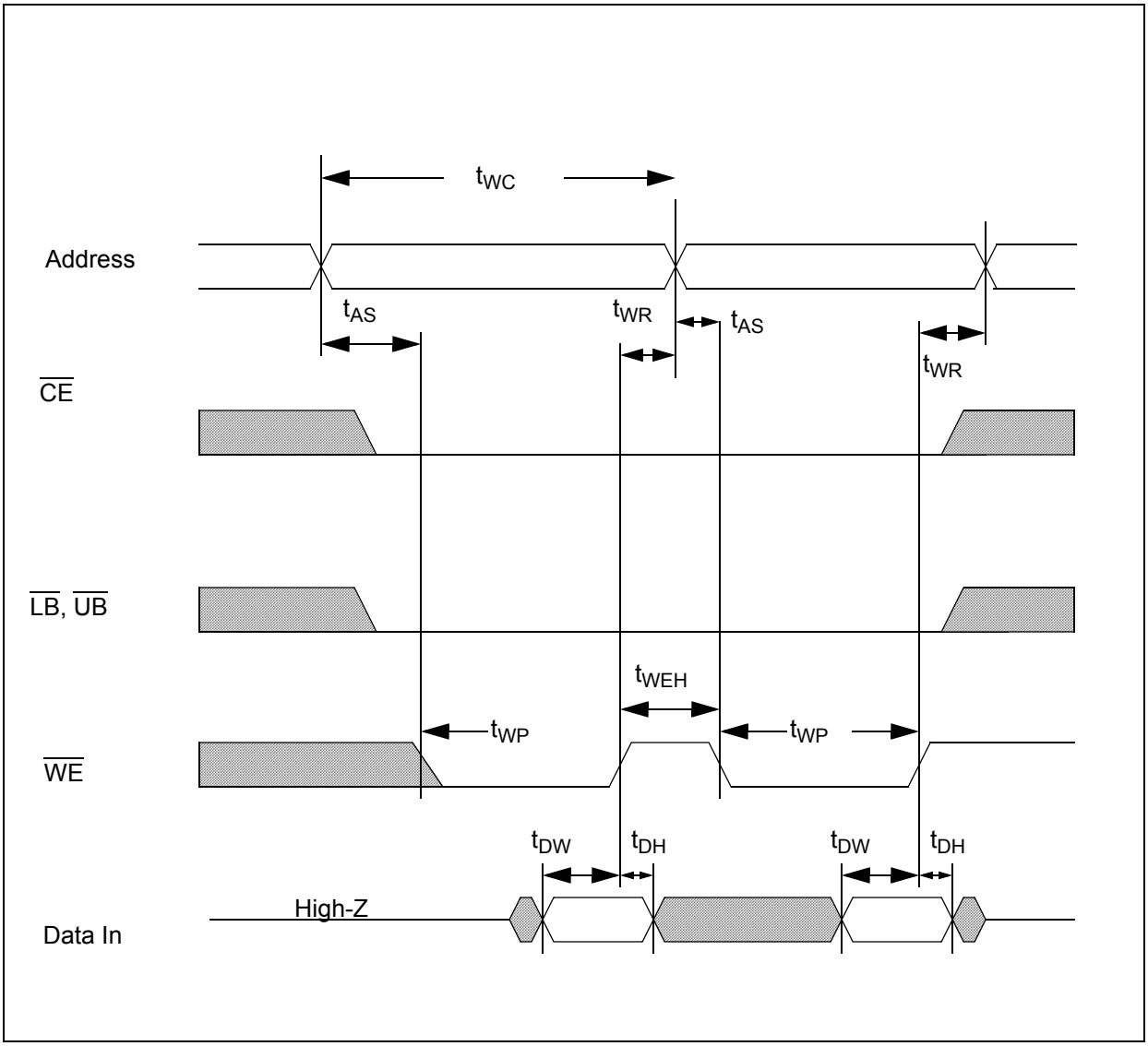
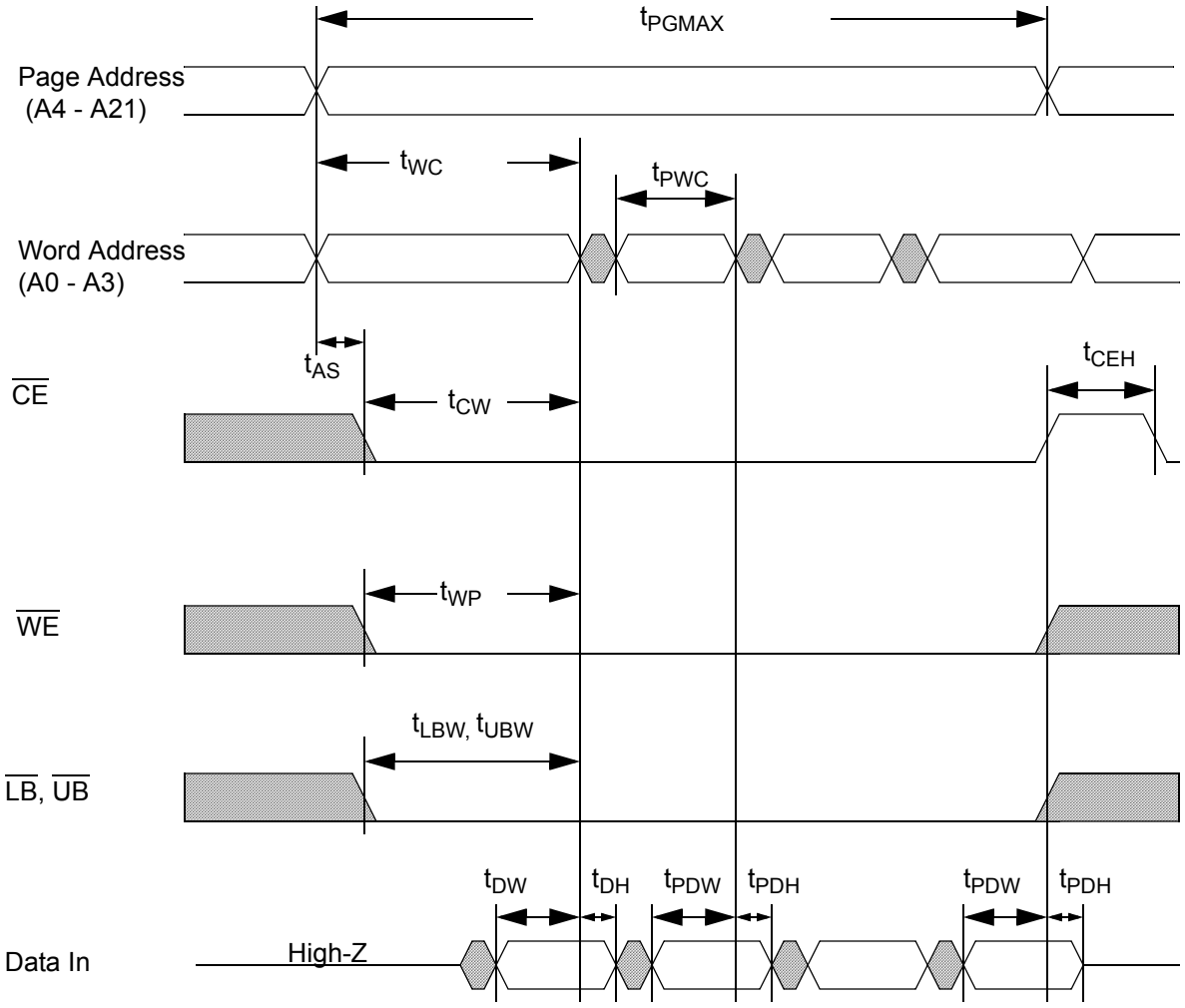


Figure 10: Timing Waveform of Page Mode Write Cycle



t_{PGMAX} means any page address (A4-A21) must be changed at least once in a 20us period

Power Up Requirements

After power is applied to bring Vcc and VccQ up, $\overline{CE}$ should be brought high. Once $\overline{CE}$ is high, a 150μs delay is required to ensure proper operation. After a 150μs delay, the device is now ready for operation or programming of the mode register.

Power Savings Modes

In the N64T1630C1B device there are several power savings modes. The three modes are:

- **Partial Array Self Refresh**
- **Temperature Compensated Refresh**
- **Deep Sleep Mode**

The operation of the power saving modes is controlled by the settings of bits contained in the Mode Register. This definition of the Mode Register is shown in Figure 11 and the various bits are used to enable and disable the various low power modes as well as enabling Page Mode operation. The Mode Register is set by using the timings defined in Figure 12.

1) Partial Array Self Refresh (PAR)

In this mode of operation, the internal refresh operation can be restricted to a 16Mb, 32Mb or 48Mb portion of the array. The array partition to be refreshed is determined by the respective bit settings in the Mode Register. The register settings for the PASR operation are defined in Table 10. In this PASR mode, when $\overline{ZZ}$ is active low, only the portion of the array that is set in the register is refreshed. The data in the remainder of the array will be lost. The PASR operating mode is only available during standby time ($\overline{ZZ}$ low) and once $\overline{ZZ}$ is returned high, the device resumes full array refresh. All future PASR cycles will use the contents of the Mode Register that has been previously set. To change the address space of the PASR mode, the Mode Register must be reset using the previously defined procedures. For PASR to be activated, the register bit, A4 must be set to a '1' value, "PASR Enabled". If this is the case, PASR will be activated 10us after $\overline{ZZ}$ is brought low. If the A4 register bit is set equal to '0', PASR will not be activated.

2) Temperature Compensated Refresh (TCR)

In this mode of operation, the internal refresh rate can be optimized for the operating temperature used an this can then lower standby current. The DRAM array in the PSRAM must be refreshed internally on a regular basis. At higher temperatures, the DRAM cell must be refreshed more often than at lower tempertures. By setting the temperature of operation in the Mode Register, this refresh rate can be optimized to yield the lowest standby current at the given operating temperature. There are four different temperature settings that can be programmed in to the PSRAM. These are defined in Figure 11.

3) Deep Sleep Mode

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing $\overline{ZZ}$ low with the A4 register bit set to a '0', "Deep Sleep Enabled". If this is the case, Deep Sleep will be entered 10us after $\overline{ZZ}$ is brought low. The device will remain in this mode as long as $\overline{ZZ}$ remains low. If the A4 register bit is set equal to '1', Deep Sleep will not be activated.

Other Mode Register Settings

The Page Mode operation can also be enabled and disabled using the Mode Register. Register bit A7 controls the operation of Page Mode and setting this bit to a '1', enables Page Mode. If the register bit A7 is set to a '0', Page Mode operation is disabled.

Figure 11: Mode Register

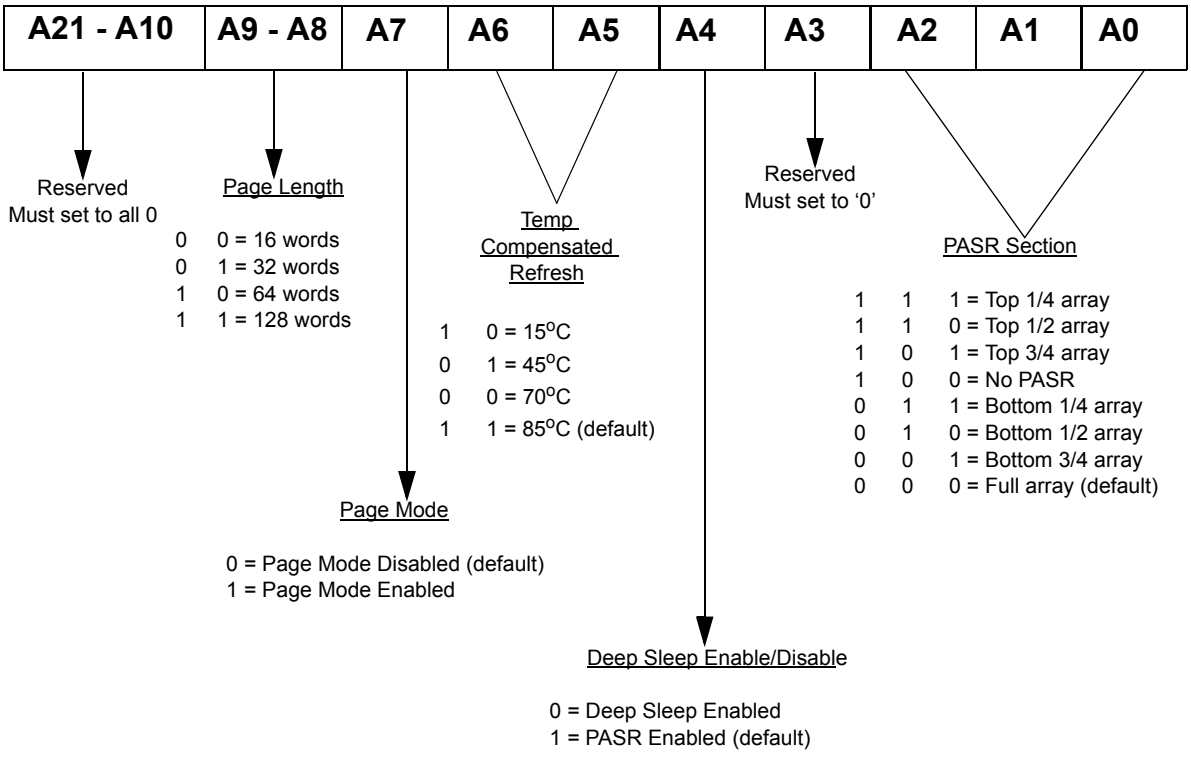


Figure 12: Mode Register Update Timings ($\overline{UB}$, $\overline{LB}$, $\overline{OE}$ are Don't Care)

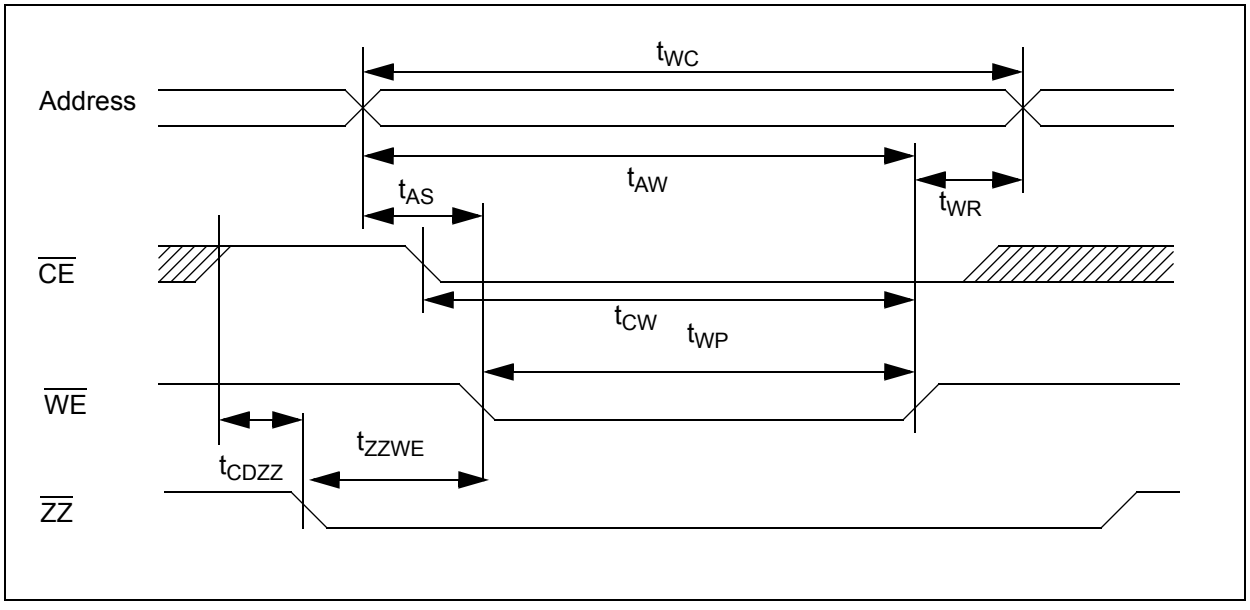


Figure 13: Deep Sleep Mode - Entry/Exit Timings

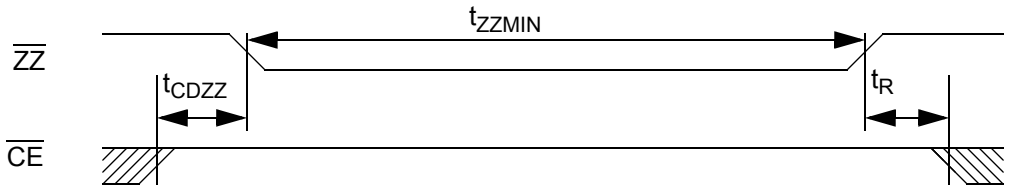


Table 9: Mode Register Update and Deep Sleep Timings

Item	Symbol	Min	Max	Unit	Note
Chip deselect to $\overline{ZZ}$ low	t_{CDZZ}	5		ns	
$\overline{ZZ}$ low to $\overline{WE}$ low	t_{ZZWE}	10	500	ns	
Write register cycle time	t_{WC}	70/85		ns	1
Chip enable to end of write	t_{CW}	70/85		ns	1
Address valid to end of write	t_{AW}	70/85		ns	1
Write recovery time	t_{WR}	0		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WR}	40		ns	
Deep Sleep Pulse Width	t_{ZZMIN}	10		us	
Deep Sleep Recovery	t_R	150		us	

1) Minimum cycle time for writing register is equal to speed grade of product.

Table 10: Address Patterns for PASR (A4 = 1)

A2	A1	A0	Active Section	Address space	Size	Density
1	1	1	Top quarter of die	300000h - 3FFFFFh	1Mb x 16	16Mb
1	1	0	Top half of die	200000h - 3FFFFFh	2Mb x 16	32Mb
1	0	1	Top three quarter of die	100000h - 3FFFFFh	3Mb x 16	48Mb
1	0	0	No PASR	None	0	0
0	1	1	Bottom quarter of die	000000h - 0FFFFFh	1Mb x 16	16Mb
0	1	0	Bottom half of die	000000h - 1FFFFFh	2Mb x 16	32Mb
0	0	1	Bottom three quarter of die	000000h - 2FFFFFh	3Mb x 16	48Mb
0	0	0	Full array	000000h - 3FFFFFh	4Mb x 16	64Mb

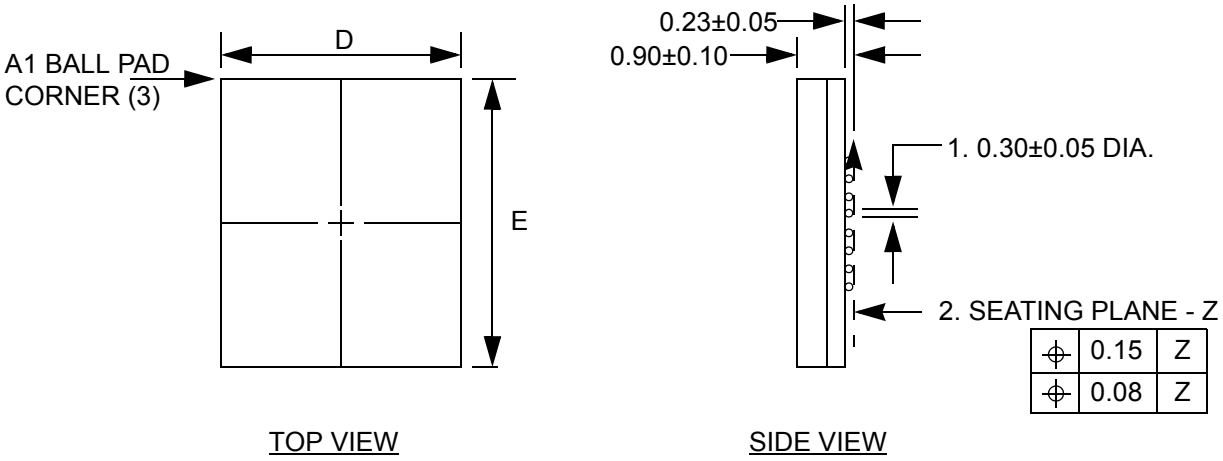
Table 11: Deep ICC Characteristics for N64T1630C1B

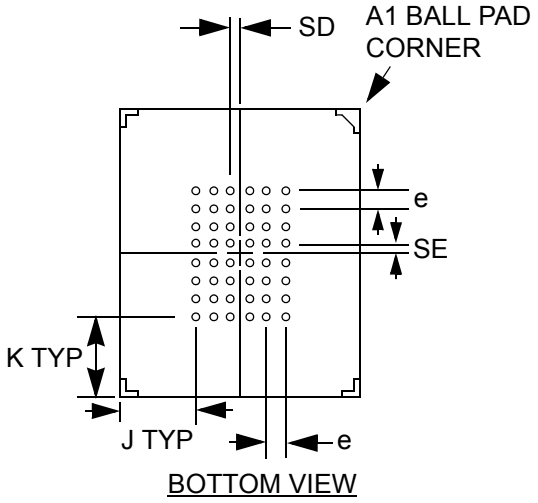
Item	Symbol	Test	Array Partition	Typ	Max	Unit
PASR Mode Standby Current	I_{PASR}	V_{IN} = V_{CC} or 0V, Chip Disabled, t_A= 85°C	None		70	µA
			1/4 Array		105	
			1/2 Array		110	
			3/4 Array		115	
			Full Array		170	

Item	Symbol	Max Temperature	Typ	Max	Unit
Temperature Compensated Refresh Current	I_{TCR}	15°C		70	µA
		45°C		85	
		70°C		105	
		85°C		170	

Item	Symbol	Test	Typ	Max	Unit
Deep Sleep Current	I_{ZZ}	V_{IN} = V_{CC} or 0V, Chip in $\overline{ZZ}$ mode, t_A= 25°C	30		µA

Package Dimensions





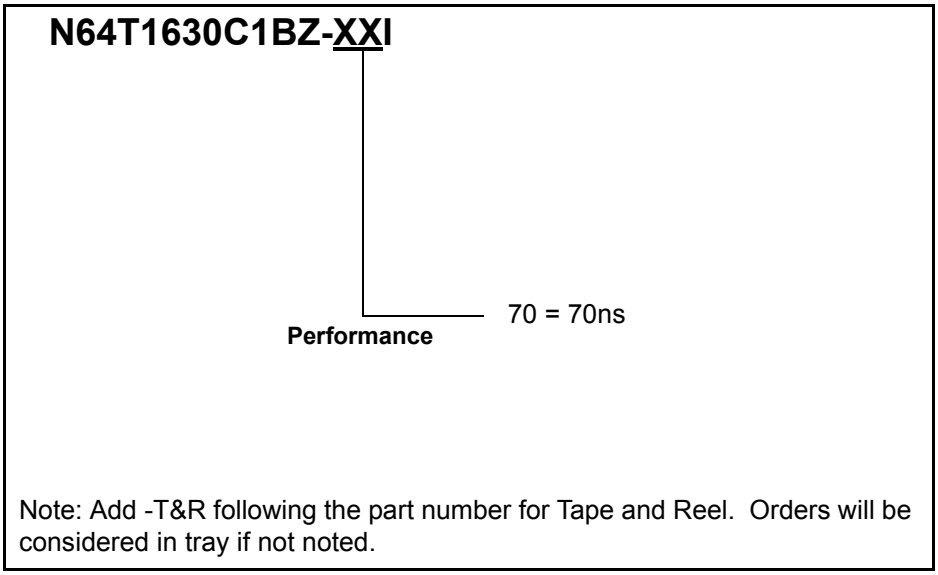
1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Figure 14: Ordering Information



Note: Add -T&R following the part number for Tape and Reel. Orders will be considered in tray if not noted.

Table 12: Revision History

Revision	Date	Change Description
A	June 2004	Original ADVANCED Datasheet
B	January 2005	Changed maximum Vcc rating
C	January 2005	General Update
D	May 2005	Isb change to 170uA
E	July 2005	Changed Vih to 0.8VccQ