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NAND GATES: 4011 QUAD 2 INPUT 4012 DUAL 4 INPUT 4023 TRIPLE 3 INPUT

GENERAL DESCRIPTION

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No. DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

The MMC 4011, MMC 4012 and MMC 4023E/F/G/H NAND gates provide the system designer with direct implementation of the NAND function. All inputs and outputs are buffered.
The MMC 4011, MMC 4012 and MMC 4023E/F/G/H types are supplied in 14-lead hermetic dual-in-line ceramic or plastic packages.

FEATURES

- Propagation delay time = 60 ns (typ.) at C_L = 50 pF, V_{DD} = 10 V
- Buffered inputs and outputs
- 5 V, 10 V and 15 V parametric ratings
- 100% tested quiescent current
- High noise immunity 0.45 V_{DD} (typical)

APPLICATIONS

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage:	G and H types	-0.5 to	20	V
		E and F types	-0.5 to	18	V
V_I	Input voltage		-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)			±10	mA
P_{tot}	Total power dissipation (per package)			200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range			100	mW
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	-40 to	85	°C
T_{stg}	Storage temperature		-65 to	150	°C

* All voltages are referred to V_{SS} pin voltage

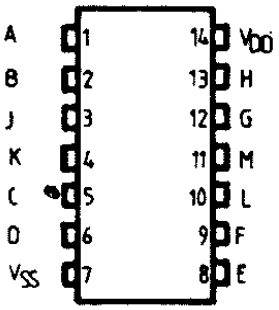
RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage:	G and H types	3 to	18	V
		E and F types	3 to	15	V
V_I	Input voltage		0 to	V_{DD}	V
T_A	Operating temperature :	G and H types	-55 to	125	°C
		E and F types	40 to	95	°C

CONNECTION DIAGRAMS

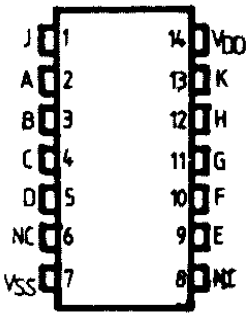
MMC 4011

$J = \overline{A \cdot B}$
$K = \overline{C \cdot D}$
$L = \overline{E \cdot F}$
$M = \overline{G \cdot H}$



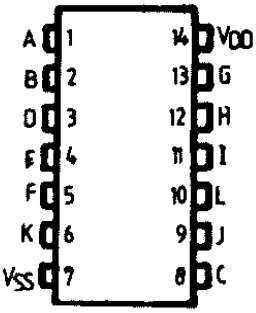
$J = \overline{A \cdot B \cdot C \cdot D}$
$K = \overline{E \cdot F \cdot G \cdot H}$

MMC 4012



$J = \overline{A \cdot B \cdot C}$
$K = \overline{D \cdot E \cdot F}$
$L = \overline{G \cdot H \cdot I}$

MMC 4023



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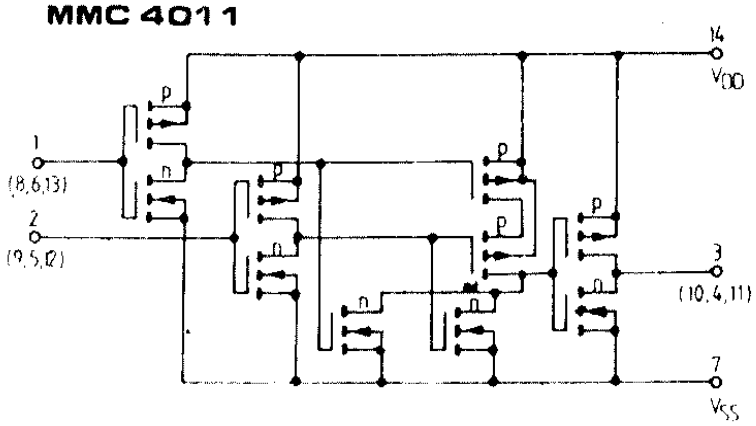
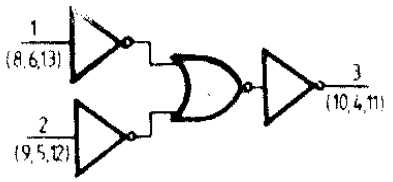
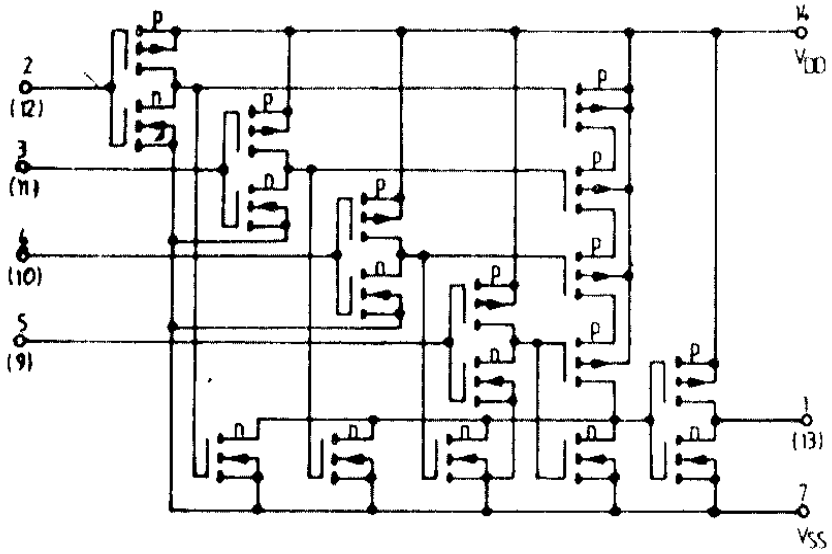
SCHEMATIC AND LOGIC DIAGRAMS

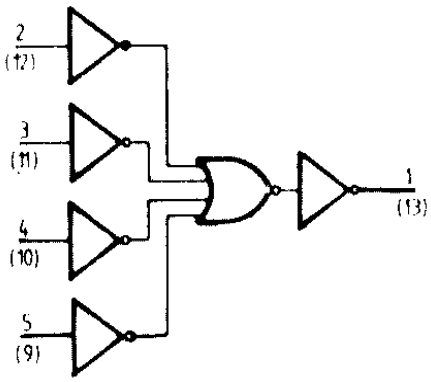
MMC 4011



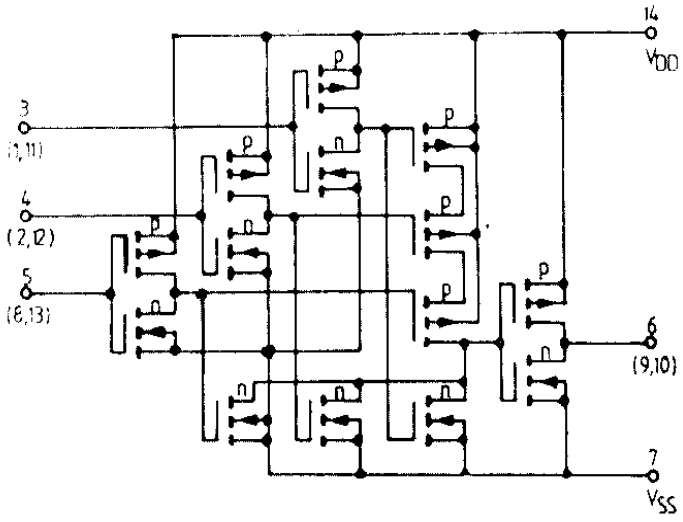


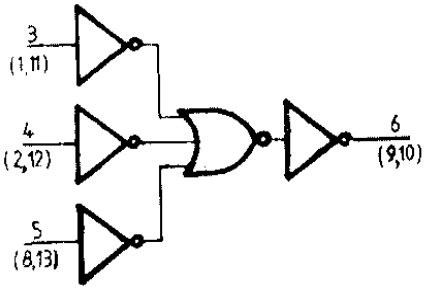
MMC 4012





MMC 4023





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STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNI
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
						min.	max.	min.	typ	max.	min.	max.	
I_L Quiescent current	G, H types	0/ 5			5		0.25		0.01	0.25		7.5	μA
		0/10			10		0.5		0.01	0.5		15	
		0/15			15		1		0.01	1		30	
		0/20			20		5		0.02	5		150	
	E, F types	0/ 5			5		1		0.01	1		7.5	
		0/10			10		2		0.01	2		15	
		0/15			15		4		0.01	4		30	
V_{OH} Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH} Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL} Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH} Output drive current	G, H types	0/ 5	2.5		5	−2		−1.6	−3.2		−1.15		mA
		0/ 5	4.6		5	−0.64		−0.51	−1		−0.36		
		0/10	9.5		10	−1.6		−1.3	−2.6		−0.9		
		0/15	13.5		15	−4.2		−3.4	−6.8		−2.4		
	E, F types	0/ 5	2.5		5	−1.53		−1.36	−3.2		−1.1		
		0/ 5	4.6		5	−0.52		−0.44	−1		−0.36		
		0/10	9.5		10	−1.3		−1.1	−2.6		−0.9		
		0/15	13.5		15	−3.6		−3.0	−6.8		−2.4		
I_{OL} Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
C_I Input capacitance			Any input						5	7.5			pF

T_{LOW} = −55°C for G, H devices; 40° C for E, F devices.

T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

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DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200k, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

PARAMETER	TEST CONDITIONS	VALUES			UNIT
	V_{DD} (V)	min	typ	max	
t_{PLH}, t_{PHL} Propagation delay time	5		125	250	ns
	10		60	120	
	15		45	90	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	