

Description

The μ PB8286 and μ PB8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8- or 16-bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

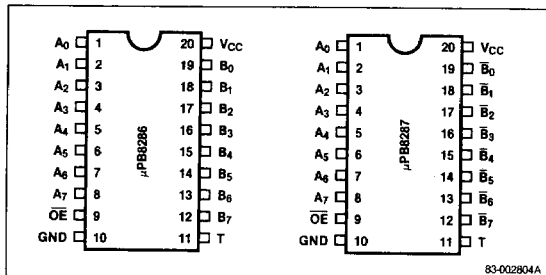
Features

- ☐ Data bus buffer driver for μ COM-8 (8080, 8085A, 780) and μ COM-16 (8086) families
- ☐ Low input load current – 0.2 mA max
- ☐ High output drive capability for driving system data bus
- ☐ Three-state outputs

Ordering Information

Part Number	Package Type	I/O Delay, Max
μ PB8286C	20-pin plastic DIP	22 ns
μ PB8287C	20-pin plastic DIP	30 ns

Pin Configurations



Pin Identification

No.	Symbol	Function
1-8	A ₀ -A ₇	Local data bus
9	OE	Output enable
10	GND	Ground
11	T	Transmit
12-19	(μ PB8286) B ₇ -B ₀ (μ PB8287) B ₇ -B ₀	System data bus
20	V _{CC}	Power supply

Pin Functions

$\overline{OE}$ (Output Enable)

This active low input control signal enables the output drivers selected by T.

T (Transmit)

This input controls the direction of data through the transceivers. When high, data is transferred from the A₀-A₇ inputs to the B₀-B₇ outputs. When low, data is transferred from the B₀-B₇ inputs to the A₀-A₇ outputs.

A₀-A₇ (Local Data Bus)

A₀-A₇ are bidirectional drivers that, depending on the state of the transmit pin, accept data from or transfer data to the processor's local bus.

B₀-B₇ (System Data Bus)

B₀-B₇ are bidirectional drivers that, depending on the state of the transmit pin, accept data from or transfer data to the system bus.

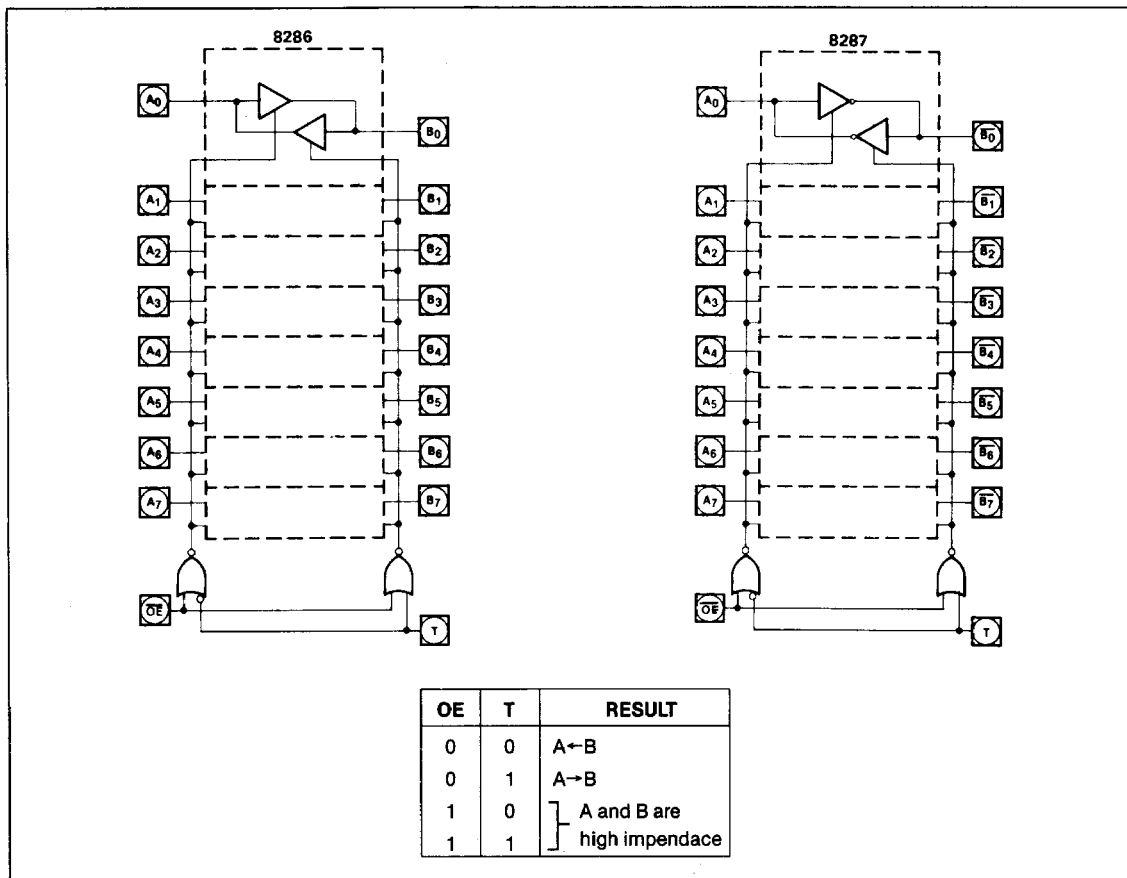
GND (Ground)

This is the ground.

V_{CC} (Power Supply)

This is the +5 V power supply.

Block Diagram



Functional Description

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.

These octal bus transceivers are designed to do the necessary buffering.

Bidirectional Driver

Each buffered line of the octal driver consists of two separate three-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side

of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

Control Gating, $\overline{OE}$, T

The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the A₀-A₇ inputs to the B₀-B₇ outputs, and when low, data is transferred from B₀-B₇ to the A₀-A₇ outputs.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$

Power supply voltage, V_{CC}	-0.5 V to +7 V
Input voltage, V_I	-1.0 V to +5.5 V
Output voltage, V_O	-0.5 V to +7 V
Operating temperature, T_{OPT}	0°C to $+70^\circ\text{C}$
Storage temperature, T_{STG}	-65°C to $+150^\circ\text{C}$

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +5\text{ V} \pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage low — A side	V_{IL}			+0.8	V	$V_{CC} = 5.0\text{ V}$, (Note 1)
				+0.9	V	$V_{CC} = 5.0\text{ V}$, (Note 1)
Input voltage high	V_{IH}		2		V	$V_{CC} = 5.0\text{ V}$, (Note 1), $F = 1\text{ MHz}$
Output voltage low — B outputs	V_{OL}			+0.45	V	$I_{OL} = 32\text{ mA}$
				+0.45	V	$I_{OL} = 16\text{ mA}$
Output voltage high — B outputs	V_{OH}	2.4			V	$I_{OH} = -5\text{ mA}$
		2.4			V	$I_{OH} = -1\text{ mA}$
Input clamp voltage	V_C		-1		V	$I_C = -5\text{ mA}$
Input forward current	I_F		-0.2		μA	$V_F = 0.45\text{ V}$
Input reverse current	I_R		50		μA	$V_R = 5.25\text{ V}$
Power supply current	I_{CC}					
				130	mA	μPB8287
				160	mA	μPB8286
Output off current	I_{OFF}		I_F			$V_{OFF} = 0.45\text{ V}$
Output off current	I_{OFF}		I_R			$V_{OFF} = 5.25\text{ V}$

Note:

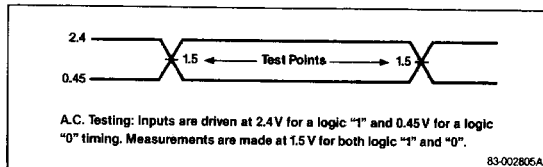
- (1) B outputs — $I_{OL} = 32\text{ mA}$, $I_{OH} = -5\text{ mA}$, $C_L = 300\text{ pF}$
 A outputs — $I_{OL} = 16\text{ mA}$, $I_{OH} = -1\text{ mA}$, $C_L = 100\text{ pF}$

AC Characteristics

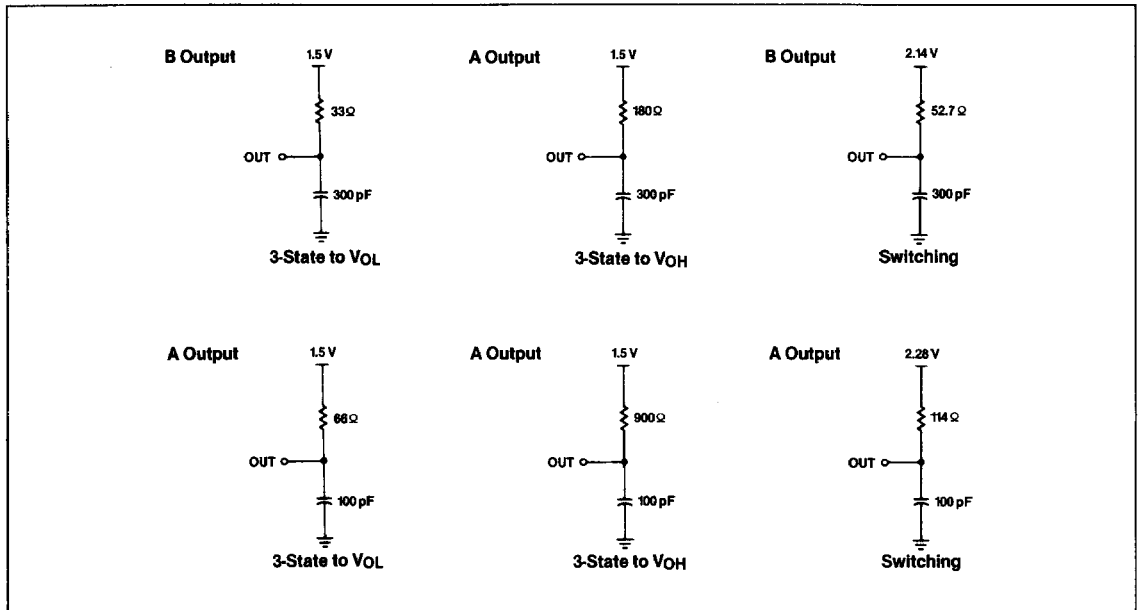
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input to output delay	t_{IVOV}					
Inverting		5		22	ns	
Non-inverting		5		30	ns	
Transmit / receive hold time	t_{EHTV}				ns	
Transmit / receive setup	t_{TVEL}	10			ns	
Output disable time	t_{EHOZ}	5		22	ns	
Output enable time	t_{ELOV}	10		30	ns	
I / O rise time	t_{ILIH} t_{OLOH}			20	ns	
I / O fall time	t_{IHIL} t_{OHOL}			12	ns	

AC Test Conditions



Test Load Circuits



Timing Waveform

