DATA SHEET

GPLD1160A

4 GS 96X64 / 80X80 LCD Driver

MAR. 28, 2008

Version 1.4

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4 GS 96/80-CH SEG AND 64/80-CH COM DRIVER

1. GENERAL DESCRIPTION

The GPLD1160A, a 4-gray scale dot matrix LCD driver with 96/80 SEG and 64/80 COM outputs.

With a built-in charge pump, GPLD1160A is able to generate a voltage of 2×/3×/4×/5×VDD depending on the configuration of external capacitors. In additional, a stable LCD driving voltage, VLCD, is also provided by a built-in BandGap reference and bias generation circuits.

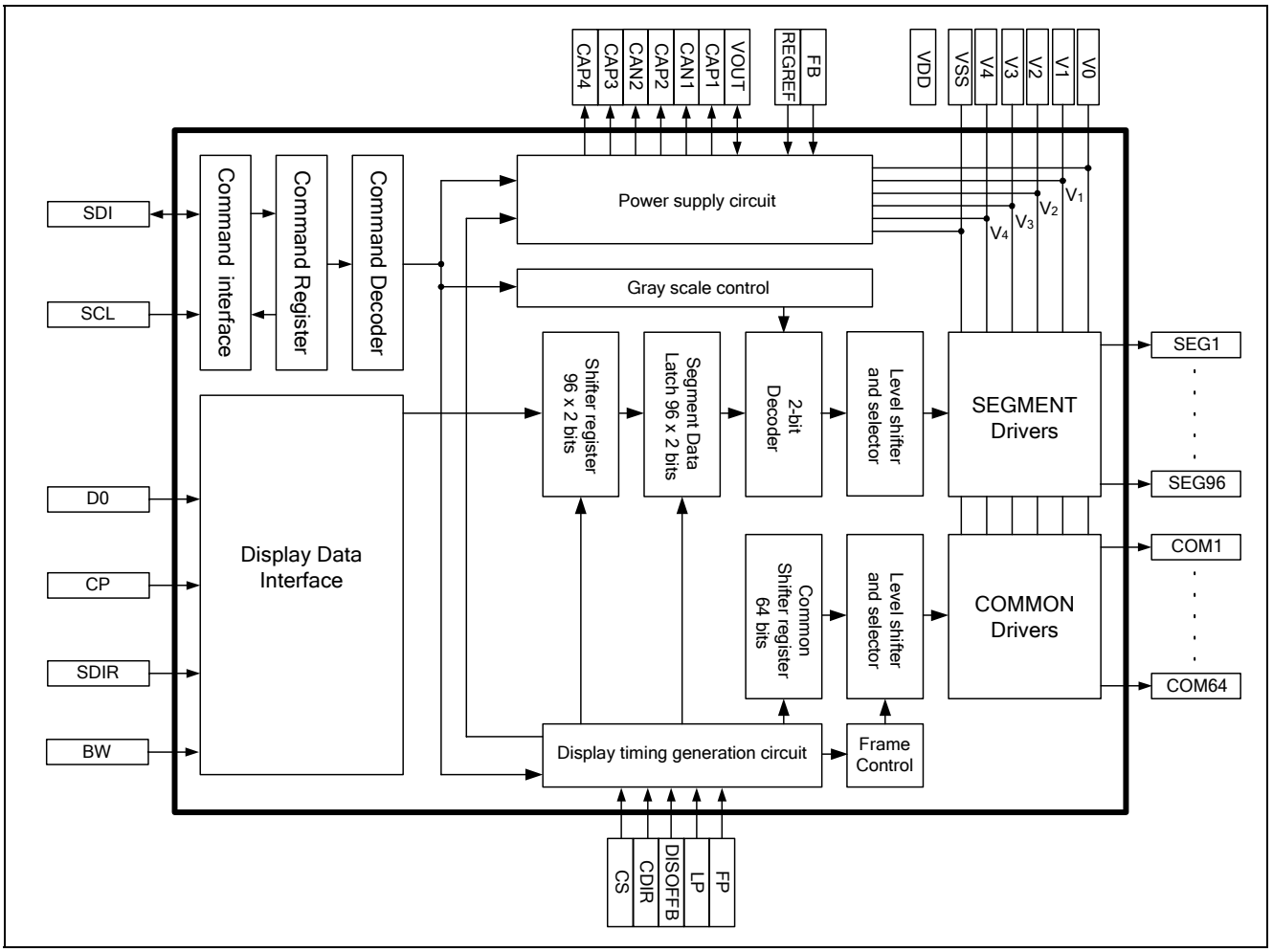
GPLD1160A sets the instructions by a serial interface that user can program the GPLD1160A at any time.

A flexible allocation of SEG/COM outputs is also implemented with GPLD1160A. With this feature, user can choose the most suitable SEG/COM allocation depending on the COG applications.

2. FEATURES

- Operation voltage for logic: 2.4V – 3.6V
- Driving voltage for LCD, V_{LCD}: 11V Max.
- Max. operating frequency 6.0MHz @ 3.3V
- 1-bit serial data input
- Bi-direction function for SEG and COM drivers
- Black-White / Gray mode option
- 4 gray scale can be selected form 16 gray scales
- Built-in charge pump circuit is able to provide 2x/3x/4x/5xVDD
- Built-in bias generation circuits
- 32 levels brightness control
- LCD dots: 96X64, 80X80
- Built-in bias control 1/9(96X64), 1/10(80X80) bias
- Display off function
- Package: COG

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	Type	Description
Y[1:160]	O	Common / Segment outputs.
CAP1	O	Coupling capacitor for charge pump.
CAN1	O	Coupling capacitor for charge pump.
CAP2	O	Coupling capacitor for charge pump.
CAN2	O	Coupling capacitor for charge pump.
CAP3	O	Coupling capacitor for charge pump.
CAP4	O	Coupling capacitor for charge pump.
VOUT	I/O	DC/DC voltage converter. Provide 2x/3x/4x/5xVDD by application circuit.
V0	I/O	The bias voltages for LCD driving.
V1	I/O	The bias voltages for LCD driving.
V2	I/O	The bias voltages for LCD driving.
V3	I/O	The bias voltages for LCD driving.
V4	I/O	The bias voltages for LCD driving.
FB	I	Gain adjustment input of V0. By adjusting the RA, RB ratio between V0, FB, and REGREF, a LCD driving voltage, V0, which is equal to V_{REF}x(1+RA/RB) can be obtained. V_{REF} is the internal reference voltage.
VDD	I	Power
VSS	I	GND
VSSP	I	The GND for Charge pump, must be independent ITO layout from PCB GND.
REGREF	I	Internal regulator reference.
CP	I	Clock input for shifting display data at the falling edge of CP.
LP	I	Line pulse input. Display data is latched to line buffer at the rising edge of LP. LP is used as shift clock of common driver, too.
FP	I	Frame pulse input. FP is the shift data input of common driver.
D0	I	Display data input.
SDIR	I	Bi-direction selection of segment driver.
CDIR	I	Bi-direction selection of common driver.
DISOFFB	I	Control input of chip enable/disable. When DISOFFB = 1, GPLD1160A operates normally. When DISOFFB = 0, GPLD1160A will be in a standby mode.
SDI	I	Data input of instruction interface.
SCL	I	Clock input of instruction interface.
CS	I	Common and segment selection, CS=1 96segX64com display, 1/9 bias CS=0 80segX80com display, 1/10 bias
BW	I	Black-white mode or 4 gray mode select. BW=0 4 gray mode BW=1 black-white mode

5. FUNCTION DESCRIPTIONS

5.1. Segment and Common Driver

5.1.1. The allocation of driver outputs

There are a variety of combinations of segment and common driver outputs with GPLD1160A. By setting CDIR and SDIR, user can change the allocations of segment and common outputs for their own application. Table1, Table2 shows these combinations.

Table1: Combinations of Segment and Common driver outputs When CS=1 the display is 96segX64con.

SDIR	CDIR	Segment Outputs			Common Outputs							
		SEG1	• • •	SEG96	COM1	COM2	• • •	COM32	COM33	• • •	COM63	COM64
0	0	Y33	• • •	Y128	Y32	Y31	• • •	Y1	Y129	• • •	Y159	Y160
0	1	Y33	• • •	Y128	Y160	Y159	• • •	Y129	Y1	• • •	Y31	Y32
1	0	Y128	• • •	Y33	Y32	Y31	• • •	Y1	Y129	• • •	Y159	Y160
1	1	Y128	• • •	Y33	Y160	Y159	• • •	Y129	Y1	• • •	Y31	Y32

Table2: Combinations of Segment and Common driver outputs When CS=0 the display is 80segX80con.

SDIR	CDIR	Segment Outputs			Common Outputs							
		SEG1	• • •	SEG80	COM1	COM2	• • •	COM40	COM41	• • •	COM79	COM80
0	0	Y41	• • •	Y120	Y40	Y39	• • •	Y1	Y121	• • •	Y159	Y160
0	1	Y41	• • •	Y120	Y160	Y159	• • •	Y121	Y1	• • •	Y39	Y40
1	0	Y120	• • •	Y41	Y40	Y39	• • •	Y1	Y121	• • •	Y159	Y160
1	1	Y120	• • •	Y41	Y160	Y159	• • •	Y121	Y1	• • •	Y39	Y40

Here, we define the 1st segment output as SEG1, 2nd segment output as SEG2, and so on, the same, COM1 is the 1st common output, and COM80 is the 80th common output. The corresponding output of segment or common outputs, YN, will be different when different CDIR and SDIR are set. For examples, when CS=1, CDIR=1 and SDIR=1, the corresponding outputs of SEG1, SEG96, COM1, COM64 will be Y128, Y33, Y160, Y32 respectively. In the following, we will use SEGN and COMN to represent the segment and common outputs in different CDIR and SDIR combinations instead of using YN.

5.1.2. Relationship between display data and segment driver

SDIR and BW determine the relationship between display data and segment output. SDIR and BW are input pins. BW is used to determine the display mode. When BW=1, the black-white mode is selected, there is only 1 bit data correspond to 1 pixel; when BW=0, the gray mode is selected, there are 2 bit data correspond to 1 pixel. SDIR is used to determine the shift direction.

Table3: Relationship of display data and driver output with black-white mode when CS=1

BW	SDIR	Input Data	Figure of Clock								
			CLK1	CLK2	CLK3	CLK4	• • •	CLK93	CLK94	CLK95	CLK96
1	0	D0	Y33	Y34	Y35	Y36	• • •	Y125	Y126	Y127	Y128
BW Mode	1	D0	Y128	Y127	Y126	Y125	• • •	Y36	Y35	Y34	Y33

Table4: Relationship of display data and driver output with 1 bit I/F and gray mode when CS=1

BW	SDIR	Input Data	Figure of Clock								
			CLK1	CLK2	CLK3	CLK4	• • •	CLK189	CLK190	CLK191	CLK192
0	0	D0	Y33(D0H)	Y33(D0L)	Y34(D0H)	Y34(D0L)	• • •	Y127(D0H)	Y127(D0L)	Y128(D0H)	Y128(D0L)
Gray	1	D0	Y128(D0H)	Y128(D0L)	Y127(D0H)	Y127(D0L)	• • •	Y34(D0H)	Y34(D0L)	Y33(D0H)	Y33(D0L)

GPLD1160A provides eight types of driving configurations for various applications:

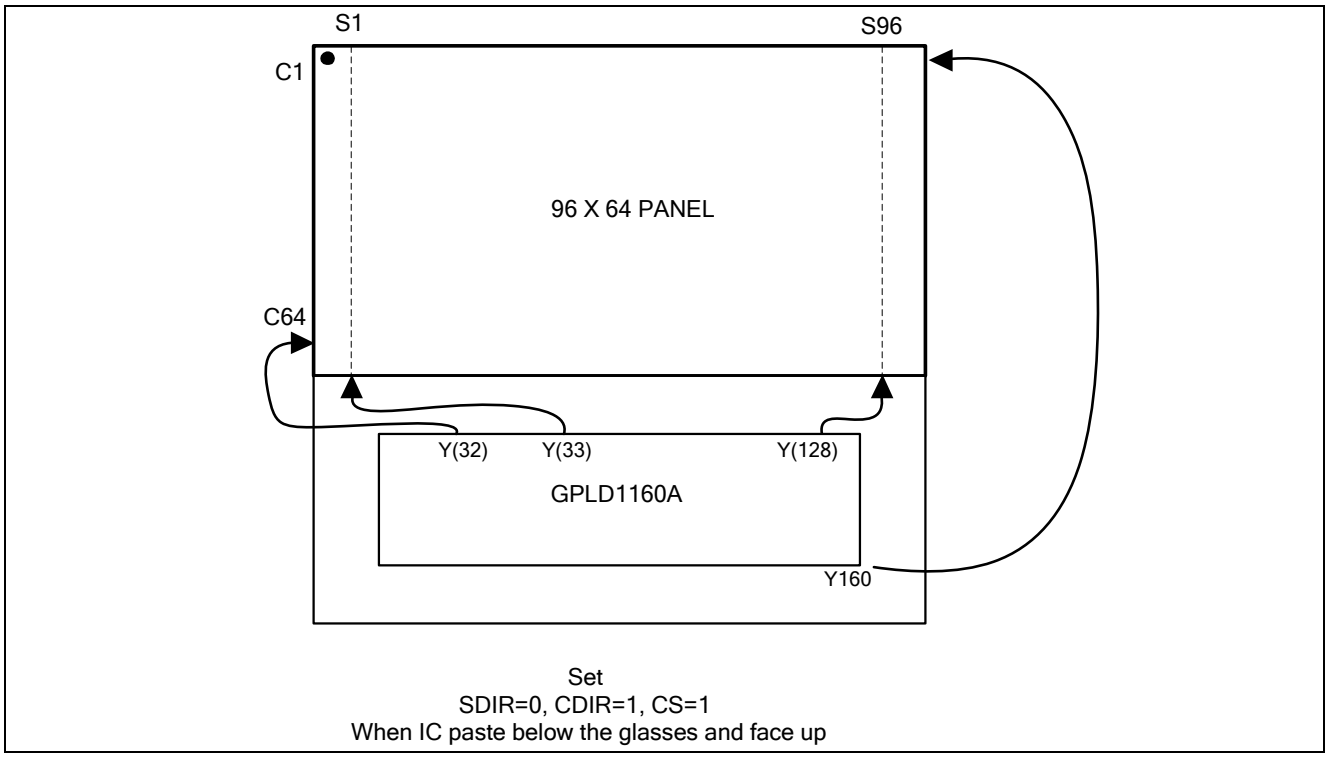
SDIR	CDIR	CS=1 96segX64con SEGMENT COMMON
0	0	S[1:96] = Y[33:128], C[1:32] = Y[32:1] C[33:64] = Y[129:160]
0	1	S[1:96] = Y[33:128], C[1:32] = Y[160:129] C[33:64] = Y[1:32]
1	0	S[1:96] = Y[128:33], C[1:32] = Y[32:1] C[33:64] = Y[129:160]
1	1	S[1:96] = Y[128:33], C[1:32] = Y[160:129] C[33:64] = Y[1:32]

SDIR	CDIR	CS=0 80segX80con SEGMENT COMMON
0	0	S[1:80] = Y[41:120], C[1:40] = Y[40:1] C[41:80] = Y[121:160]
0	1	S[1:80] = Y[41:120], C[1:40] = Y[160:121] C[41:80] = Y[1:40]
1	0	S[1:80] = Y[120:41], C[1:40] = Y[40:1] C[41:80] = Y[121:160]
1	1	S[1:80] = Y[120:41], C[1:40] = Y[160:121] C[41:80] = Y[1:40]

5.1.3. Relationship between common driver and panel layout

The GPLD1160A is COG, and it can paste on the glasses with face up or face down, above or below the glass.

Example: When GPLD1160A paste below the glasses and face up. That Y33 be Segment 1, and Y160 be Common 1, so Y128 is Segment 96 and Y32 is Common 64. Here we can set, SDIR=0, CDIR=1, CS=1 to use it.



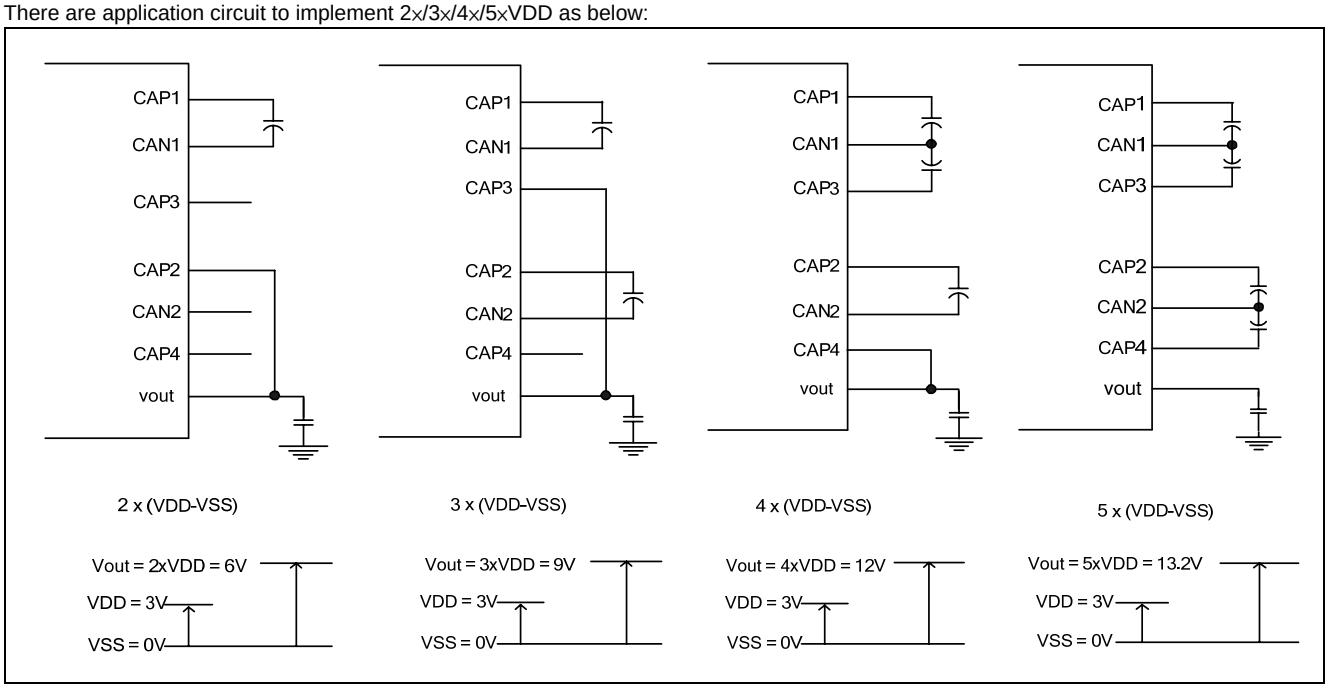
Set
SDIR=0, CDIR=1, CS=1
When IC paste below the glasses and face up

5.2. Built-in Bias Generation Circuits

5.2.1. Charge pump

Charge pump provide the highest voltage (V_{OUT}) for GPLD1160A. Built-in charge pump circuit is able to provide 2x/3x/4x/5xVDD

There are application circuit to implement 2x/3x/4x/5xVDD as below:



Note1: These capacitors are 0.1μF~1μF dependent on panel size (reference: 1.5 inch use 0.1μ, 2 inch use 0.22μ, >2.5inch use 1μ), if V_{OUT} > 13.2V then it will be clamped at 13.2V.

Note2: These capacitors are 1μF, if panel is big.

Note3: $V_{OUT} > V_0 + 1$

5.2.2. Regulator circuits

The booster voltage generated at V_{OUT} outputs, the liquid crystal driver voltage V_0 through the voltage regulator circuit. Because the GPLD1160A chips have an internal high-accuracy fixed voltage power supplies with a 32-level electronic volume function for the V_0 voltage regulator.

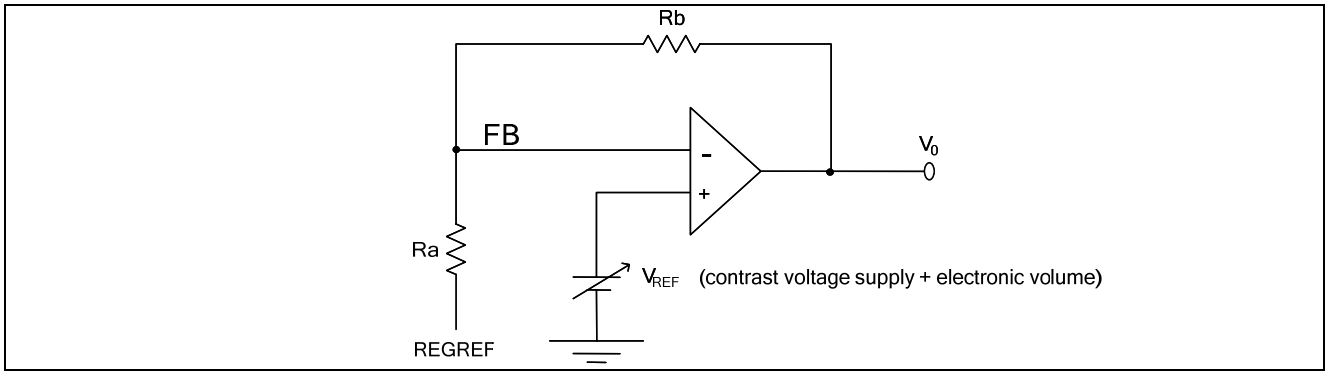
5.2.3. When the V_0 voltage regulator with external resistors are used

Through the use of the V_0 voltage regulator, external resistors and the electronic volume function, the liquid crystal power supply voltage, V_0, can be controlled by command alone, making it possible to adjust the liquid crystal display brightness. The V_0 voltage can be calculated by using equation E-1 over the range where $|V_0| < |V_{OUT}|-2V$

The Rb and Ra are external resisters.

$V_0 = (1 + Rb/Ra) \bullet V_{REF}$

$= (1 + Rb/Ra) \bullet (1 - \alpha/220) \bullet 2.2$ -------- E-1

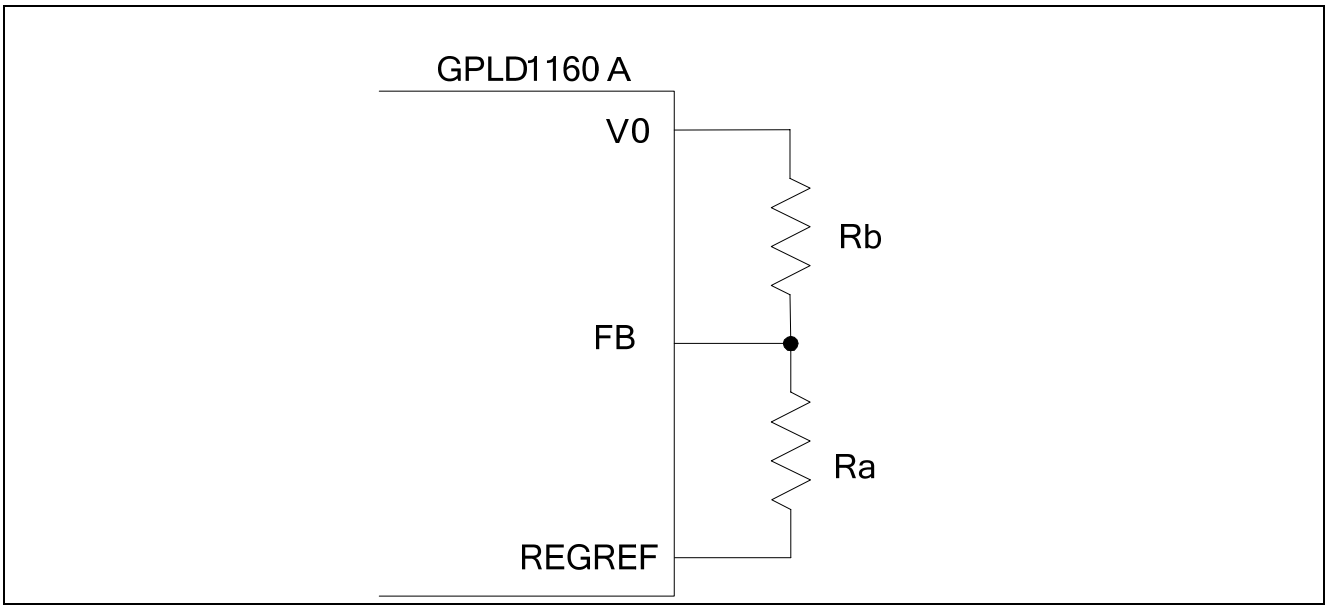


V_{REF} is the IC-internal fixed voltage supply and its voltage at T_A = 25°C is 2.04V. When use default value **S_4~S_0**.

For power saving please selection Rb > 1000K ohm (saving DC current from V0 through Rb, Ra to ground)

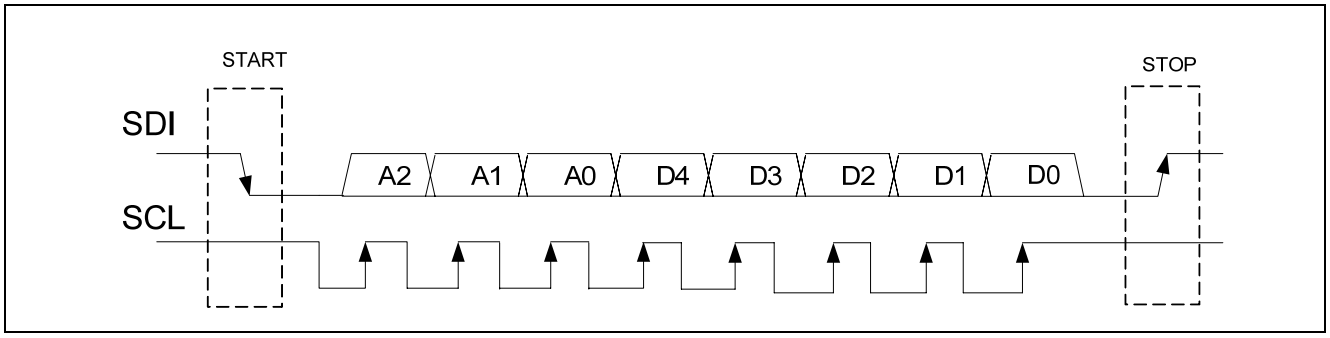
The α is set from 0 level to 31 possible levels by the electronic volume function depending on the data set in the 5-bit electronic volume register S_4~S_0. The following table shows the value for depending on the electronic volume register settings.

S_4	S_3	S_2	S_1	S_0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
:	:	:	:	:	:
0	1	1	1	1	16(default)
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0



5.3. Serial Communication Interface

By setting SDI to “Low” and SCL at “High”, GPLD1160A is able to receive serial input data. Serial data is input in the order of “A2, A1, A0, D4, D3, D2, D1, D0” from the serial data input pin (SDI) and be latched at the rising edge of serial clock (SCL). After the 8-bit data have been read into the shift register, the shift register will automatically convert serial data to change V0 voltage or gray scale.



Timing Diagram of Serial Data Transfer

5.4. Command Register A1, A0 and D5~D0 Data

A2	A1	A0	D4	D3	D2	D1	D0
0	1	0	S4	S3	S2	S1	S0
1	0	1	X	LUT13	LUT12	LUT11	LUT10
1	1	0	X	LUT23	LUT22	LUT21	LUT20

S[4:0] : Brightness control (default value 01111)

LUT1[3:0] gray level selection (default value 0100)
LUT2[3:0] gray level selection (default value 1010)

1st gray scale be fixed at GND

2nd gray scale selection registers [LUT13, LUT12, LUT11, LUT10].
For example: LUT13 ~ LUT10 = 0100,
2nd gray scale = Gray level 4

3rd gray scale selection registers [LUT23, LUT22, LUT21, LUT20].
For example: LUT23 ~ LUT20 = 1010,
3rd gray scale = Gray level 10

4th gray scale fixed at VDD.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Applicable Pins	Ratings	Unit
Supply Voltage (for Digital)	VDD	VDD	-0.3 ~ 3.6	V
Supply Voltage (for LCD)	V_{LCD}	V0	-0.3 ~ 13.5	V
Input Voltage (for Digital)	V_{I1}	FP, LP, CDIR, SDIR, CP, D0, SCL, SDI, CS, BW, DISOFFB	-0.3 ~ VDD + 0.3	V
Input Voltage (for LCD)	V_{I2}	V0, V1, V2, V3, V4, VOUT	-0.3 ~ V_{LCD} + 0.3	V
Storage Temperature	T_{STG}	NA	-50 ~ +150	℃

Note1: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

Note2: All the applied voltages are referenced to VSS (0V).

6.2. Recommended Operating Conditions

Characteristics	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit
Supply Voltage (for Digital)	VDD	VDD	2.4	-	3.6	V
Supply Voltage (for LCD)	V_{LCD}	V0	8.0	-	11	V
Operating Temperature	T_A	NA	0	-	70	℃

Note: All the applied voltages are referenced to VSS (0V).

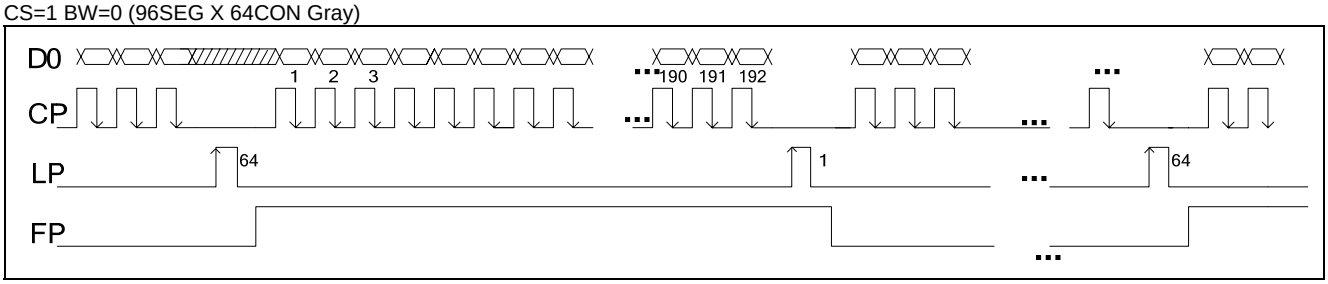
6.3. DC Characteristics (VDD = 2.4V - 3.6V, V_{LCD} = 8.0V - 11V, T_A = -20℃ ～ +70℃)

Characteristics	Symbol	Applicable Pins	Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IH}	FP, LP, DISOFFB, CDIR, CP, SDIR, D0, SCL, SDI, CS, BW	-	0.8xVDD	-	VDD	V
	V_{IL}		-	0	-	0.2xVDD	V
Input Leakage Current (1)	I_{LEAKH1}	FP, LP, DISOFFB, CDIR, CP, SDIR, D0, SCL, SDI, CS, BW	V_{I1} = VDD	-	-	1.0	μA
	I_{LEAKL1}		V_{I1} = VSS	-1.0	-	-	μA
Input Leakage Current (2)	I_{LEAKH2}	V0, V1, V2, V3, V4, VOUT	V_{I2} = 12V	-	-	5.0	μA
	I_{LEAKL2}		V_{I2} = 0V	-5.0	-	-	μA
Standby Current	I_{SB}	VSS	DISOFFB = VSS	-1.0	-	1.0	μA
Operating Current (1)	I_{DD}	VDD	Note1	-	-	400	μA
Output Resistance	R_{ON}	Y160 - 1	V_{LCD} = 9.0V, 1/9 Bias	-	-	1.5	KΩ

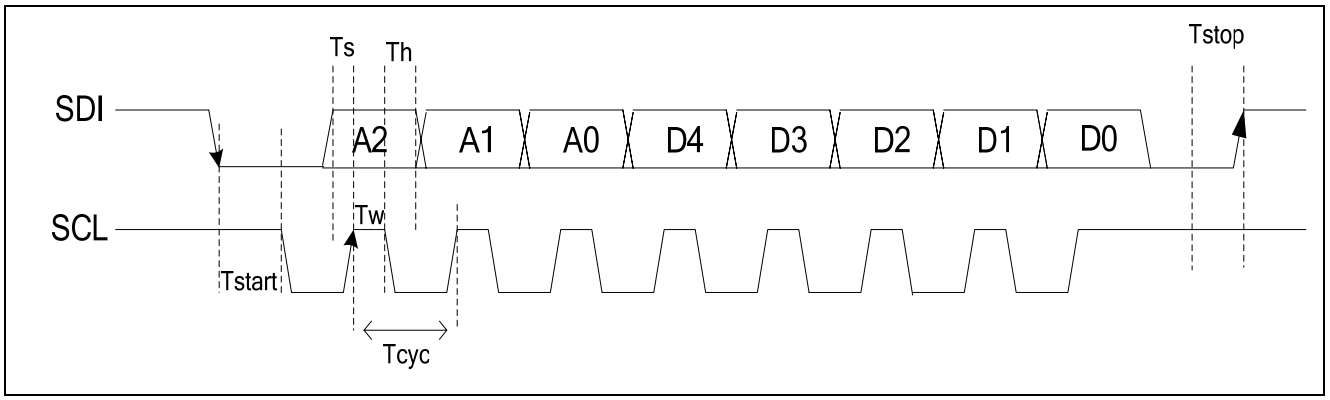
Note1: NO load, VDD = 3.3V, VLCD = 10V, CP = 1MHz, LP = 6.0KHz, FP = 75Hz.
DISOFFB = H, command register BW = 0;
The input data, D0, is latched by CP falling.

6.4. AC Characteristics

CS=1 BW=0 (96SEG X 64CON Gray)

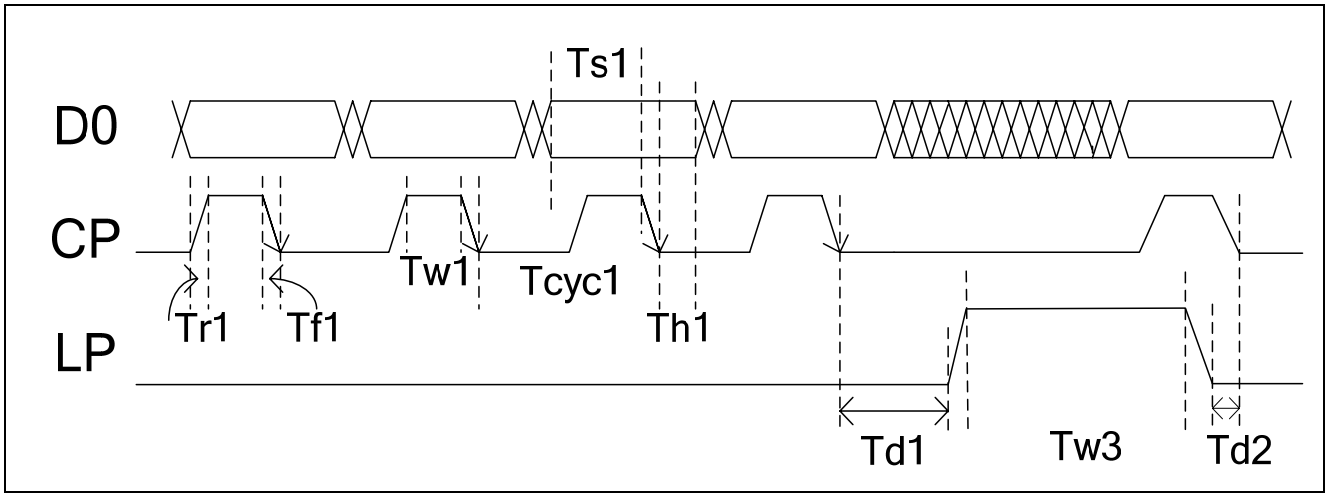


6.4.1. Timing characteristic of command interface:



Parameter	Symbol	Min.	Typ.	Max.	Unit
The Hold Time of SDI Falling to SCL Falling	Tstart	100	-	-	ns
SCL Period	Tcyc	200	-	-	ns
SCL High Width	Tw	50	-	-	ns
SCL Setup Time in Order to Latch SDI Data	Ts	50	-	-	ns
SDI Hold Time That Is from SCL Falling to SDI Change	Th	50	-	-	ns
SCL Rising to SDI Rising in Order to Load Data to Register	Tstop	50	-	-	ns

6.4.2. LCD control signal timing characteristic:

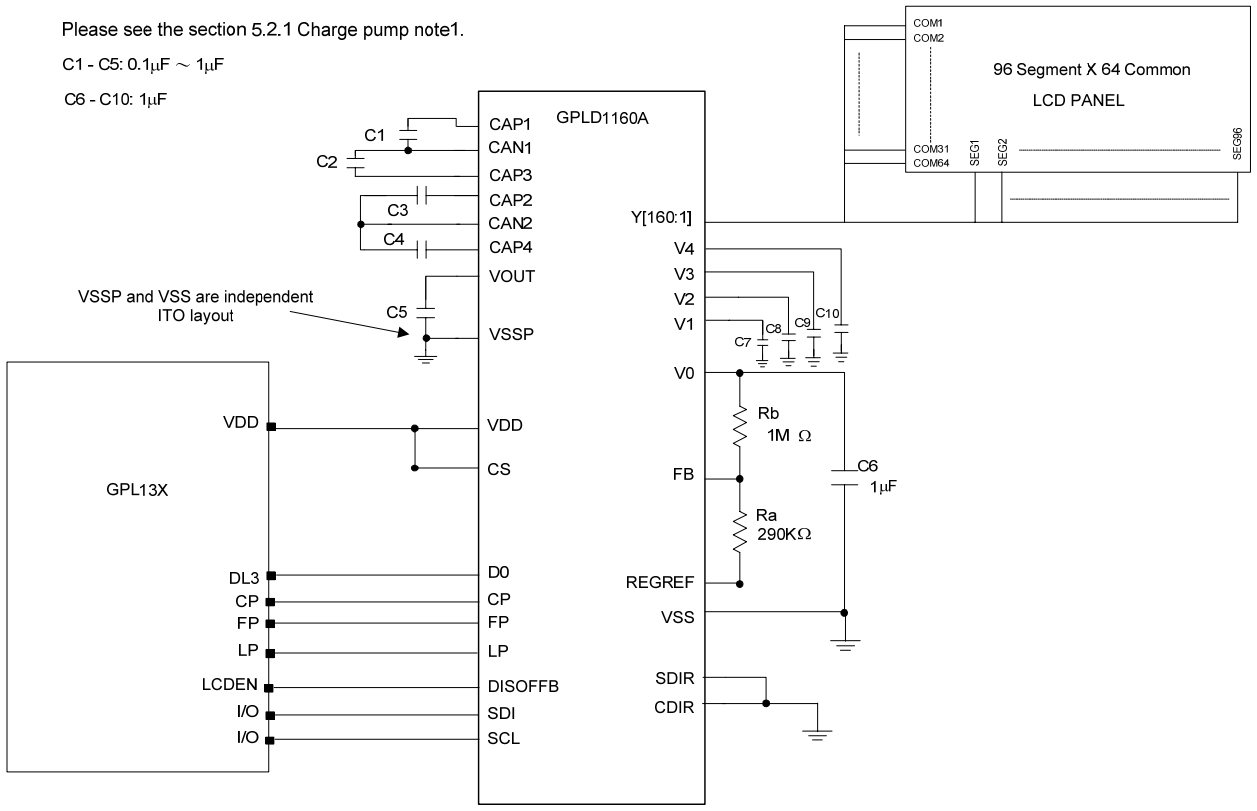


Parameter	Symbol	Min.	Typ.	Max.	Unit
CP Rising Time	Tr1	-	-	5	ns
CP Falling Time	Tf1	-	-	5	ns
CP Clock High Plus Width	Tw1	80	-	-	Ns
CP Clock Period	Tcyc1	200	-	-	Ns
The Setup Time That CP Clock Latch Data	Ts1	50	-	-	Ns
The Hold Time That CP Clock Latch Data	Th1	50	-	-	ns
The Delay Time from CP Falling to LP Rising	Td1	0	-	-	ns
The Timing from LP Falling to CP Falling	Td2	10	-	-	ns
LP Clock High Plus Width	Tw3	80	-	-	ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
LP Signal Rising Time	Tr2	-	-	5	ns
LP Signal Falling Time	Tf2	-	-	5	ns
LP Falling to FP Rising	Td3	0	-	-	ns
The Setup Time for LP to Latch FP	Ts2	200	-	-	ns
LP Pulse Width	Tw2	100	-	-	ns
LP Falling to FP Falling	Th2	0	-	-	ns

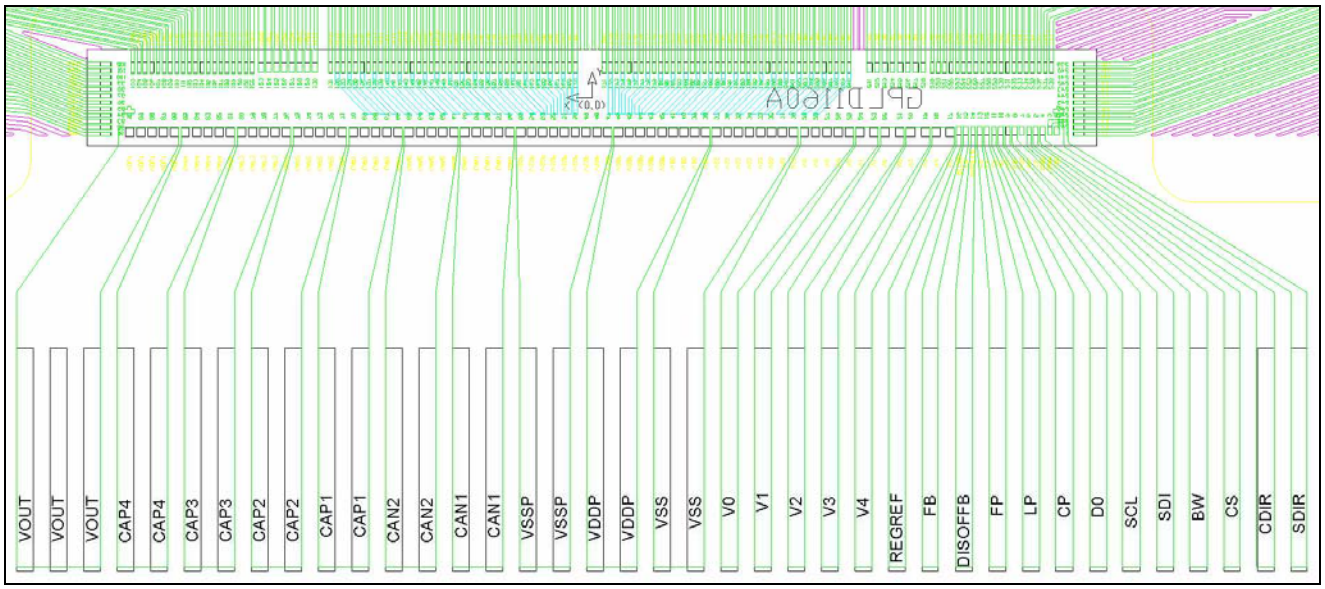
7. APPLICATION CIRCUITS

7.1. Application Circuit - (1)



Application 1 : GPLD1160A with 1-Bit interface Internal VLCD Bias Refrenc Generation

8. ITO Lay-Out Guideline

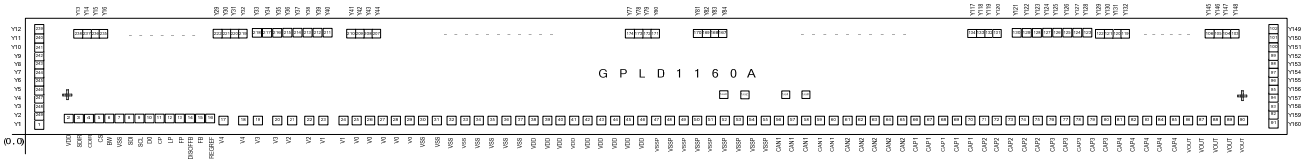


Note1: ITO resistance is 10 ohm/square.

Note2: VSSP and VSS pin must be independent ITO layout from PCB GND.

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment



This IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, bond all VDD and VSS pins.
Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

9.2. Ordering Information

Product Number	Package Type
GPLD1160A - C	Chip Form with Gold Bump

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 28, 2008	1.4	Add section 8. ITO Lay-out Guideline	14
FEB. 14, 2008	1.3	Modify the “Ordering Information” in section 8.2.	14
OCT. 05, 2007	1.2	1. Modify the “FEATURES” in section 2. 2. Modify the “SIGNAL DESCRIPTION” in section 4.	3 4
SEP. 21, 2007	1.1	Modify the “Timing characteristic of command interface” in section 6.4.1.	11
AUG. 07, 2007	1.0	1. Modify the V_{LCD} Max. value. 2. Modify the cap value in section 7. APPLICATION CIRCUITS.	13
JUN. 20, 2007	0.4	1. Delete VDDP description in section 4. 2. Modify the “Application Circuit” in section 7.1 3. Modify the “Pad Assignment” in section 8.1.	4 13 14
JUN. 06, 2007	0.3	Modify the “Pad Assignment” in section 8.1.	14
May 22, 2007	0.2	1. Modify the “BLOCK DIAGRAM” in section 3. 2. Modify the “Charge pump” in section 5.2.1. 3. Modify the “When the V_0 voltage regulator with external resistors are used” in section 5.2.3. 4. Add section 6.4.1 and 6.4.2. 5. Modify the “Application Circuit” in section 7.1. 6. Add section 8.1.	3 7 7 11 13 14
MAR. 30, 2007	0.1	Original	14