DATA SHEET

GPR25V0805F

2.3V-3.6V, 8M-Bit [x 1/x 2/x 4] CMOS MXSMIO® (Serial Multi I/O) Flash Memory

May 25, 2016

Version 1.0

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2.3V-3.6V, 8M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

1.1. General

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 8,388,608 x 1 bit structure
  or 4,194,304 x 2 bits (two I/O mode) structure
  or 2,097,152 x 4 bits (four I/O mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K/64K byte each
  - Any Block can be erased individually
- Single Power Supply Operation
  - Operation Voltage: 2.3V-3.6V for Read, Erase and Program Operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- **GPR25V0805F is compatible with MX25V8035F**

1.2. Performance

- High Performance
  - Fast read
  - 1 I/O: 108MHz with 8 dummy cycles
  - 2 I/O: 104MHz with 4 dummy cycles, equivalent to 208MHz
  - 4 I/O: 104MHz with 2+4 dummy cycles, equivalent to 416MHz
  - Fast program and erase time
  - 8/16/32/64 byte Wrap-Around Burst Read Mode
- Low Power Consumption
- Minimum 100,000 erase/program cycles
- 20 years data retention

1.3. Software Features

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
- Additional 8K bits secured OTP
  - Features unique identifier.
  - Factory locked identifiable and customer lockable
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector or block
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Command Reset
- Program/Erase Suspend and Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode
- Support Unique ID

1.4. Hardware Features

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- HOLD#/SIO3
  - HOLD feature, to pause the device without deselecting the device or Serial input & Output for 4 x I/O read mode
- PACKAGE
  - 8-pin SOP (200mil)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

GPR25V0805F is 8Mb bits Serial NOR Flash memory, which is configured as 1,048,576 x 8 internally. When it is in four I/O mode, the structure becomes 2,097,152 bits x 4 or 4,194,304 bits x 2.

GPR25V0805F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The GPR25V0805F MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

The GPR25V0805F reliably stores memory contents even after 100,000 program and erase cycles.

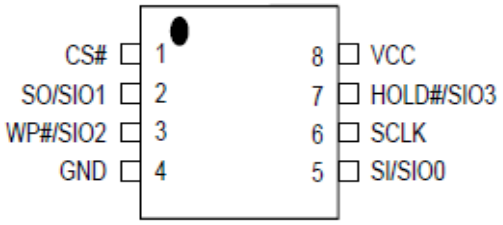
Table1. Additional Feature

Protection and Security	GPR25V0805F
Flexible Block Protection (BP0-BP3)	V
8K-bit security OTP	V

Fast Read Performance					
I/O	1 I/O	1I/2O	2 I/O	1I/4O	4 I/O
Dummy Cycle	8	8	4	8	6
Frequency	108MHz	104MHz	104MHz	104MHz	104MHz

3. PIN CONFIGURATIONS

3.1. 8-PIN SOP (200mil)

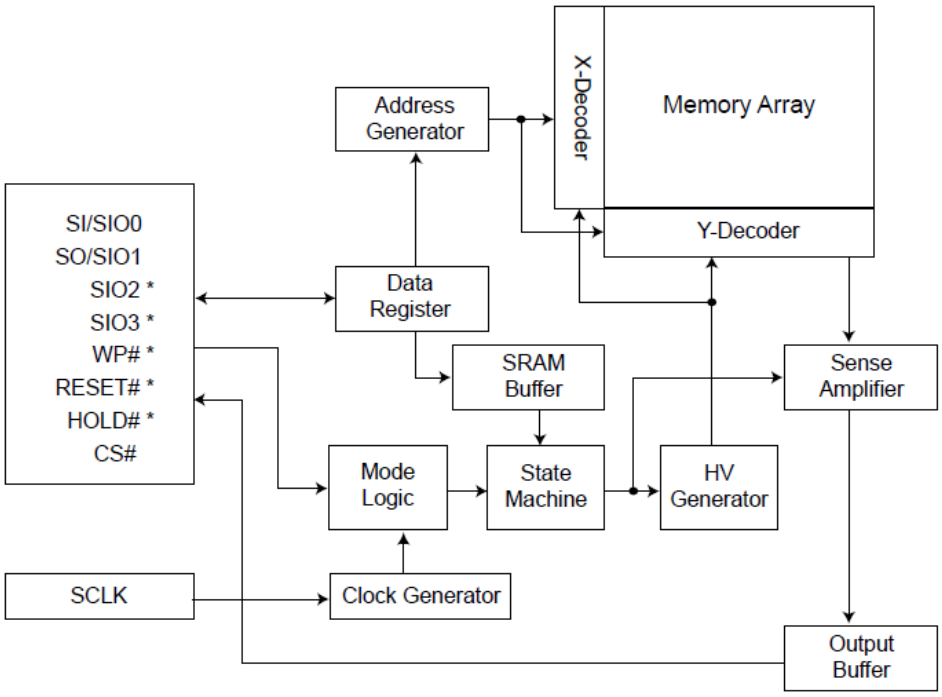


4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
HOLD#/SIO3	To pause the device without deselecting the device or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground

Note: HOLD# and WP# with internal pull high circuit.

5. BLOCK DIAGRAM



* Depends on part number options.

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

• Power-on reset: to avoid sudden power switch by system power supply transition, the power-on reset may protect the Flash.

• Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

• Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data.

• Deep Power Down Mode: By entering deep power down mode, the flash device is under protected from writing all commands except toggling the CS#. For more detail please see "10-24. Deep Power-down (DP)".

• Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as "Table 2. Protected Area Sizes", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect (SRWD) bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	8Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 15th)
0	0	1	0	2 (2blocks, block 14th-15th)
0	0	1	1	3 (4blocks, block 12th-15th)
0	1	0	0	4 (8blocks, block 8th-15th)
0	1	0	1	5 (16blocks, protect all)
0	1	1	0	6 (16blocks, protect all)
0	1	1	1	7 (16blocks, protect all)
1	0	0	0	8 (16blocks, protect all)
1	0	0	1	9 (16blocks, protect all)
1	0	1	0	10 (16blocks, protect all)
1	0	1	1	11 (16blocks, protect all)
1	1	0	0	12 (16blocks, protect all)
1	1	0	1	13 (16blocks, protect all)
1	1	1	0	14 (16blocks, protect all)
1	1	1	1	15 (16blocks, protect all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	8Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)

Status bit				Protect Level
BP3	BP2	BP1	BP0	8Mb
0	0	1	1	3 (4blocks, block 0th-3rd)
0	1	0	0	4 (8blocks, block 0th-7th)
0	1	0	1	5 (16blocks, protect all)
0	1	1	0	6 (16blocks, protect all)
0	1	1	1	7 (16blocks, protect all)
1	0	0	0	8 (16blocks, protect all)
1	0	0	1	9 (16blocks, protect all)
1	0	1	0	10 (16blocks, protect all)
1	0	1	1	11 (16blocks, protect all)
1	1	0	0	12 (16blocks, protect all)
1	1	0	1	13 (16blocks, protect all)
1	1	1	0	14 (16blocks, protect all)
1	1	1	1	15 (16blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 8K-bit secured OTP for unique identifier: to provide 8K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

The 8K-bit secured OTP area is composed of two rows of 4K-bit. Customer could lock the first 4K-bit OTP area and factory could lock the other.

- Security register bit 0 indicates whether the 2nd 4K-bit is locked by factory or not.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "Table 11. Security Register Definition" for security register bit definition and table of "Table 3. 8K-bit Secured OTP Definition" for address range definition.
- To program 8K-bit secured OTP by entering secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting secured OTP mode by writing EXSO command.

Note: Once lock-down whatever by factory or customer, the corresponding secured area cannot be changed any more. While in 8K-bit Secured OTP mode, array access is not allowed.

Table3. 8K-bit Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

7. MEMORY ORGANIZATION

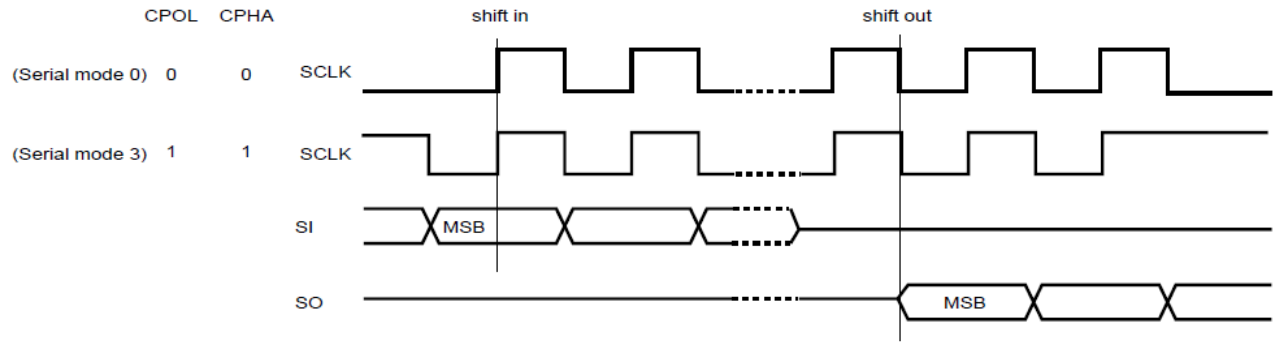
Table 4. Memory Organization

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31 | 30	255	0FF000h	0FFFFFh
		:	:	:
		240	0F0000h	0F0FFFh
14	29 | 28	239	0EF000h	0EFFFFh
		:	:	:
		224	0E0000h	0E0FFFh
13	27 | 26	223	0DF000h	0DFFFFh
		:	:	:
		208	0D0000h	0D0FFFh
12	25 | 24	207	0CF000h	0CFFFFh
		:	:	:
		192	0C0000h	0C0FFFh
11	23 | 22	191	0BF000h	0BFFFFh
		:	:	:
		176	0B0000h	0B0FFFh
10	21 | 20	175	0AF000h	0AFFFFh
		:	:	:
		160	0A0000h	0A0FFFh
9	19 | 18	159	09F000h	09FFFFh
		:	:	:
		144	090000h	090FFFh
8	17 | 16	143	08F000h	08FFFFh
		:	:	:
		128	080000h	080FFFh
7	15 | 14	127	07F000h	07FFFFh
		:	:	:
		112	070000h	070FFFh
6	13 | 12	111	06F000h	06FFFFh
		:	:	:
		96	060000h	060FFFh
5	11 | 10	95	05F000h	05FFFFh
		:	:	:
		80	050000h	050FFFh
4	9 | 8	79	04F000h	04FFFFh
		:	:	:
		64	040000h	040FFFh
3	7 | 6	63	03F000h	03FFFFh
		:	:	:
		48	030000h	030FFFh
2	5 | 4	47	02F000h	02FFFFh
		:	:	:
		32	020000h	020FFFh
1	3 | 2	31	01F000h	01FFFFh
		:	:	:
		16	010000h	010FFFh
0	1 | 0	15	00F000h	00FFFFh
		:	:	:
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Figure 1. Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDCR, RDSCUR, READ, FAST_READ, DREAD, 2READ, 4READ, QREAD, RDSFDP, RES, REMS, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, SUSPEND, RESUME, NOP, RSTEN, RST, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note: CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2.Serial Input Timing

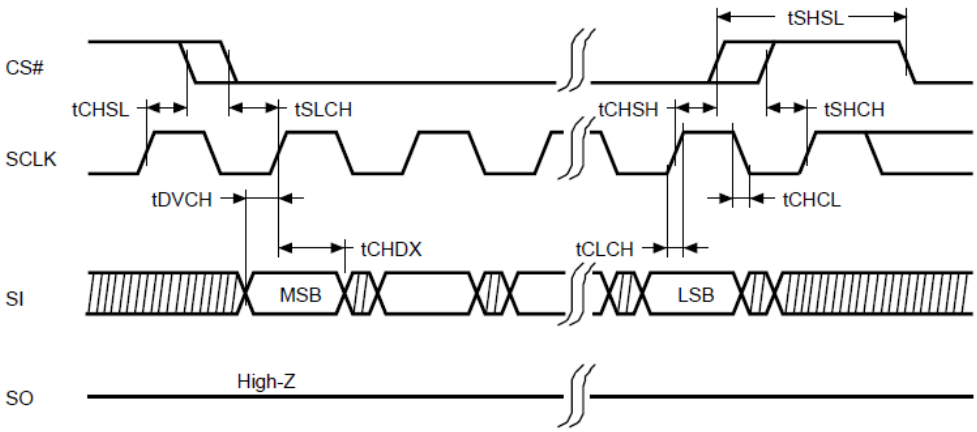


Figure 3. Output Timing

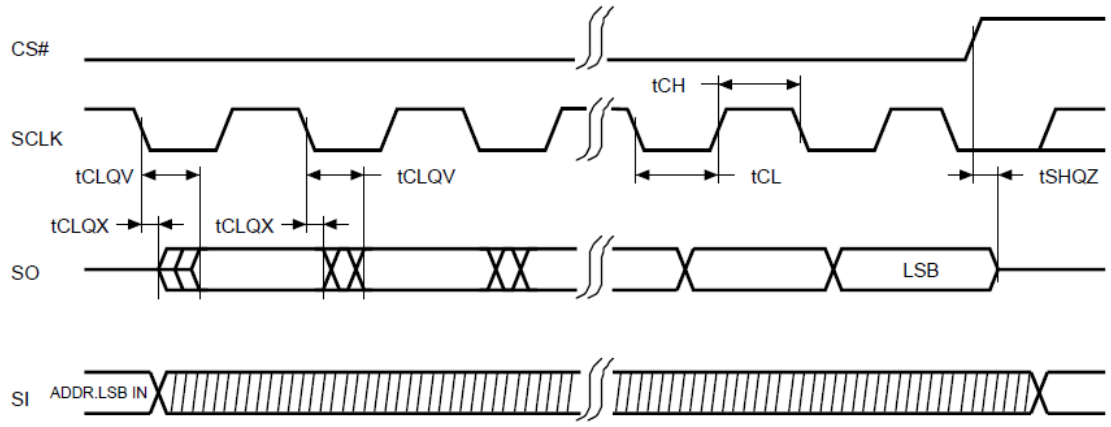
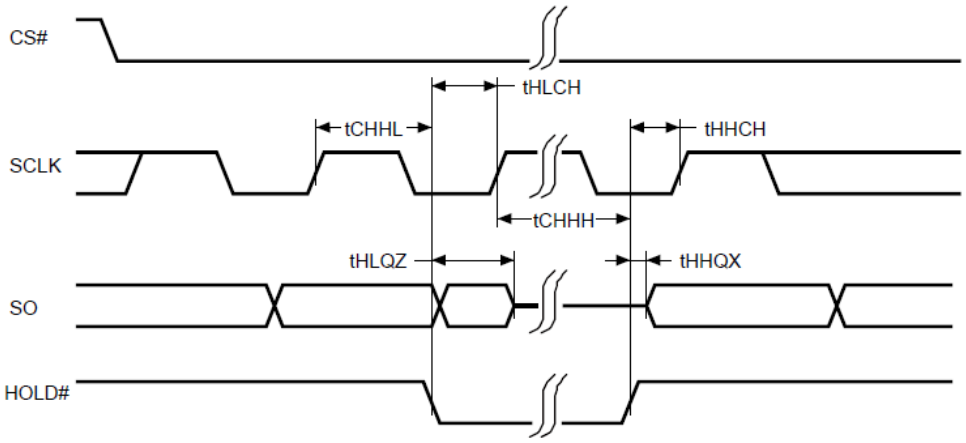


Figure 4. Hold Timing



* SI is "don't care" during HOLD operation.

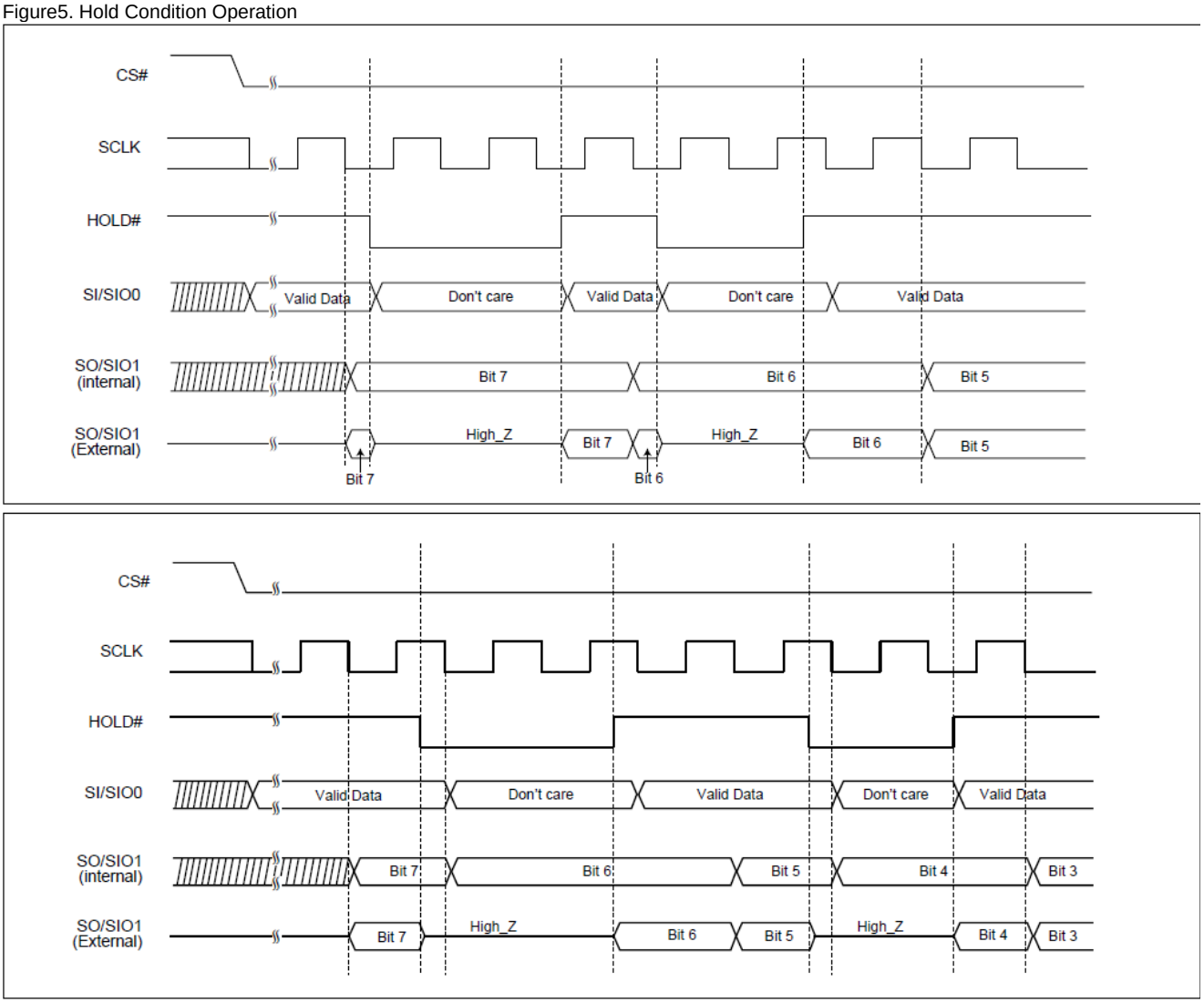
9. HOLD FEATURE

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low).

The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock(SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low).

Figure5. Hold Condition Operation



During the HOLD operation, the Serial Data Output (SO) is high impedance when Hold# pin goes low and will keep high impedance until Hold# pin goes high. The Serial Data Input (SI) is don't care if both Serial Clock (SCLK) and Hold# pin goes low and will keep the state until SCLK goes low and Hold# pin goes high. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

Note: The HOLD feature is disabled during Quad I/O mode.

10. COMMAND DESCRIPTION

Table5. Command Sets

Read/Write Array Commands

I/O	1	1	2	2	4	4
Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	4READ (4 x I/O read)	QREAD (1I/4O read)
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy	Dummy	Dummy	Dummy	Dummy
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual Output until CS# goes high	Quad I/O read with 6 dummy cycles	n bytes read out by Quad output until CS# goes high

I/O	1	4	1	1	1	1	1
Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	RDSFDP (Read SFDP)
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)	5A (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1		ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2		ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3		ADD3
5th byte							Dummy
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32KB block	to erase the selected block	to erase whole chip	Read SFDP mode

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status register)	PGM/ERS Suspend (Suspends Program/Erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	75 or B0 (hex)
2nd byte					Values	
3rd byte					Values	
4th byte						
5th byte						
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the configuration/ status register	program/erase operation is interrupted by suspend command

Command (byte)	PGM/ERS Resume (Resumes Program/Erase)	DP (Deep power down)	SBL (Set Burst Length)
1st byte	7A or 30 (hex)	B9 (hex)	C0 (hex)
2nd byte			Value
3rd byte			
4th byte			
5th byte			
Action	to continue performing the suspended program/erase sequence	enters deep power down mode	to set Burst length

ID/Reset Commands

Command (byte)	RDID (read identification)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)
1st byte	9F (hex)	AB (hex)	90 (hex)	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)
2nd byte		x	x				
3rd byte		x	x				
4th byte		x	ADD (Note 1)				
5th byte							
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	to enter the 8K-bit secured OTP mode	to exit the 8K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)

COMMAND (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			(Note 3)

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

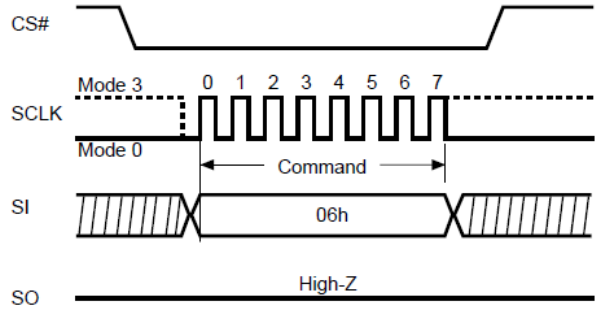
10.1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

The SIO[3:1] are "don't care" .

Figure 6. Write Enable (WREN) Sequence



10.2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

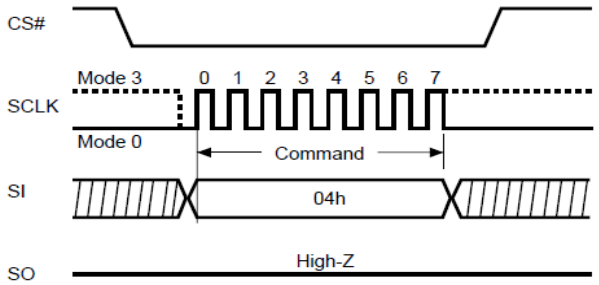
The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The WEL bit is reset by following situations:

- Power-up
- Completion of Write Disable (WRDI) instruction
- Completion of Write Status Register (WRSR) instruction
- Completion of Page Program (PP) instruction
- Completion of Quad Page Program (4PP) instruction
- Completion of Sector Erase (SE) instruction
- Completion of Block Erase 32KB (BE32K) instruction
- Completion of Block Erase (BE) instruction
- Completion of Chip Erase (CE) instruction
- Program/Erase Suspend
- Completion of Softreset command
- Completion of Write Security Register (WRSCUR) command

Figure 7. Write Disable (WRDI) Sequence



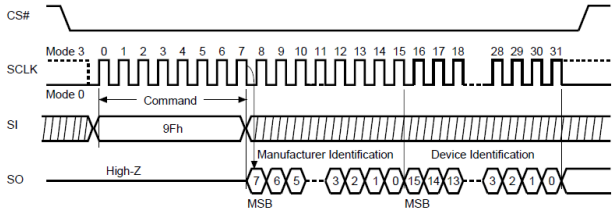
10.3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Manufacturer ID and Device ID are listed as "Table 6. ID Definitions".

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 8. Read Identification (RDID) Sequence



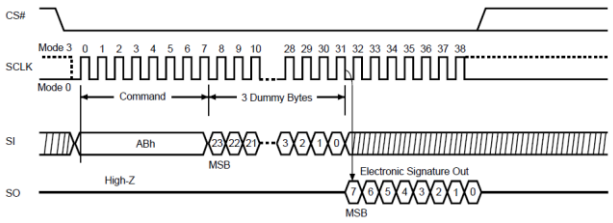
10.4. Read Electronic Signature (RES)

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as "Table 6. ID Definitions". This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

The SIO[3:1] are "don't care".

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low.

Figure 9. Read Electronic Signature (RES) Sequence



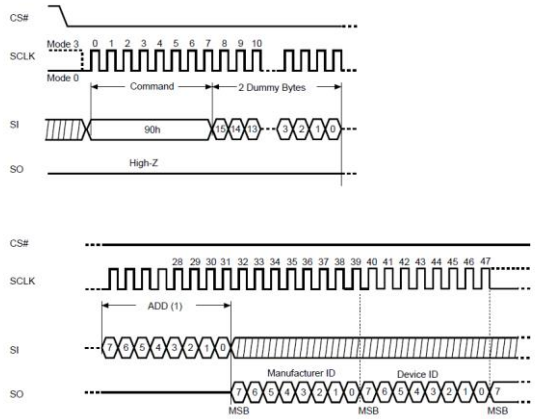
10.5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in "Table 6. ID Definitions".

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which, the manufacturer ID and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If

the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 10. Read Electronic Manufacturer & Device ID (REMS) Sequence



Note:

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

10.6. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Table 6. ID Definitions

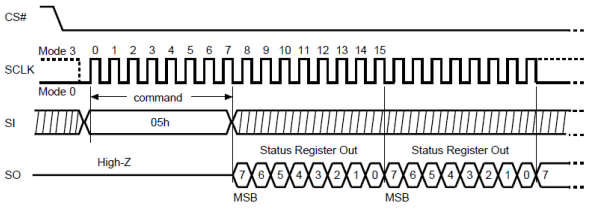
Command Type	GRP25L0805F		
RDID	Manufacturer ID	Memory type	Memory density
	C2	23	14
RES	Electronic ID		
	14		
REMS	Manufacturer ID	Device ID	
	C2	14	

10.7. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO. The SIO[3:1] are "don't care".

Figure 11. Read Status Register (RDSR) Sequence



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 12. Program/Erase flow with read array data

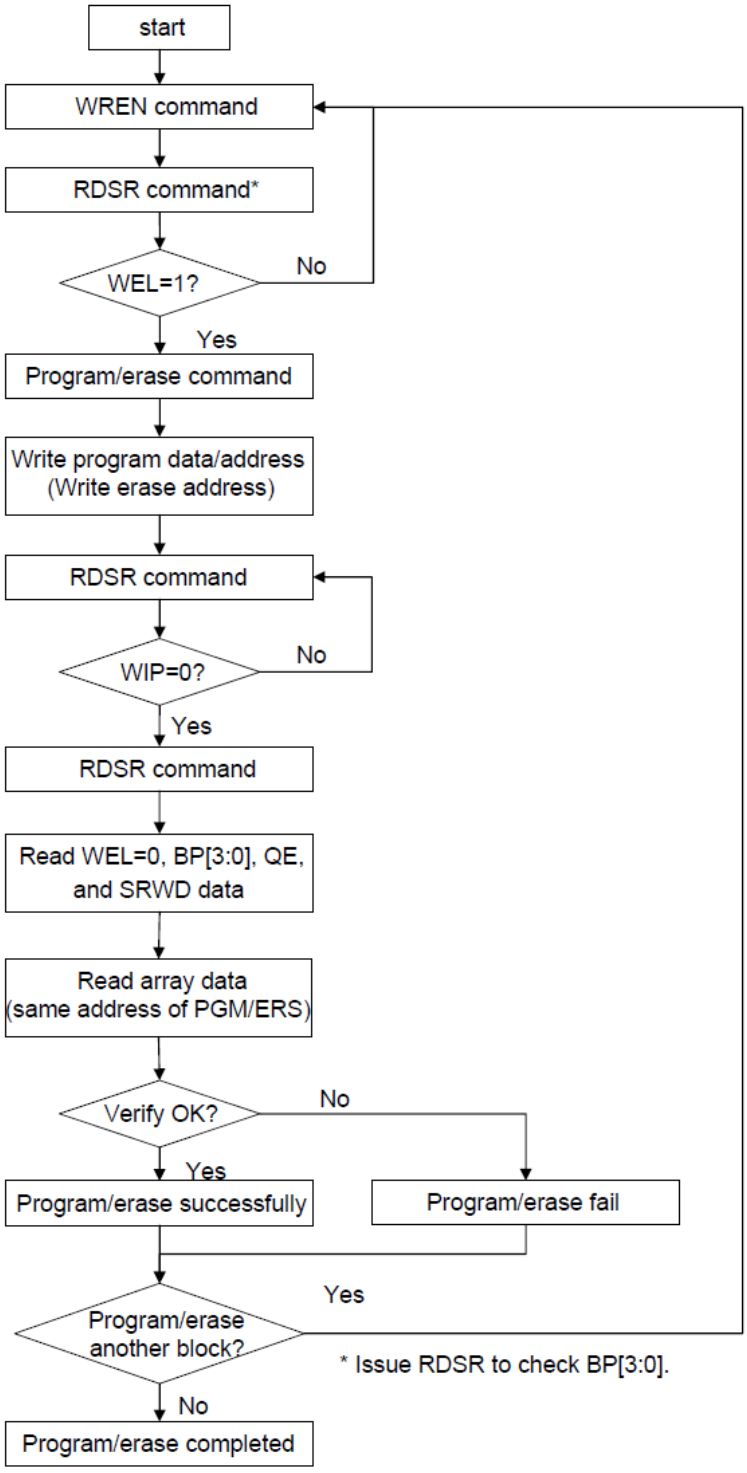
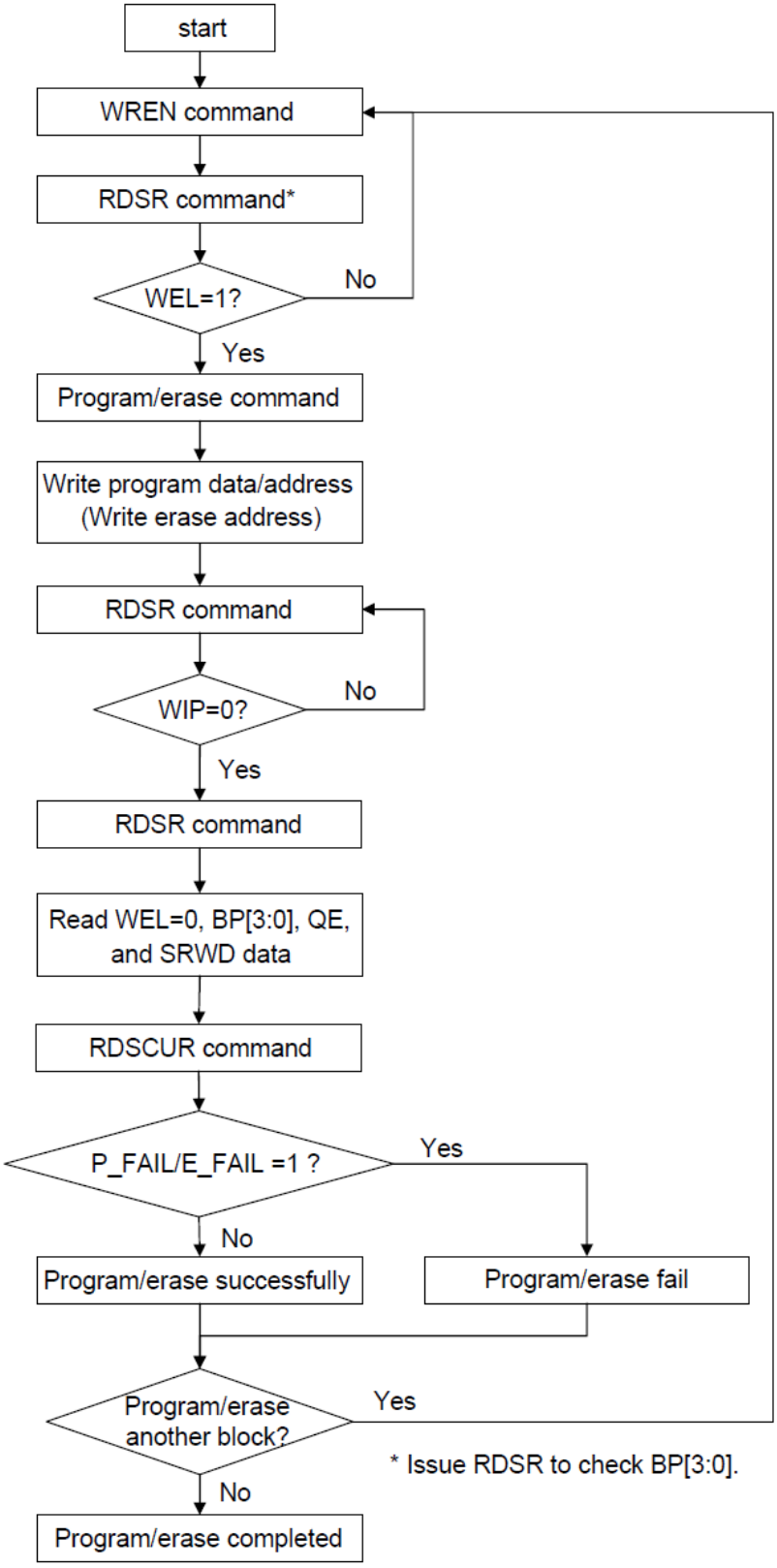


Figure 13. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to “1” by the WREN instruction. WEL needs to be set to “1” before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to “0” when a program or erase operation completes. To ensure that both WIP and WEL are “0” and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be “0” before checking that WEL is also “0”. If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to “0”.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in "Table 2. Protected Area Sizes") of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE/BE32K) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default, which is un-protected.

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In the other words, if the system goes into four I/O mode (QE=1), the feature of HPM and HOLD will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Table 7. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the "Table 2. Protected Area Sizes".

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

TB bit

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bit requires the Write Status Register (WRSR) instruction to be executed.

Table 8. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	Reserved
x	2READ/ 4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	x
x	Volatile bit	x	x	OTP	x	x	x

Table 9. Dummy Cycle Table

	DC	Numbers of Dummy Cycles
2READ	0 (default)	4
	1	8
4READ	0 (default)	6
	1	10

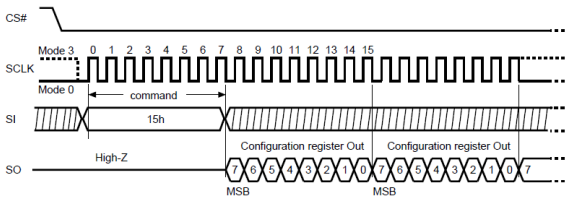
10.8. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

The SIO[3:1] are don't care.

Figure 14. Read Configuration Register (RDCR) Sequence



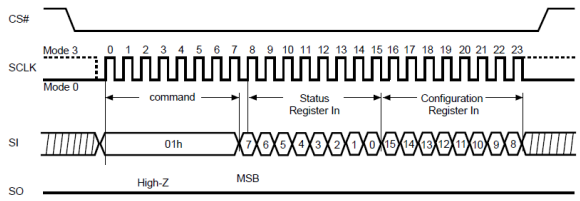
10.9. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in "Table 2. Protected Area Sizes"). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset. For more detail please check "Table 18. AC Characteristics".

Figure 15. Write Status Register (WRSR) Sequence



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Note: If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note: To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

Table 10.Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in "Table 2. Protected Area Sizes".

Figure 16. WRSR flow

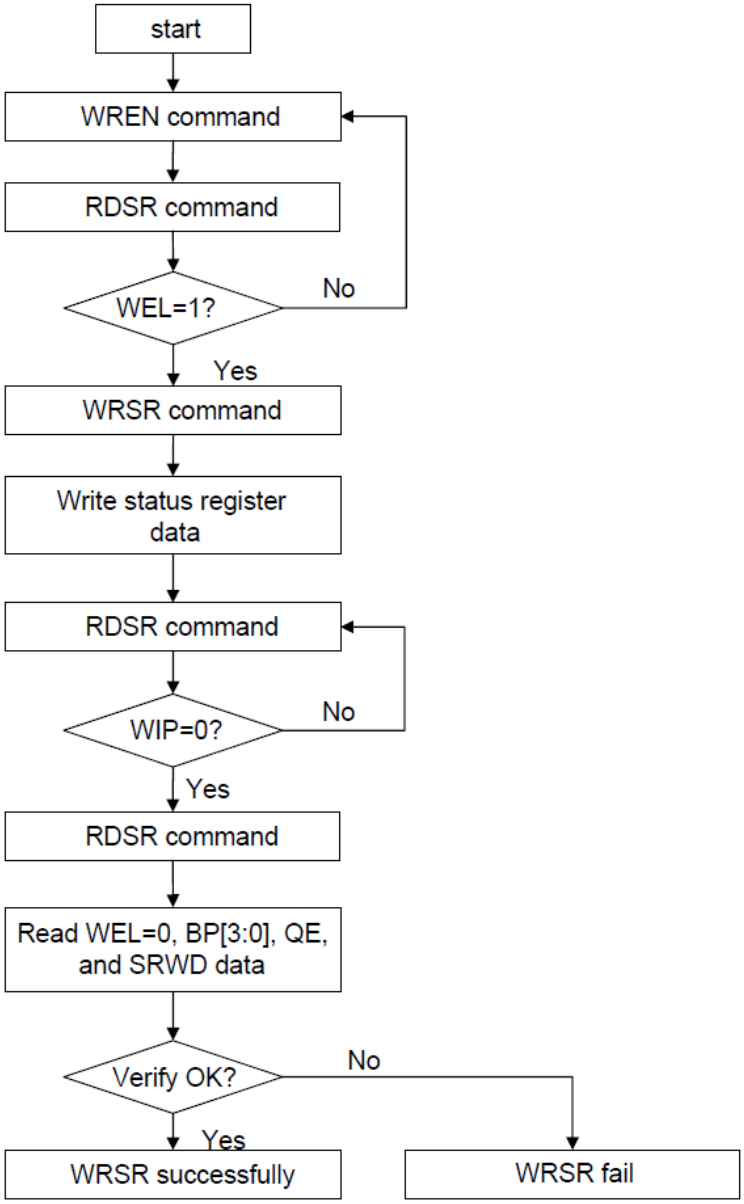
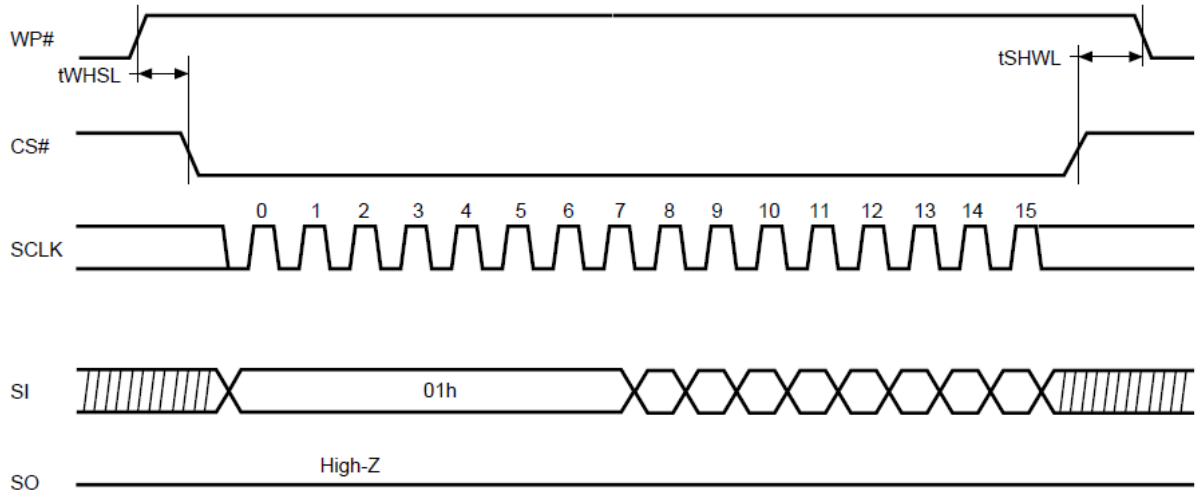


Figure 17. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



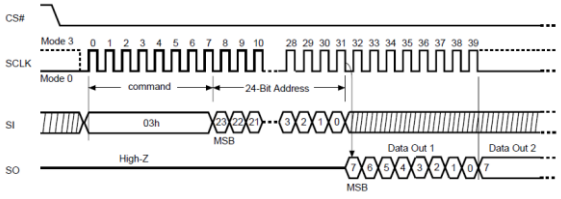
Note: WP# must be kept high until the embedded operation finish.

10.10. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 18. Read Data Bytes (READ) Sequence



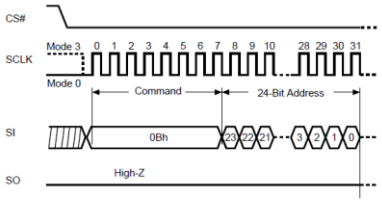
10.11. Read Data Bytes at Higher Speed (FAST_READ)

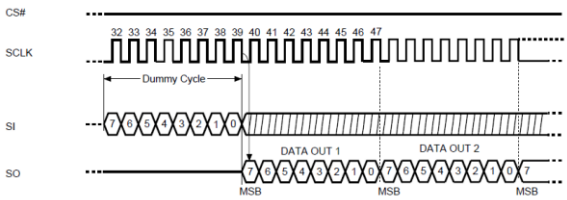
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 19. Read at Higher Speed (FAST_READ) Sequence





10.12. Dual Read Mode (DREAD)

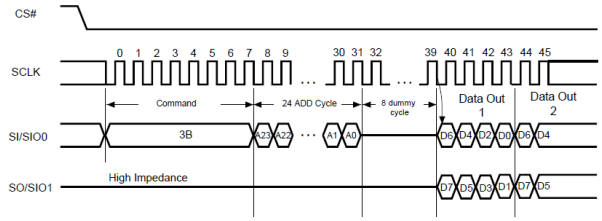
The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing

DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO1 & SIO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 20. Dual Read Mode Sequence (Command 3B)



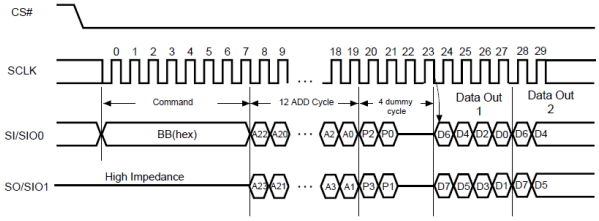
10.13. 2 x I/O Read Mode (2READ)

The 2READ instruction enables Double Transfer Rate of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 21. 2 x I/O Read Mode Sequence (Command BB)



Note: SI/SIO0 or SO/SIO1 should be kept "0h" or "Fh" in the first two dummy cycles. In other words, P2=P0 or P3=P1 is necessary.

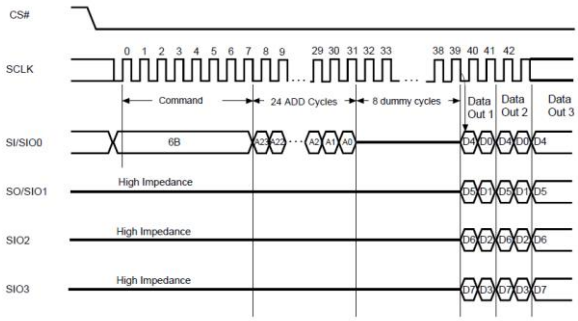
10.14. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the QREAD instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 22. Quad Read Mode Sequence (Command 6B)



10.15. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3,

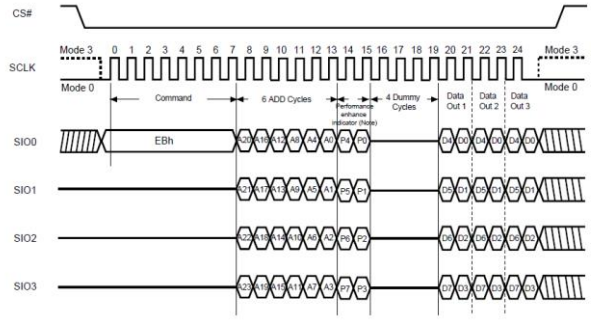
SIO2, SIO1 & SIO0→2+4 dummy cycles→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

Another sequence of issuing 4READ instruction especially useful in random access is: CS# goes low→sending 4READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) →24-bit random access address.

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 23. 4 x I/O Read Mode Sequence



Note:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

10.16. Burst Read

This device supports Burst Read.

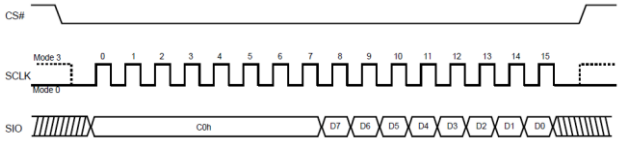
To set the Burst length, following command operation is required

Issuing command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with“1h”. Next 4 clocks is to define wrap around depth. Definition as following table:

Data	Wrap Around	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

The wrap around unit is defined within the 256Byte page, with random initial address. It’s defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0” command in which data=‘1xh”. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another “C0” command in which data=“0xh”. “EBh” supports wrap around feature after wrap around enable. The device id default without Burst read.

Figure 24. Burst Read



10.17. Performance Enhance Mode

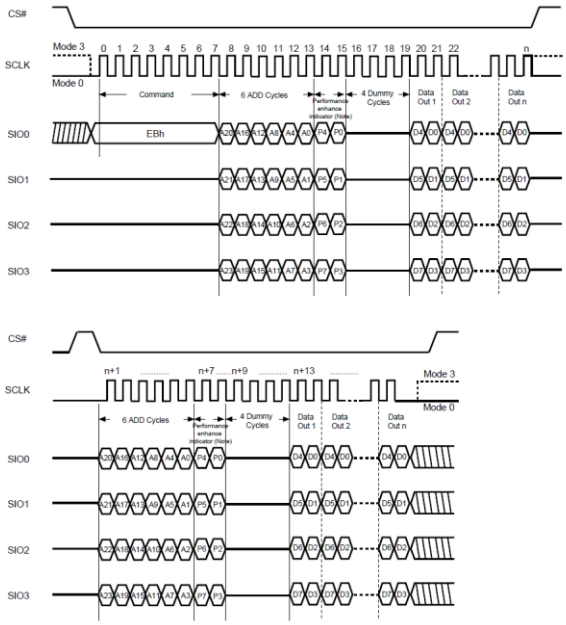
The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

“EBh” command supports enhance mode. The performance enhance mode is not supported in dual I/O mode.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue ”FFh” command to exit enhance mode.

Figure 25. 4 x I/O Read enhance performance Mode Sequence



Note:

1. Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
2. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF

10.18. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see "Table 4. Memory Organization") is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

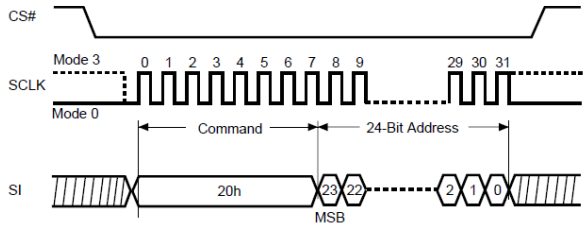
Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

Figure 26. Sector Erase (SE) Sequence



10.19. Block Erase (BE32K)

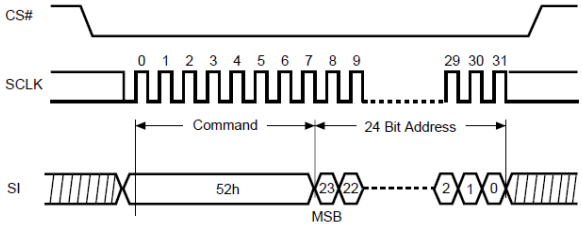
The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see "Table 4. Memory Organization") is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0, the array data will be protected (no change) and the WEL bit still be reset.

Figure 27. Block Erase 32KB (BE32K) Sequence (Command 52)



10.20. Block Erase (BE)

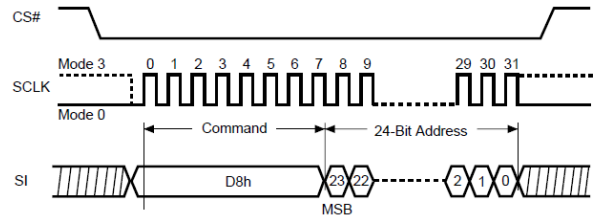
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to "Table 4. Memory Organization") is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

Figure 28. Block Erase (BE) Sequence



10.21. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte

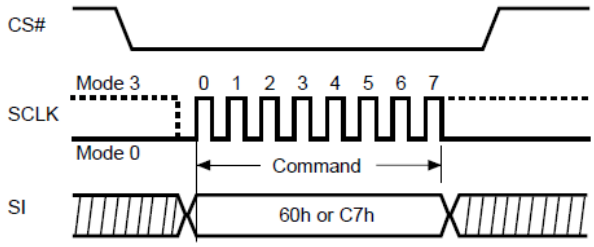
boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

The SIO[3:1] are "don't care".

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP3, BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP3, BP2, BP1, BP0 all set to "0".

Figure 29. Chip Erase (CE) Sequence



10.22. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

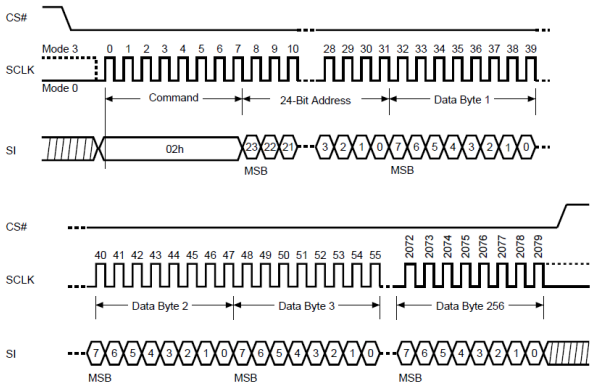
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

The SIO[3:1] are "don't care".

Figure 30. Page Program (PP) Sequence

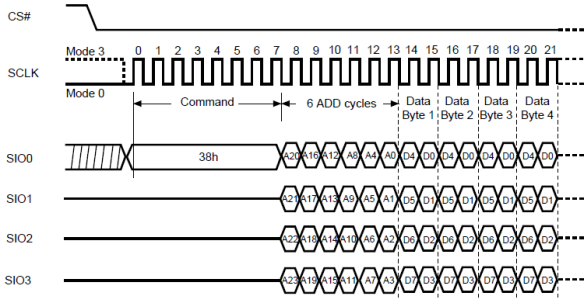


10.23. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The 4PP operation frequency supports as fast as f4PP. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

Figure 31. 4 x I/O Page Program (4PP) Sequence



10.24. Deep Power-down (DP)

The Deep Power-down (DP) instruction places the device into a minimum power consumption state, Deep Power down mode, in which the quiescent current is reduced from ISB1 to ISB2.

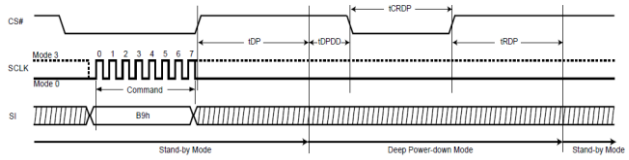
The sequence of issuing DP instruction: CS# goes low→ send DP instruction code→ CS# goes high. The CS# must

go high at the byte boundary; otherwise the instruction will not be executed. SIO[3:1] are "don't care".

After CS# goes high there is a delay of tDP before the device transitions from Stand-by mode to Deep Power-down mode and the current reduces from ISB1 to ISB2. Once in Deep Power-down mode, all instructions will be ignored.

CS# must not be pulsed low until the device has been in Deep Power-down mode for a minimum of tDPDD. The device exits Deep Power-down mode and returns to Stand-by mode if CS# pulses low for tCRDP or if the device is power-cycled or hardware reset. After CS# goes high, there is a delay of tRDP before the device transitions from Deep Power-down mode back to Stand-by mode.

Figure 32. Deep Power-down (DP) Sequence and Release from Deep Power-down Sequence



10.25. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. While the device is in 8K-bit Secured OTP mode, array access is not available. The additional 8K-bit secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

The SIO[3:1] are "don't care".

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

10.26. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 8K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

The SIO[3:1] are "don't care".

10.27. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

The SIO[3:1] are "don't care".

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 1st 4K-bit Secured OTP area cannot be updated any more.

Program Suspend Status bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Erase Suspend Status bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Fail Flag bit. The Program Fail bit shows the status of the last Program operation. The bit will be set to "1" if the program operation failed or the program region was protected. It will be automatically cleared to "0" if the next program operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Fail Flag bit. The Erase Fail bit shows the status of last Erase operation. The bit will be set to "1" if the erase operation failed or the erase region was protected. It will be automatically cleared to "0" if the next erase operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Table 11. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend status)	PSB (Program Suspend status)	LDSO (lock-down 1st 4K-bit Secured OTP)	Secured OTP Indicator bit (2nd 4K-bit Secured OTP)
Reserved	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	Reserved	0=Erase is not suspended 1=Erase is suspended (default=0)	0=Program is not suspended 1=Program is suspended (default=0)	0 = not lockdown 1 = lock-down (cannot program/ erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
Reserved	Read Only	Read Only		Read Only	Read Only	OTP	Read Only

10.28. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 1st 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the 1st 4K-bit Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is: CS# goes low→ sending WRSCUR instruction → CS# goes high.

The SIO[3:1] are "don't care".

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

10.29. Program/Erase Suspend/Resume

The Suspend instruction interrupts a Page Program, Sector Erase, or Block Erase operation to allow access to the memory array. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the sector or block being erased ("Table 12. Readable Area of Memory While a Program or Erase Operation is Suspended").

Table 12. Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended Operation	Readable Region of Memory Array
Page Program	All but the Page being programmed
Sector Erase (4KB)	All but the 4KB Sector being erased
Block Erase (32KB)	All but the 32KB Block being erased
Block Erase (64KB)	All but the 64KB Block being erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL ("Figure 34. Suspend to Read/Program Latency") before the Write Enable Latch (WEL) bit clears to “0” and the PSB or ESB sets to “1”, after which the device is ready to accept one of the commands listed in "Table 13. Acceptable Commands During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to "Table 18. AC Characteristics" for tPSL and tESL timings. "Table 14. Acceptable Commands During Suspend (tPSL/tESL not required)" lists the commands for which the tPSL and tESL latencies do not apply. For example, RDSR, RDSCUR, RSTEN, and RST can be issued at any time after the Suspend instruction.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

Table 13. Acceptable Commands During Program/Erase Suspend after tPSL/tESL

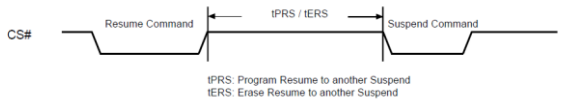
Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
READ	03h	•	•
FAST READ	0Bh	•	•
DREAD	3Bh	•	•
QREAD	6Bh	•	•
2READ	BBh	•	•

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
4READ	EBh	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
REMS	90h	•	•
SBL	C0h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h		•
RESUME	7Ah or 30h	•	•
PP	02h		•
4PP	38h		•

Table 14. Acceptable Commands During Suspend (tPSL/tESL not required)

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

Figure 33. Resume to Suspend Latency

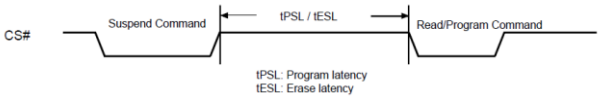


10.29.1. Erase Suspend to Program

The “Erase Suspend to Program” feature allows Page Programming while an erase operation is suspended. Page Programming is permitted in any unprotected memory except within the sector of a suspended Sector Erase operation or within the block of a suspended Block Erase operation. The Write Enable (WREN) instruction must be issued before any Page Program instruction.

A Page Program operation initiated within a suspended erase cannot itself be suspended and must be allowed to finish before the suspended erase can be resumed. The Status Register can be polled to determine the status of the Page Program operation. The WEL and WIP bits of the Status Register will remain “1” while the Page Program operation is in progress and will both clear to “0” when the Page Program operation completes.

Figure 34. Suspend to Read/Program Latency



Notes:

1. Please note that Program only available after the Erase-Suspend operation
2. To check suspend ready information, please read security register bit2(PSB) and bit3(ESB)

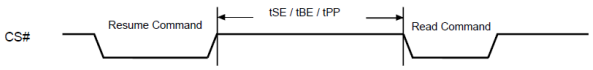
10.30. Program Resume and Erase Resume

The Resume instruction resumes a suspended Page Program, Sector Erase, or Block Erase operation. Before issuing the Resume instruction to restart a suspended erase operation, make sure that there is no Page Program operation in progress.

Immediately after the Serial NOR Flash receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”. The program or erase operation will continue until finished ("Figure 35. Resume to Read Latency") or until another Suspend instruction is received. A resume-to-suspend latency of tPRS or tERS must be observed before issuing another Suspend instruction ("Figure 33. Resume to Suspend Latency").

Please note that the Resume instruction will be ignored if the Serial NOR Flash is in “Performance Enhance Mode”. Make sure the Serial NOR Flash is not in “Performance Enhance Mode” before issuing the Resume instruction.

Figure 35. Resume to Read Latency



10.31. No Operation (NOP)

The "No Operation" command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

The SIO[3:1] are don't care.

10.32. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN)

command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are "don't care".

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 36. Software Reset Recovery

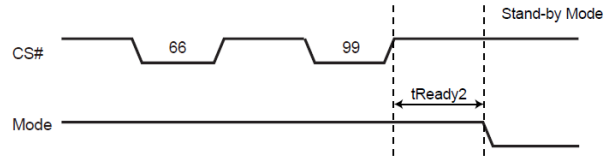
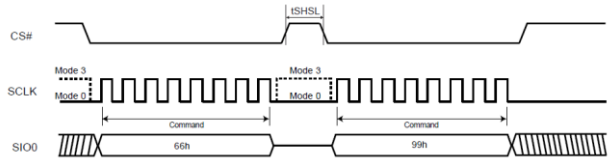


Figure 37. Reset Sequence



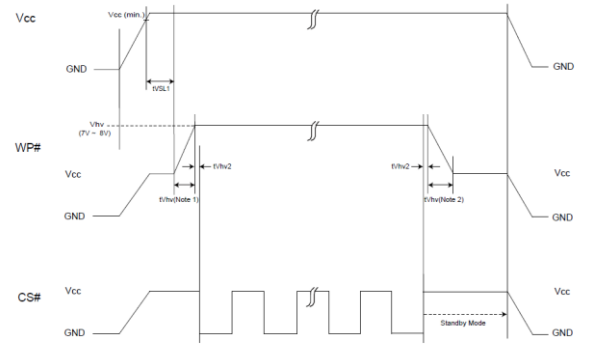
10.33. High Voltage Operation

The flash device supports High Voltage Operation. This opeartion allows user can have better performance in following Program/Erase operation.

To enable High Voltage Opeartion, WP#/SIO2 need to apply Vhv during whole operation. If the voltage can not sustain in Vhv range, the Program/Erase opeation might be failed. CS# can only go low after tVSL1+tVhv +tVhv2 timing during High Voltage Operation. WP# can only start to go low after whole Erase/Program Operation has been done.

To check the operation status, user may check the status of WIP bit.

Figure 38. High Voltage Operation Diagram



Note 1: Please note that the CS# can only go low after tVSL1+tVhv +tVhv2 timing during High Voltage Operation.

Note 2: Please note that the WP# can only start to go low after whole Erase/Program Operation has been done.

To check the operation status, user may check the status of WIP bit.

Note 3: tVhv(min.) = 250ns, tVSL 1(min.) = 800us; tVhv2(min.) = 0ns

Note 4: Vhv range is 7V(min.) ≤ Vhv ≤ 8(max.)

Note 5: The High Voltage Operation can only work during Vcc(min.) ≤ Vcc ≤ 2.0V

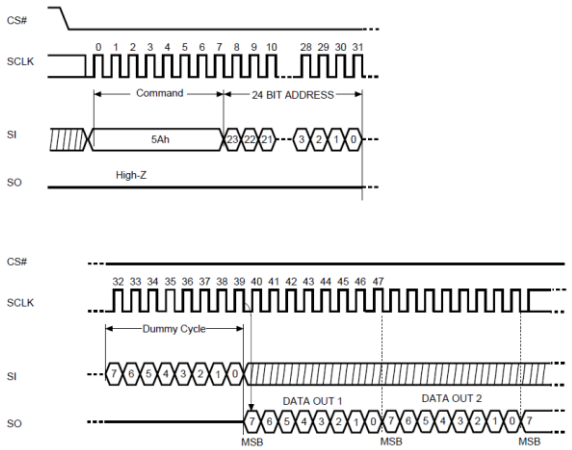
10.34. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is same as FAST_READ: CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216B.

Figure 39. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



11. POWER-ON STATE

The device is at the following states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the "Figure 46. Power-up Timing".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during this stage if a write, program, erase cycle is in progress.

12. ELECTRICAL SPECIFICATIONS

12.1. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 40. Maximum Negative Overshoot Waveform

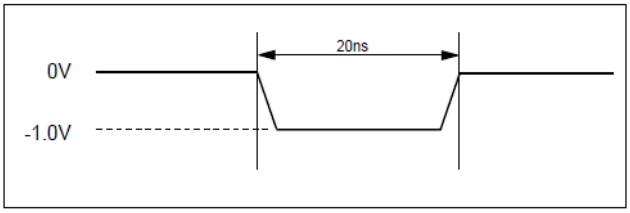
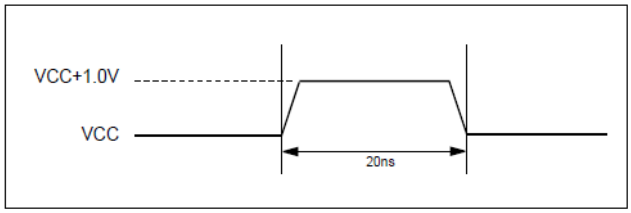


Figure 41. Maximum Positive Overshoot Waveform

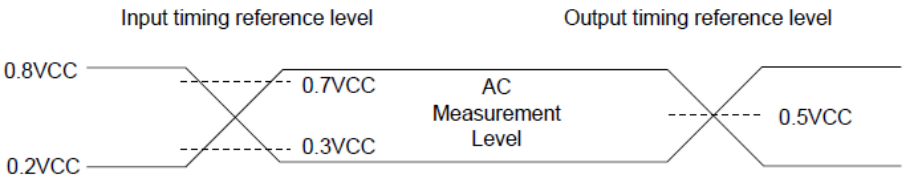


12.2. Capacitance

TA = 25°C, f = 1.0 MHz

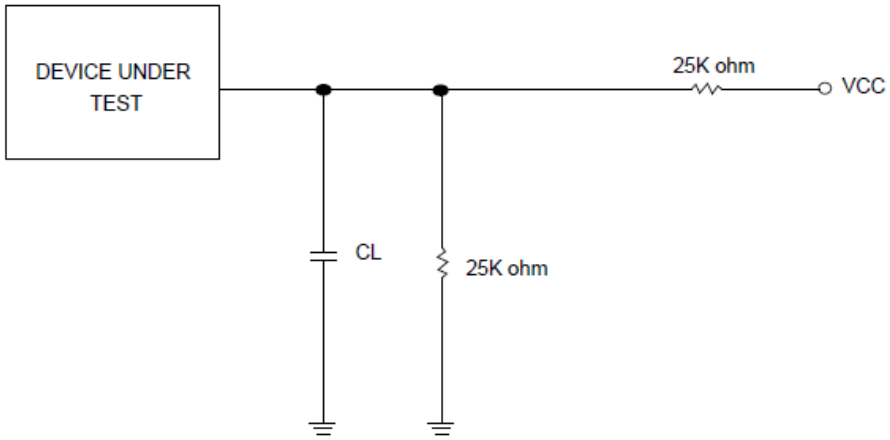
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance	-	-	6	pF	VIN = 0V
COUT	Output Capacitance	-	-	8	pF	VOUT = 0V

Figure 42. Input Test Waveforms and Measurement Level



Note: Input pulse rise and fall time are <5ns

Figure 43. Output Loading



CL=15/30pF Including jig capacitance

12.3. DC Characteristics

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
Iwph	Leakage Current while WP# at Vhv				30	uA	VCC < 2.1V
ISB1	VCC Standby Current	1		9	40	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			0.1	0.5	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		4.2	6.7	mA	f=108MHz SCLK=0.1VCC/0.9VCC, SO=Open
				5	8	mA	f=104MHz (2x I/O) SCLK=0.1VCC/0.9VCC, SO=Open
				3.9	6.5	mA	f=33MHz (4x I/O) SCLK=0.1VCC/0.9VCC, SO=Open
				6.5	9.5	mA	f=104MHz (4x I/O) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		5.8	10	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			3.5	10	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (64K) Erase Current (SE/BE)	1		3.5	10	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		4	10	mA	Erase in Progress, CS#=VCC
Vhv	High Voltage Applied at WP# pin		7		8	V	Test Condition, VCC=2.0V
VIL	Input Low Voltage		-0.5		0.2VCC	V	
VIH	Input High Voltage		0.8VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes:

1. Device operation range: 2.3V-3.6V, Typical values at VCC = 3.0V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

12.4. AC Characteristics

Symbol	Alt.	Parameter		Min.	Typ.(2)	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE32K, BE, CE, DP, RES, WREN, WRDI, RDID, RDSR, WRSR		D.C.		108	MHz
fRSCLK	fR	Clock Frequency for READ instructions				50	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions				104	MHz
	fQ	Clock Frequency for 4READ/QREAD instructions				104	MHz
f4PP		Clock Frequency for 4PP (Quad page program)				104	MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK)	45% x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK)	45% x (1/fSCLK)			ns
			Normal Read (fRSCLK)	13			ns
tCLCH(8)		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL(8)		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read	15			ns
			From Write/Erase/Program to Read Status Register	30			ns
tSHQZ(8)	tDIS	Output Disable Time				8	ns
tCLQV	tV	Clock Low to Output Valid	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		HOLD# Active Setup Time (relative to SCLK)		8			ns
tCHHH		HOLD# Active Hold Time (relative to SCLK)		8			ns
tHHCH		HOLD# Not Active Setup Time (relative to SCLK)		8			ns
tCHHL		HOLD# Not Active Hold Time (relative to SCLK)		8			ns
tHHQX	tLZ	HOLD# to Output Low-Z				10	ns
tHLQZ	tHZ	HOLD# to Output High-Z				10	ns
tWHSL(3)		Write Protect Setup Time		10			ns
tSHWL(3)		Write Protect Hold Time		10			ns
tDP		CS# High to Deep Power-down Mode				10	us
tDPDD		Delay Time for Release from Deep Power-Down Mode once entering Deep Power-Down Mode		30			us
tCRDP		CS# Toggling Time before Release from Deep Power- Down Mode		20			ns
tRDP		Recovery Time for Release from deep power down mode		35			us
tW		Write Status Register Cycle Time				30	ms

Symbol	Alt.	Parameter	Min.	Typ.(2)	Max.	Unit
tREADY2		Reset Recovery time (During instruction decoding)	40			us
		Reset Recovery time (for read operation)	35			us
		Reset Recovery time (for program operation)	310			us
		Reset Recovery time(for SE4KB operation)	12			ms
		Reset Recovery time (for BE32K/64K operation)	25			ms
		Reset Recovery time (for Chip Erase operation)	100			ms
		Reset Recovery time (for WRSR operation)	40			ms
tESL(7)		Erase Suspend Latency			40	us
tPSL(7)		Program Suspend Latency			40	us
tPRS (4)		Latency between Program Resume and next Suspend	0.3			us
tERS (5)		Latency between Erase Resume and next Suspend	0.3			us
tBP		Byte-Program		30	100	us
		Byte-Program (Applied Vhv at WP# pin)		30	100	us
tPP		Page Program Cycle Time		0.8	4	ms
		Page Program Cycle Time (Applied Vhv at WP# pin)		0.56	3.6	ms
tSE		Sector Erase Cycle Time		38	240	ms
		Sector Erase Cycle Time (Applied Vhv at WP# pin)		34	210	ms
tBE32K		Block Erase (32KB) Cycle Time		0.225	1.5	s
		Block Erase (32KB) Cycle Time (Applied Vhv at WP# pin)		0.2	1.05	s
tBE		Block Erase (64KB) Cycle Time		0.45	3	s
		Block Erase (64KB) Cycle Time (Applied Vhv at WP# pin)		0.4	2.1	s
tCE		Chip Erase Cycle Time		5.6	18	s
		Chip Erase Cycle Time (Applied Vhv at WP# pin)		5	16	s

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Program operation may be interrupted as often as system request. The minimum timing of tPRS must be observed before issuing the next program suspend command. However, in order for an Program operation to make progress, tPRS ≥ 100us must be included in resume-to-suspend loop(s). Not 100% tested.
5. Erase operation may be interrupted as often as system request. The minimum timing of tERS must be observed before issuing the next erase suspend command. However, in order for an Erase operation to make progress, tERS ≥ 200us must be included in resume-to-suspend loop(s). The details are described in application notes. Not 100% tested.
6. Test condition is shown as "Figure 42. Input Test Waveforms and Measurement Level", "Figure 43. Output Loading".
7. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
8. The value guaranteed by characterization, not 100% tested in production.

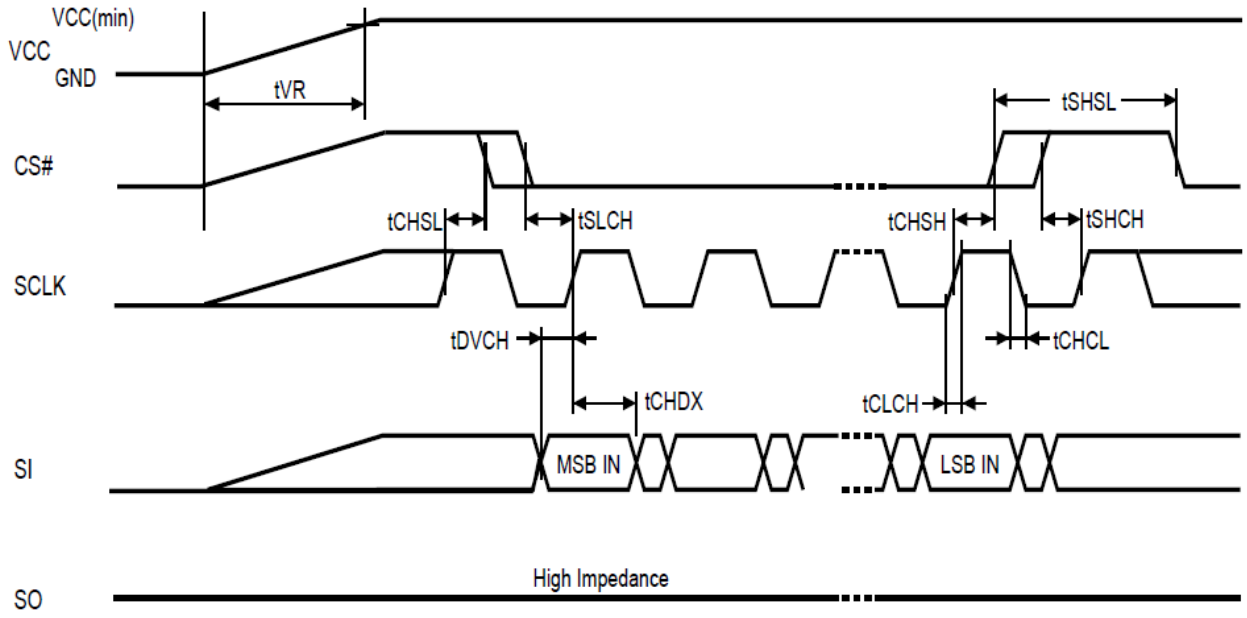
13. TIMING ANALYSIS

At Device Power-Up and Power-Down

AC timing illustrated in "Figure 44. AC Timing at Device Power-Up" and "Figure 45. Power-Down Sequence" are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 44. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "12.4 . AC Characteristics".

Figure 45. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

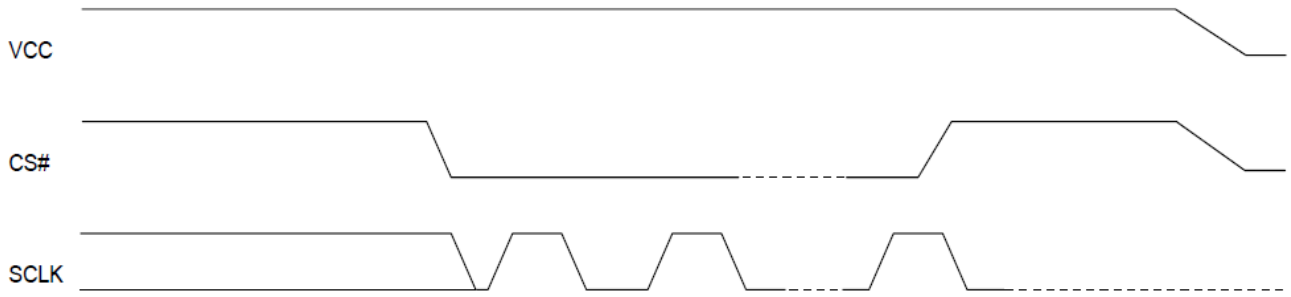


Figure 46. Power-up Timing

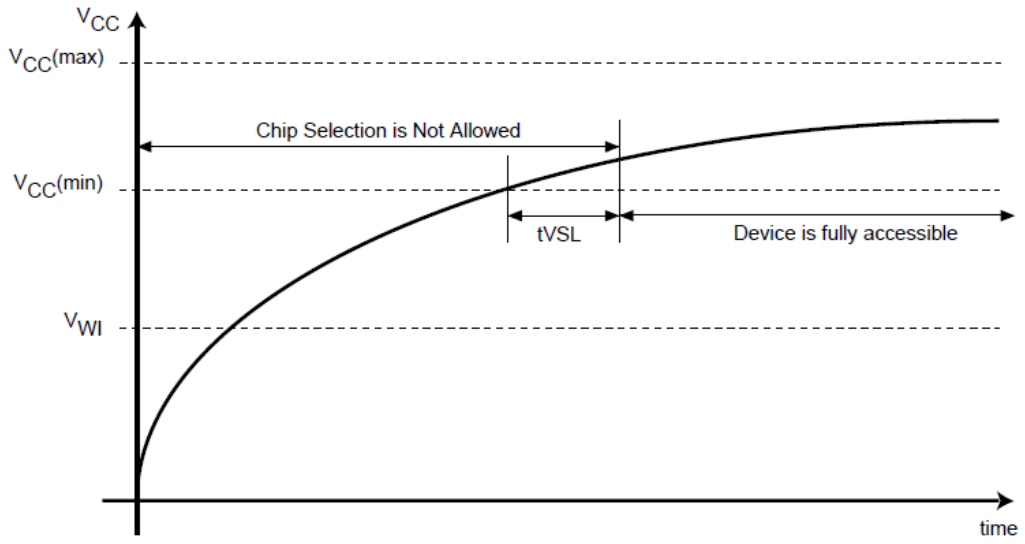


Figure 47. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

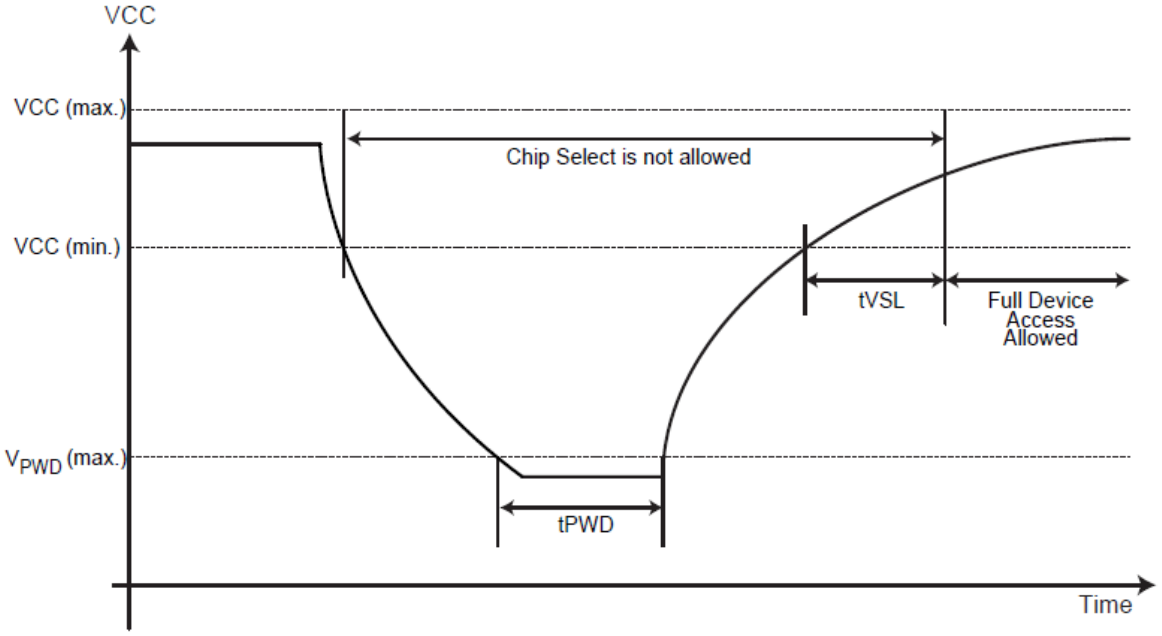


Table 19. Power-Up/Down Voltage and Timing

Symbol	Parameter		Min.	Max.	Unit
tVSL	VCC(min.) to device operation		800	-	us
VWI	Write Inhibit Voltage		1.1	2.1	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur	Deep Power Mode	-	0.4	V
		others	-	0.9	V
tPWD	The minimum duration for ensuring initialization will occur		300	-	us
tVR	VCC Rise Time		20	500000	us/V

Note: These parameters are characterized only.

13.1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

14. ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	Min.	Typ.(1)	Max.(2)	Unit
Write Status Register Cycle Time			30	ms
Sector Erase Cycle Time (4KB)		38	240	ms
Sector Erase Cycle Time (4KB) (Applied Vhv at WP# pin)		34	210	ms
Block Erase Cycle Time (32KB)		0.225	1.5	s
Block Erase Cycle Time (32KB) (Applied Vhv at WP# pin)		0.2	1.05	s
Block Erase Cycle Time (64KB)		0.45	3	s
Block Erase Cycle Time (64KB) (Applied Vhv at WP# pin)		0.4	2.1	s
Chip Erase Cycle Time		5.6	18	s
Chip Erase Cycle Time (Applied Vhv at WP# pin)		5	16	s
Byte Program Time		30(4)	100	us
Byte Program Time (Applied Vhv at WP# pin)		30	100	us
Page Program Time		0.8(4)	4	ms
Page Program Time (Applied Vhv at WP# pin)		0.56	3.6	ms
Erase/Program Cycle	100,000			cycles

Notes:

1. Typical erase assumes the following conditions: 25°C, typical operation voltage and all zero pattern.
2. Under worst conditions of 85°C and minimum operation voltage.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Typical program assumes the following conditions: 25°C, typical VCC, and checkerboard pattern.

15. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = typical operation voltage, one pin at a time.		

16. PACKAGE/PAD LOCATIONS

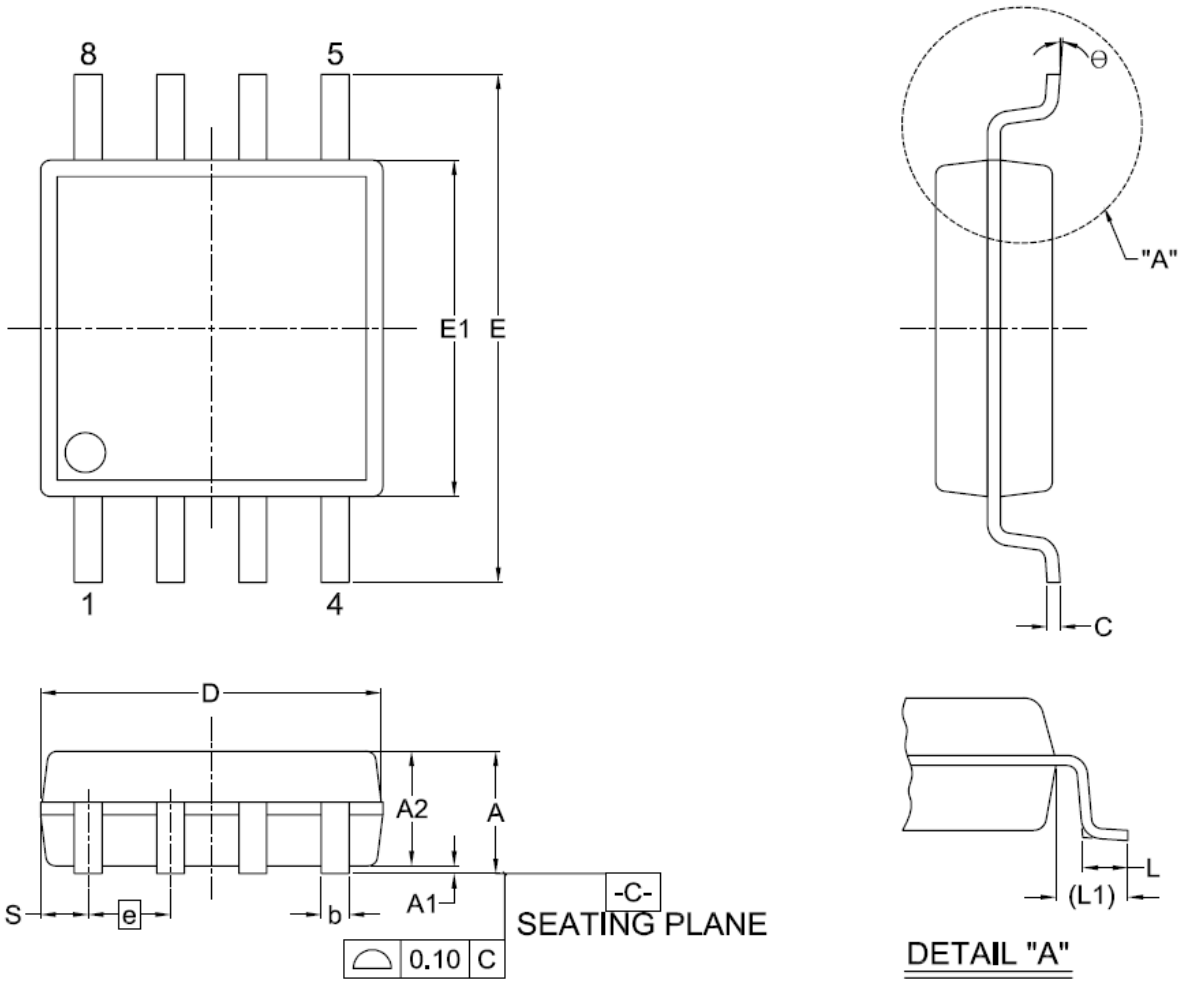
16.1. Ordering Information

Product Number	Package Type
GPR25V0805F-QS13x	SOP 8L 200mil-Halogen Free Package

Note: x = 1 - 9, serial number.

16.2. Package Information

16.2.1. Package Outline for SOP 8L (200MIL)



16.2.1.1. Dimensions (Inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	—	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	—	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	—	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	—	0.031	0.056	0.035	8°

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	5				

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18. REVISION HISTORY

Date	Revision	Description	Page
May 25, 2016	1.0	Original	45