CML Semiconductor Products

PRODUCT INFORMATION

FX812 Voice Store and Retrieve Codec

Publication D/812/3 July 1994
Provisional Issue

Features/Applications

- **Half-Duplex Voice Storage and Replay**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answerphone and Voice-Notepad**
- **Selectable Sample Rates and "Memory Size"**
- **Small Outline (S.O.I.C.) SMD and DIL Packages**
- **Low-Power 5-Volt CMOS**

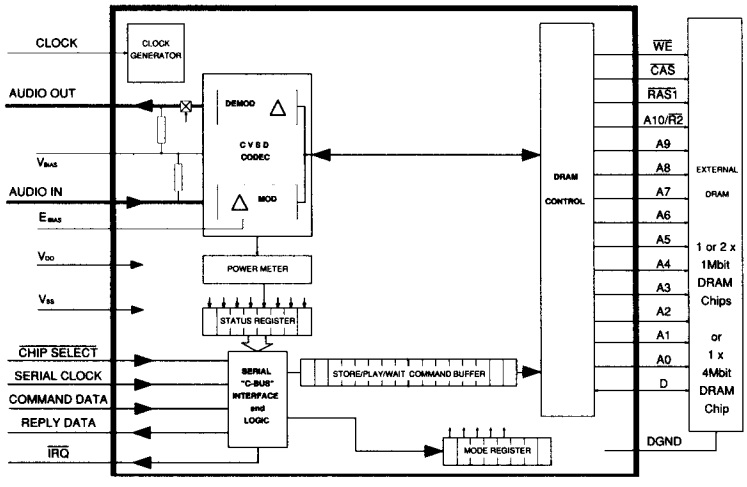


Fig.1 FX812 Voice Store and Retrieve Codec

FX812

Brief Description

The FX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the FX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with "Answerphone," "Message-Notepad" and general announcement facilities.

The FX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio's own µProcessor/Controller.

Input audio from the "Store" output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the "Play" input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The FX812 has no on-chip input or output audio filtering, this facility must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic small outline SMD and 28-pin cerdip DIL packages.

Pin Number Function

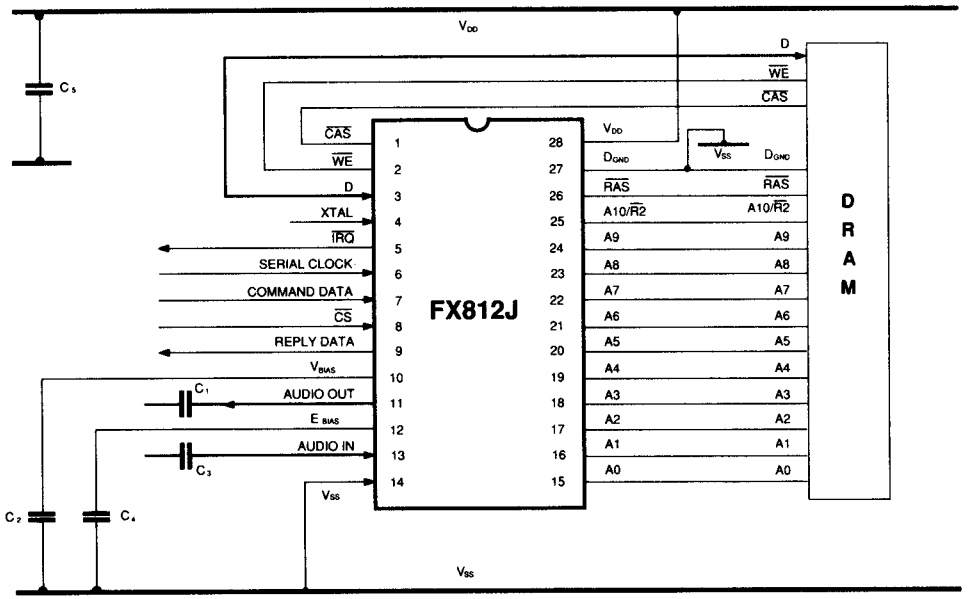
FX812DW FX812J	
1	**$\overline{CAS}$:** This output should be connected to the "Column Address Strobe" input pin(s) of all DRAM devices fitted.
2	**$\overline{WE}$:** This output should be connected to the "Write Enable" input pin(s) of all DRAM devices fitted.
3	**D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the "Data In" and "Data Out" pins ("D" and "Q") of DRAM devices.
4	**Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum "C-BUS" timings (Figures 6 and 7) would have to be increased pro-rata.
5	**Interrupt Request ($\overline{IRQ}$):** This Interrupt Request output from the FX812 is 'wire-OR able' allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the CML Serial µProcessor Data Interface publication D/µINT/1 June 1991). This output has a low-impedance pulldown to V_{SS} when active, and a high-impedance when inactive.
6	**Serial Clock:** The "C-BUS" serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams.
7	**Command Data:** The "C-BUS" serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock.
8	**Chip Select ($\overline{CS}$):** The "C-BUS" data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
9	**Reply Data:** The "C-BUS" serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController.
10	**V_{BIAS}:** The output of the internal analogue circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2 (see Figure 2).
11	**Audio Out:** The analogue output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands (62_H) active, the VSR Codec will play-out an idle pattern of "101010.....10^s". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at V_{BIAS} via an internal 500kΩ resistor. The output at this pin is unfiltered; An external speechband filter – such as that included on the FX816/826/836 Audio Processors – will be required. As this output is centred about $V_{DD}/2$ a coupling capacitor is required.
12	**E_{BIAS}:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to V_{SS} by a capacitor C_4, (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; It can take more than one second for the E_{BIAS} voltage to stabilize when power is first applied to this device. A faster start--up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the E_{BIAS} pin to be connected to V_{BIAS} through a resistance of approximately 100kΩ.
13	**Audio In:** The analogue input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at V_{BIAS} via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the FX816/826/836 Audio Processors.
14	**V_{SS}:** The "analogue" ground connection. See D_{GND} description.

Pin Number Function

FX812DW FX812J	
15	**A0:** DRAM address line outputs from the FX812. These pins should be connected to the corresponding address inputs of the associated DRAM.
16	**A1:**
17	**A2:**
18	**A3:**
19	**A4:**
20	**A5:**
21	**A6:**
22	**A7:**
23	**A8:**
24	**A9:**
25	**A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below:
26	**$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections.
27	**D_{GND}:** The digital signal ground connection to the VSR Codec. Both D_{GND} and V_{SS} pins should be connected to the negative side of the d.c. power supply, however the printed circuit board should be laid out so that D_{GND} is connected as closely as possible to the DRAM section ground pins.
28	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to V_{SS} via capacitor C_5, located close to the FX812 pins.

MS bit	DRAMs	Connected To	This Output
"0"	1Mbits'	DRAM No 2 $\overline{RAS}$	RAS2
"1"	4Mbit	DRAM A10	A10 Signal

Application Information



Component	Value
C_1	Dependant upon the input impedance of the driven stage
C_2	1.0µF
C_3	100nF
C_4	1.0µF non-electrolytic
	Tolerance: Capacitors = -50/+100%

Fig.2 Recommended External Components

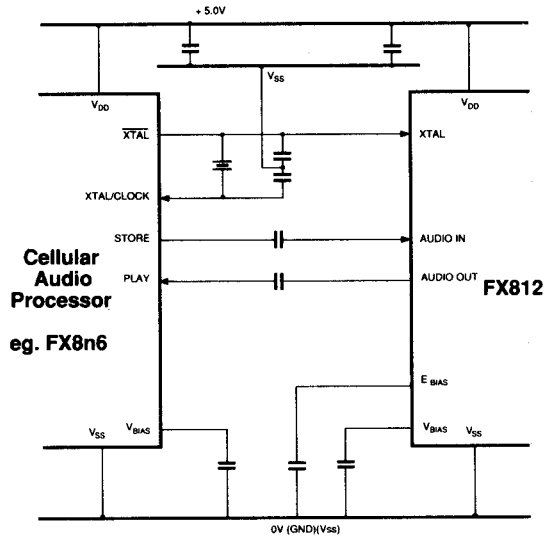


Fig.3 Interfacing to an Audio Processor

Application Information .....

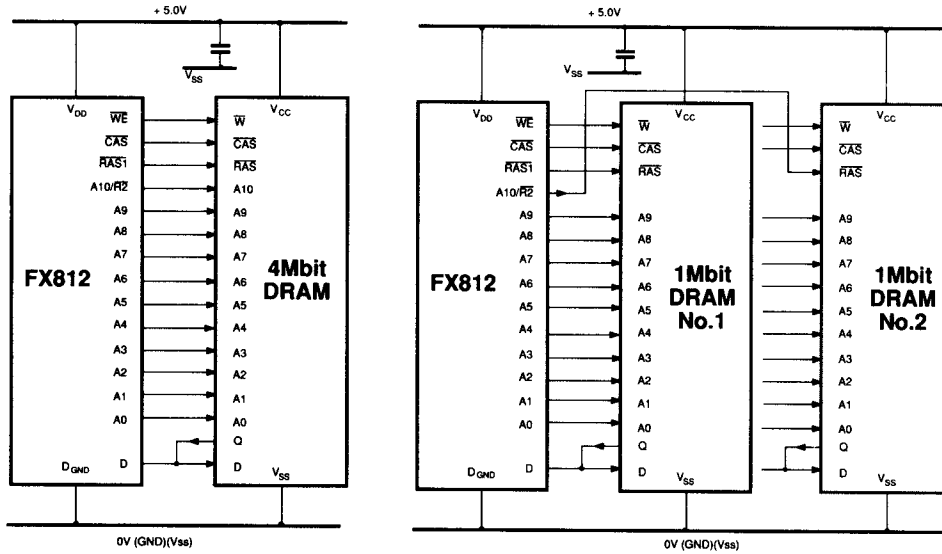


Fig.4 Example DRAM Connections

Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

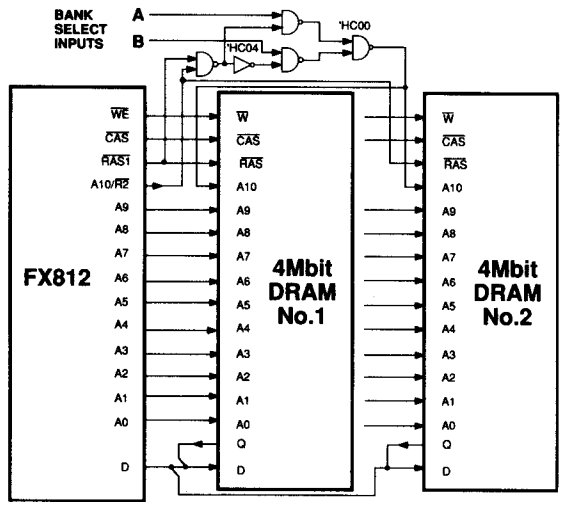


Fig.5 Employment of External Elements to Drive Two 4-MBit DRAM Chips

Driving Two 4-MBit DRAM Sections

By the addition of external logic circuitry, the FX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kb/s.

With reference to the circuitry shown in Figure 5:

With the Mode Register **MS** Bit set to "0" the FX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

Bank Select Inputs		DRAM No 1 Pages 0 – 1023	DRAM No 2 Pages 1024 – 2047
A	B		
0	0	■	■
1	0	■	■
0	1	■	■
1	1	■	■

The Controlling System

"C-BUS" Hardware Interface

"C-BUS" is CML's proprietary standard for the transmission of commands and data between a µController and CML's New Generation microcircuits.

"C-BUS" has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the FX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the FX812.
The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary (MSB … LSB)	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Mode Register	60	0 1 1 0 0 0 0 0	+	1 byte Instruction to Mode Register
Read Status Register	61	0 1 1 0 0 0 0 1	+	1 byte Reply from Status Register
Store/Play Page	62	0 1 1 0 0 0 1 0	+	2 bytes Command
Wait	63	0 1 1 0 0 0 1 1		

Table 1 – "C-Bus" Address/Commands

"Write to Mode Register" – A/C 60_H, followed by 1 byte of Command Data.

Interrupt Output – IE
Controls the FX812 IRQ output driver.

Sampling Rates – SR
The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

Memory Size – MS
The FX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

Powersave – PS
Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

Decode/Encode – DE
The Codec and DRAM operational mode."
"Play" or "Store"

Setting	*Mode Bits*
MSB	***Transmitted to 812 First***
7	**Interrupt Output**
1	Enable
0	Disable
6	**Sampling Rate**
1	63kb/s
0	32kb/s
5	**Memory (DRAM) Size**
1	Single 4Mbit
0	1 or 2 x 1Mbit
4	**Powersave**
1	CVSD Codec Powersaved
0	CVSD Codec Powered
3	**Decode/Encode**
1	Decode – Play Mode
0	Encode – Store Mode
2 1 0	**Not Used**
0 0 0	Set to 'zeros'

Table 2 Control Register

Interrupts

The FX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

IF Bit	IE Bit	$\overline{IRQ}$
"0" cleared	"0" disable	High Z
"0" cleared	"1" enable	High Z
"1" Interrupt	"0" disable	High Z
"1" Interrupt	"1" enable	V_{SS} (logic "0")

"General Reset" – A/C 01_H

Upon Power-Up the "bits" in the FX812 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the "C-BUS," and has the following effect upon the FX812.

Clear all Mode Register bits to "0"

Status Register Bit 7 (IF) to "0"

Bits 5 and 6 (MT and I) to "1"

Halt any current Store, Play or Wait execution

Clear the Store/Play/Wait Command Buffer

"Read Status Register" – A/C 61_H, followed by 1 byte of Reply Data.

Reading	Status Bits
MSB	***Received from 812 First***
7	**Interrupt Condition (Flag)**
1	Bit 6 or 5 set to a "1"
0	Cleared condition
6	**Command Buffer**
1	Buffer Empty
0	Cleared condition
5	**Device Condition**
1	Idle
0	Storing, Playing or Waiting
4 3 2 1 0	**Input Power Level**

Table 3 Status Register

Interrupt Condition (Flag) – IF

Set to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a "General Reset" command 01_H). This indication allows monitoring by 'poll' whilst Interrupts are disabled.
Cleared to a logic "0" by a General Reset command or immediately following a read of the Status Register.

Command Buffer Status – MT

Set to a logic "1" when the Command Buffer is empty or by a General Reset command.
Cleared to a logic "0" by loading a new Store, Play, Wait commands.

Device Condition – I

Set to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.
Set to a logic "0" whilst a Store, Play or Wait command is being executed.

Encode Input Power Level – POWER

Available in the Encode mode, a 5-bit representation of the analogue signal input level, updated at the end of every Store or Wait command.

Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the "C-BUS" while the FX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the FX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer from where it will be taken on completion of the previous command.

This permits the FX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the µController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers whilst observing the Status Register – Bit 6.

"Store/Play Page" – A/C 62_H, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).
One Store/Play command (loaded MSB first) will instruct the FX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM.
The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.
If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

					Bit Number												
	MSB – Loaded to FX812 First															***Loaded Last – LSB***	
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Bit**
Value	x	x	x	x	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	**Value**
Page	"0"	"0"	"0"	"0"	DRAM Page Number												Page

DRAM Size	Valid Page Nos	Bit Nos
4Mbit	0 – 4095	0 – 11
1 + 1Mbit	0 – 2047	0 – 10
1Mbit	0 – 1023	0 – 9

"Wait" – A/C 63_H, — Wait for 1024 bit periods

Causes the FX812 to wait for 1024 bit periods (approximately 16 0r 32msec).
If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.
If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

Control Timing Information

Control Timing

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

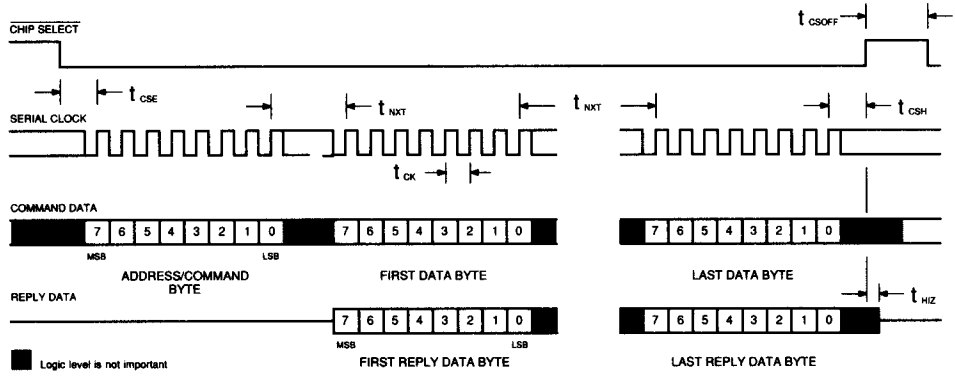


Fig.6 Control Timing Information

NOT TO SCALE

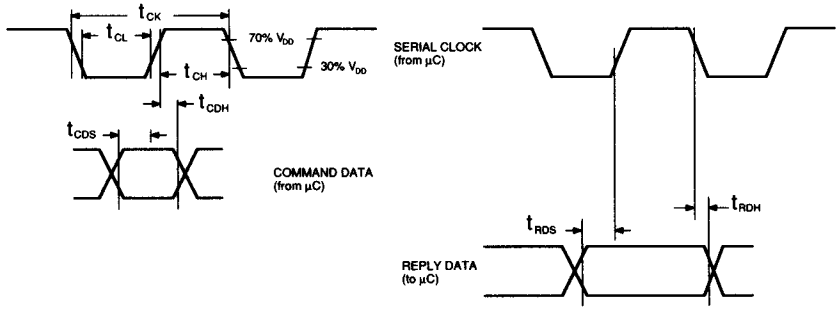


Fig.7 Control Timing Relationships

NOT TO SCALE

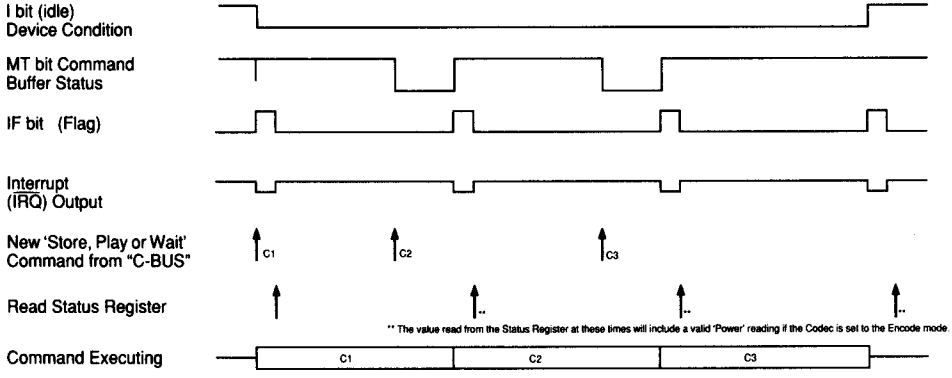


Fig.8 Typical Command Sequences

Control Timing Information .....

Timing Specification – Figures 6 and 7

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"		2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time		2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time		4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Repy Data Hold" Time		50.0	–	–	ns

Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

Memory Size (MS) Bit = "1" – 4Mbit DRAM

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/R2
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18	MA20
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19	MA21

Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19

MA20	MA21	RAS1	A10/R2	DRAM Selected
0	x	active		"first"
1	x		active	"second"

x = don't care

Table 4 Address Line Decoding

		Xtal/clock Frequency (MHz)		
Sample Rate (SR) Bit	Division Ratio	4.0	4.032	4.096
		Sampling Rate (kbits/s)		
SR = "1"	64	62.50	63.00	64.00
SR = "0"	128	31.25	31.50	32.00
		Internal Clock Rate (kHz)		
Local Decoder Clock		125.0	126.0	128.0

Table 5 Sampling Clock Rates Available

Performance

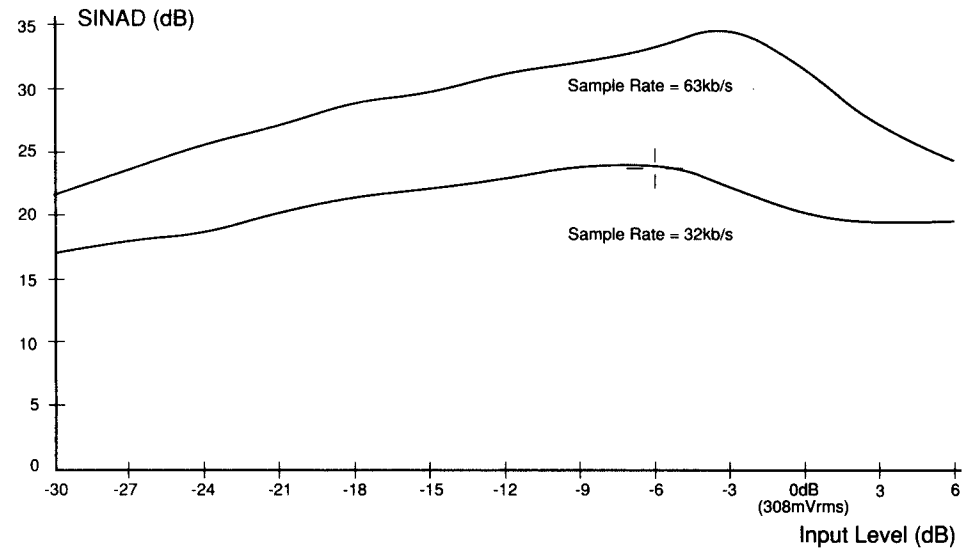


Fig.9 Typical "SINAD vs Input Level" Plot

Performance

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kb/s and 63kb/s sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 whilst the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "11111_2" (31_{10}).

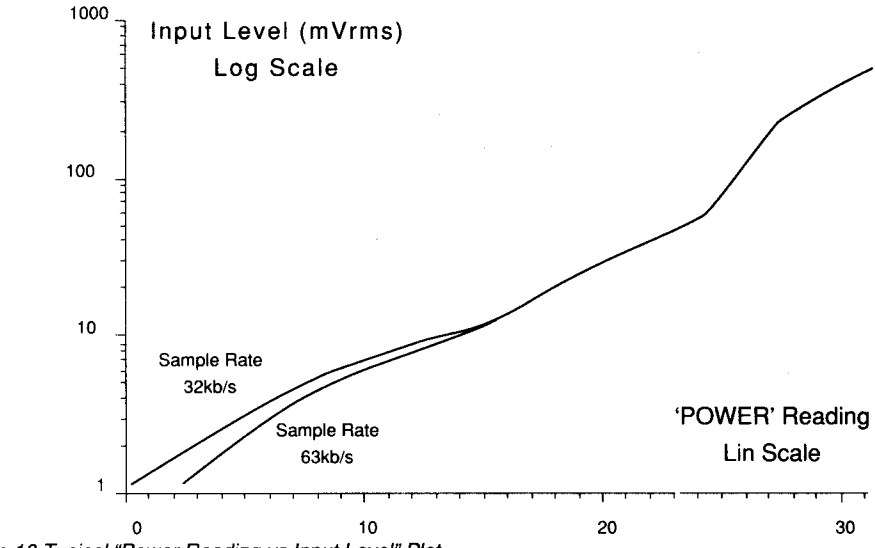


Fig.10 Typical "Power Reading vs Input Level" Plot

Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref. V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX812DW**	-40°C to +85°C (plastic)
	FX812J	-40°C to +85°C (cerdip)
Storage temperature range:	**FX812DW**	-40°C to +85°C (plastic)
	FX812J	-55°C to +125°C (cerdip)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.00MHz. Audio level 0dB ref: = 308mV rms @ 1.0kHz.
Reply Data Line loaded with 50pF//200kΩ to V_{SS}.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current						
Enabled		1	–	3.0	–	mA
Powersaved		1	–	1.0	–	mA
Analogue Input Impedance			–	100	–	kΩ
Analogue Output Impedance (Decode)			–	1.0	–	kΩ
Analogue Output Impedance (Encode or Powersave)			–	500	–	kΩ
DRAM Interface						
Input Logic "1"		2	3.5	–	–	V
Input Logic "0"		2	–	–	1.5	V
Output Logic "1"	(at I_o = -120μA)	3	2.7	–	–	V
Output Logic "0"	(at I_o = 120μA)	3	–	–	0.4	V
Input Leakage Current (at V_{IN} = 0 to V_{DD})		4	-1.0	–	1.0	μA
Input Capacitance		2	–	10.0	–	pF
Digital Interface						
Input Logic "1"		5	3.5	–	–	V
Input Logic "0"		5	–	–	1.5	V
I_{IN}	(logic "1" or "0")	5	-1.0	–	1.0	μA
Output Logic Levels						
Output Logic "1"	(-120μA)	6	4.6	–	–	V
Output Logic "0"	(360μA)	7	–	–	0.4	V
I_{Out} Tri-state	(logic "1" or "0")	6	-4.0	–	4.0	μA
Input Capacitance		5	–	–	7.5	pF
IOX	(V_{Out} = 5V)	8	–	–	4.0	μA
Dynamic Values						
"Xtal" Pin Input Frequency Range		12	4.0		4.1	MHz
Store Mode						
Analogue Input Signal Levels		9	-24.0	–	4.0	dB
Analogue Input Signal Frequency Range		9, 10	300		3400	Hz
Recommended Signal Source Impedance		9	–	–	2.0	kΩ
Play Mode						
Analogue Output Signal Levels		13	-7.0	–	-5.0	dB
Output Noise	(idle)	11	–	-55.0	–	dBp
Overall 'Store to Play' Performance						
Output Noise	(Input Short Circuit)	11	–	-50.0	–	dBp
SINAD (**SR** = 32kb/s)	(Input = 1.0kHz @ -6.0dB)	11	–	23.0	–	dB

Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full "C-BUS" compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

Package Outlines

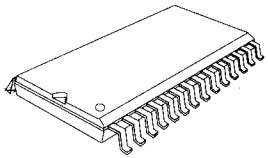
The FX812 is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

Handling Precautions

The FX812 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX812DW 28-pin plastic S.O.I.C. (D1)

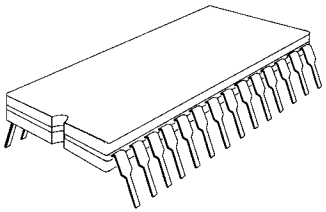
NOT TO SCALE



Max. Body Length 18.05mm
Max. Body Width 7.65mm

FX812J 28-pin cerdip DIL (J5)

NOT TO SCALE



Max. Body Length 37.05mm
Max. Body Width 13.36mm

Ordering Information

FX812DW 28-pin plastic S.O.I.C. (D1)

FX812J 28-pin cerdip DIL (J5)

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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