

Features

- Transient Protection for High-Speed Data Lines-to-GND and Lines-to-Lines.
- Provide Transient Protection for the Protected Lines to
IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air/contact)
IEC 61000-4-4 (EFT) 80A (5/50ns)
IEC 61000-4-5 (Lightning) 45A (8/20 μs) Cable Discharge Event (CDE)
- DFN3020P10E (3.0x2.0mm) Package.
- Specific Pin Out For Easy Board Layout.
- Fast Turn-On and Low Clamping Voltage.
- Low Capacitance for High Speed Interfaces.
- Low Operating Voltage: 3.3V.
- Low Leakage Current
- Solid-State Silicon-Avalanche and Active Circuit Triggering Technology.
- Green part

Applications

- WAN/LAN Device
- 10/100/1000 Ethernet
- LVDS Interfaces
- Switching Systems
- Computers
- Instruments

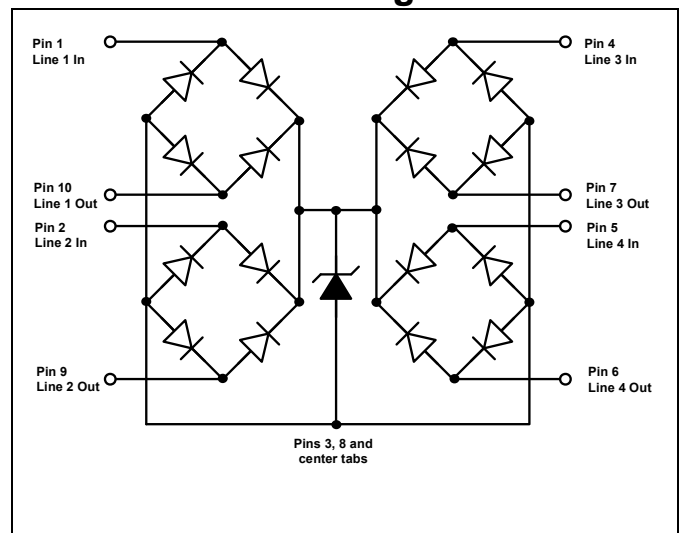
Description

AZ3133-08F is a design which includes surge rated diode arrays to protect high speed data interfaces in an electronic systems. The AZ3133-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

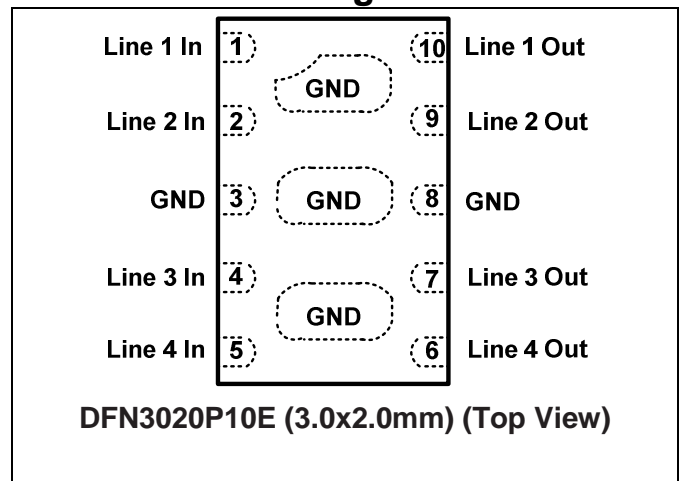
AZ3133-08F is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZ3133-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram



Pin Configuration



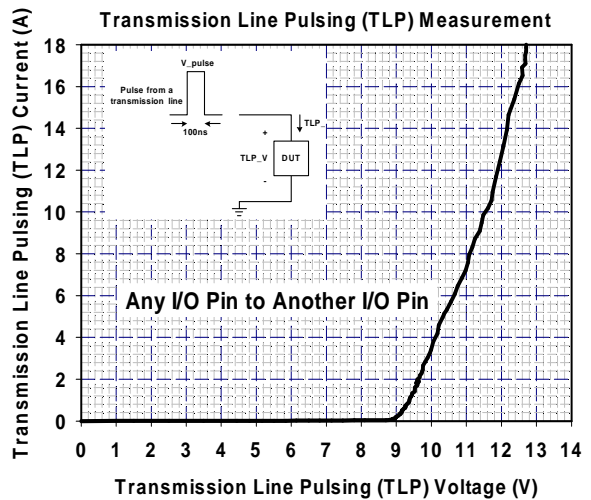
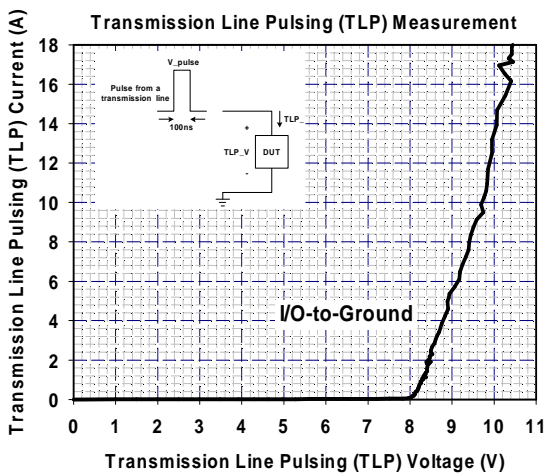
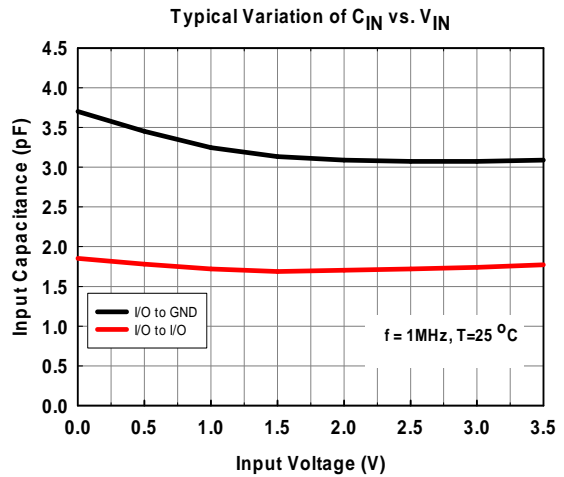
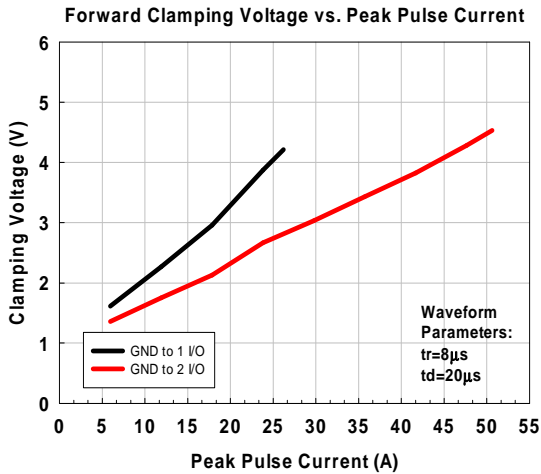
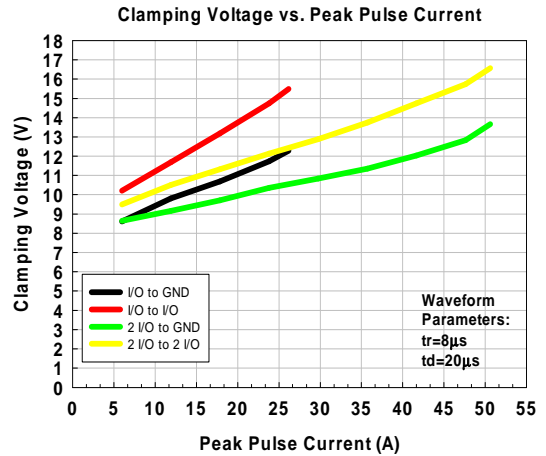
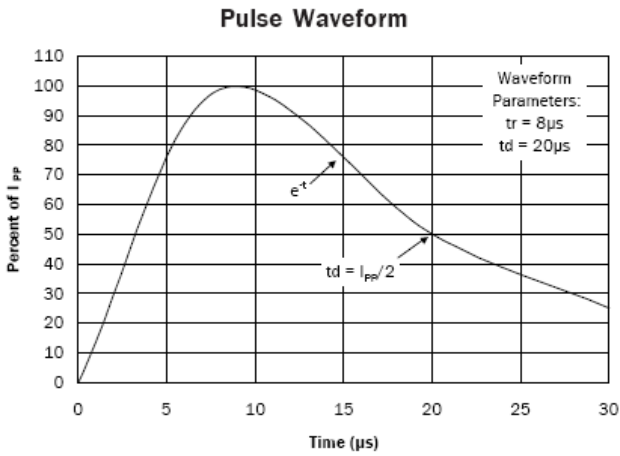


SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp =8/20us) (Note 1)	I _{PP}	45	A
ESD per IEC 61000-4-2 (Air/Contact)	V _{ESD}	±30	kV
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +125	°C
Storage Temperature	T _{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Any I/O Pin to GND, T=25 °C.			3.3	V
Channel Leakage Current	I _{Leak}	V _{RWM} = 3.3V, T=25 °C, Any I/O Pin to GND			0.5	μA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C, Any I/O Pin to GND	3.9			V
Clamping Voltage	V _{CL}	I _{PP} =5A, tp=8/20μs, T=25 °C. Any I/O Pin to GND		9.0	11.0	V
		I _{PP} =15A, tp=8/20μs, T=25 °C. Any I/O Pin to GND		10.5	12.5	V
		I _{PP} =25A, tp=8/20μs, T=25 °C. Any I/O Pin to GND		12.0	14.0	V
		I _{PP} =45A, tp=8/20μs, T=25 °C. Line-to-Line, two I/O pins connected together on each line (Note 1)		15.5	18.0	V
Channel Input Capacitance	C _{IN}	V _R = 0V, f = 1MHz, T=25 °C. Any I/O Pin to GND		3.6	5	pF
		V _R = 0V, f = 1MHz, T=25 °C. Between I/O Pins		1.7		pF

Note 1: Ratings with 2 pins connected together per the recommended configuration (i.e. pin-1 connected to pin-10, pin-2 connected to pin-9, pin-4 connected to pin-7, and pin-5 connected to pin-6).



Applications Information

The AZ3133-08F is designed to protect four high speed data lines operating at 3.3 volts to against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The AZ3133-08F designed with a flow through pin configuration is shown in Fig. 1. Fig. 2 shows a typical PCB layout example with AZ3133-08F for ESD/EFT/Lightning protection. In the Gigabit Ethernet application, pins 1, 2, 4, and 5 should be connected to pins 10, 9, 7, and 6 respectively. The traces should be unbroken and run under the device as shown. To get minimum parasitic inductance, the path length should keep as short as possible. Pins 3, 8 and the three center GND tabs are electrically connected, which should be left floating (i.e. not connected to ground) in the Ethernet application. Fig. 3 shows a typical Gigabit Ethernet protection circuit with AZ3133-08F.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3133-08F.
- Place the AZ3133-08F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.

- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

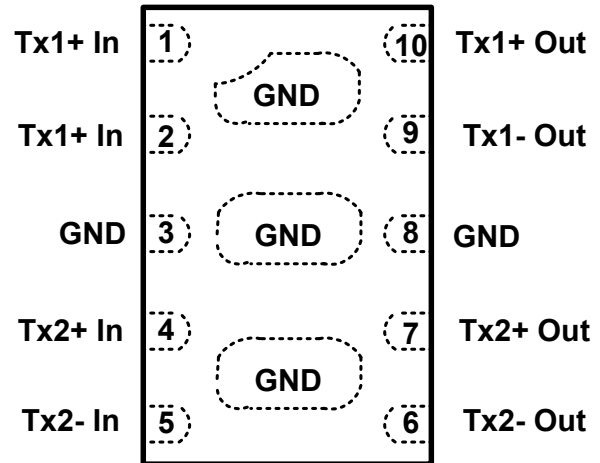


Fig. 1 Pin configuration of AZ3133-08F.

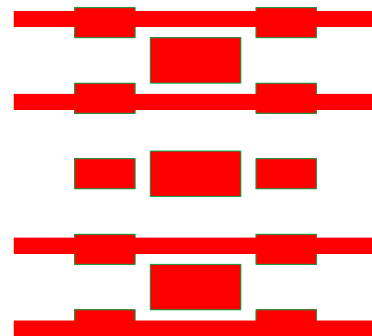


Fig. 2 Layout example of AZ3133-08F.



Gigabit Ethernet LAN Port at MB

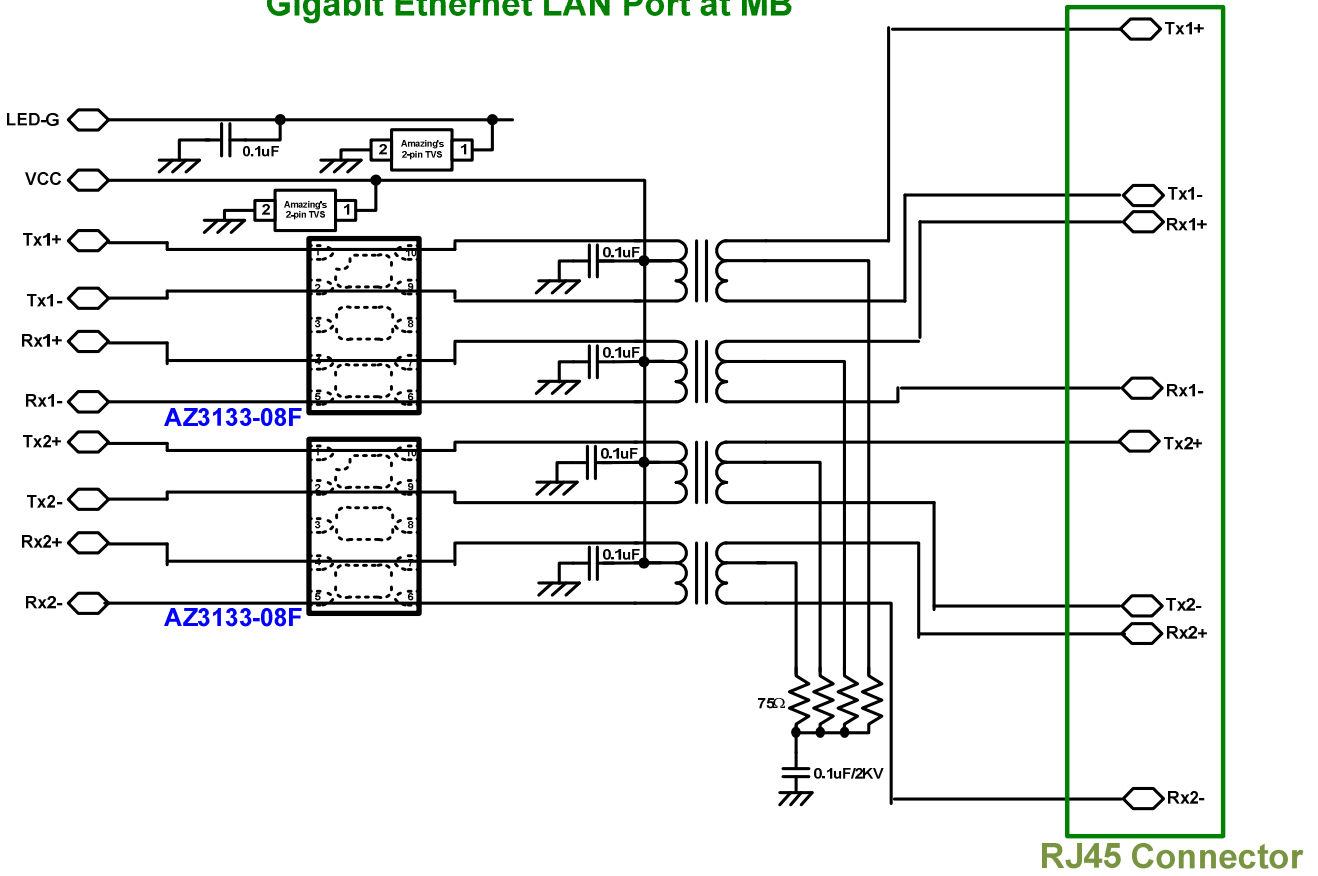
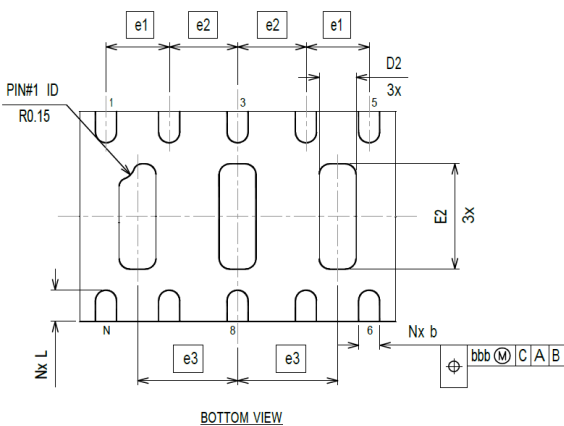
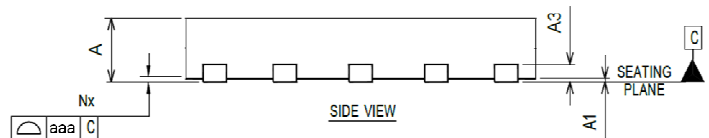
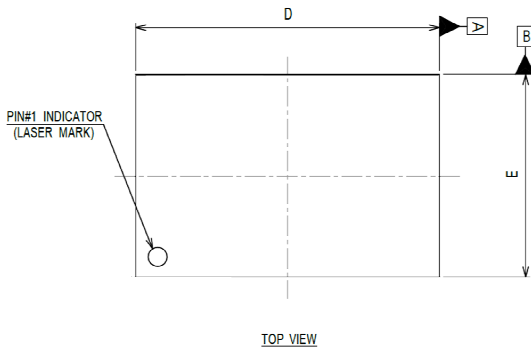


Fig. 3
Gigabit Ethernet surge protection circuit with AZ3133-08F.

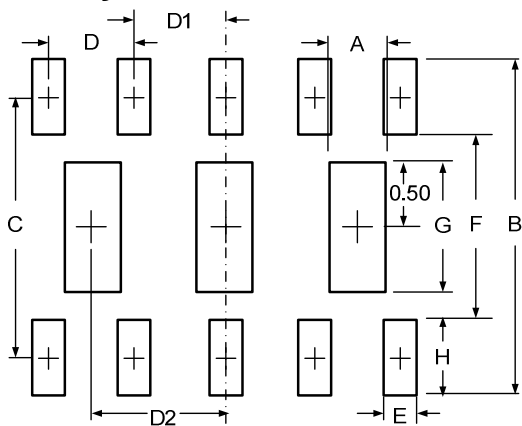
Mechanical Details

DFN3020P10E (3.0x2.0mm) PACKAGE DIAGRAMS



Symbol	Millimeters		
	min	nom	max
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
A3	0.153REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	1.90	2.00	2.10
e1	0.60BSC		
e2	0.65BSC		
e3	0.95BSC		
D2	0.25	0.35	0.45
E2	0.95	1.00	1.05
L	0.25	0.30	0.35
aaa	0.08		
bbb	0.10		

Land Layout



DIMENSIONS	
DIM	MILLIMETERS
A	0.40
B	2.56
C	1.98
D	0.60
D1	0.65
D2	0.95
E	0.25
F	1.40
G	1.00
H	0.58



MARKING CODE



338F = Device Code
W = Date Code
XX = Control Code

Part Number	Marking Code
AZ3133-08F (Green Part)	338F WXXG

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3133-08F.R7G	Green	T/R	7 inch	3,000/reel	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2013/11/12	Preliminary Release
Revision 2014/08/21	Formal Release