AKD4112B-B
AK4112B Evaluation Board Rev.0

GENERAL DESCRIPTION

AKD4112B-B is the evaluation board for AK4112B, 96kHz digital audio receiver. This board has optical, cannon connector and BNC connector to interface with other digital audio equipment.

■ Ordering guide

AKD4112B-B --- Evaluation board for AK4112B
(A cable for connecting with printer port of IBM-AT compatible PC and a control software are packed with this.)

FUNCTION

☐ Digital interface

-S/PDIF :
4 channel input (optical or BNC)
1 channel output (optical or BNC)
- Serial audio data I/F :
1 output (for DIR data output. 10-pin port)
-Serial control data I/F
1 input/output port (10-pin port)

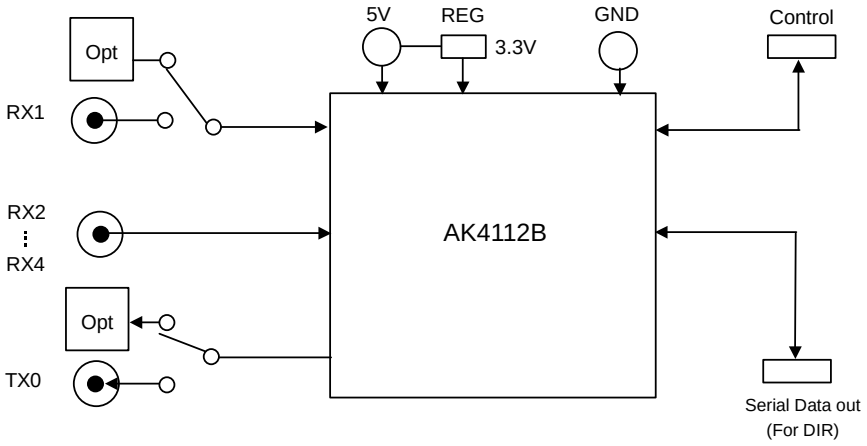


Figure 1. AKD4112B-B Block Diagram
*Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Operating sequence

(1) **Set up the power supply lines.**
[+ 5V] (Red) = 5V
[GND] (Black) = 0V

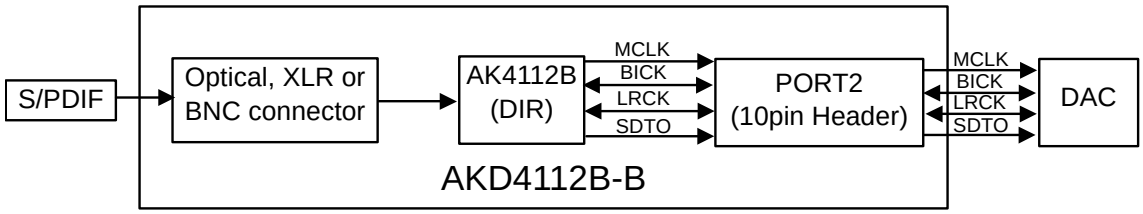
(2) **Set up the evaluation mode and jumper pins.** (Refer to the following item.)

(3) **Connect cables.** (Refer to the following item.)

(4) **Power on.**
The AK4112B should be reset once bringing PDN(SW2) "L" upon power-up.

■ Evaluation modes

(1) Evaluation for DIR
S/PDIF in (optical or BNC) – AK4112B – Serial Data out (10pin port)



The DIR generates MCLK, BICK and LRCK SDTO from the received data through optical connector(PORT1: TORX176) or BNC connector. The AKD4112B-B can be connected with the AKM's DAC evaluation board via 10-line cable.

a. Set-up of Bi-phase Input

RX1 and RX2-4 should not select BNC connector at the same time.

a-1. RX1

Connector	JP2(RX1)
Optical (PORT1)	OPT
BNC (J2)	BNC

Table 1. Set-up of RX1

a-2. RX2, 3 and 4 can be inputted from a BNC (J2) connector only.
Only RX1 can be used in parallel mode.

a-2-1. Set-up of the jumper on the sub board.

Mode	JP19	JP21	JP22
Serial mode	RX2	RX3	RX4
Parallel mode	DIF0	DIF1	DIF2

Table 2. Set-up of the Jumper on the sub board

a-2-2. Set-up of the jumper on the main board.

Input	RX2	RX3	RX4
JP	JP5	JP6	JP7
	Short	Short	RX4

The jumper, which selects the Rx channel, should be Short.
Table 3. Set-up of RX2, 3 and 4

a-3. Set-up of AK4112B input path

It sets up IPS1-0 bits in serial mode.

IPS1 bit	IPS0 bit	INPUT Data	
0	0	RX1	Default
0	1	RX2	
1	0	RX3	
1	1	RX4	

Table 4. Recovery Data Select (Serial)

b. Set-up of clock input and output

The signal level outputted/inputted from PORT2 is 3.3V.

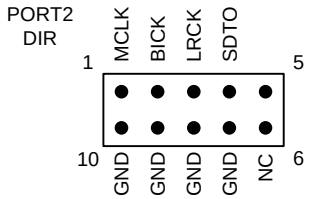


Figure 2. PORT2 pin layout

b-1. MCKO1/MCKO2

The output of MCKO1 pin or MCKO2 pin can be selected by JP12. The output frequency of MCKO1/MCKO2 is selected by OCKS 1-0.

Output signal	JP12	
MCKO1	MCKO1	Default
MCKO2	MCKO2	

Table 5. MCKO1/MCKO2 set-up

OCKS1 pin (SW3_2)	OCKS0 pin (SW3_3)	(X'tal)	MCKO1	MCKO2	fs (max)	
OCKS1 bit	OCKS0 bit					
0	0	256fs	256fs	256fs	108 kHz	Default
0	1	256fs	256fs	128fs	108 kHz	
1	0	512fs	512fs	256fs	54 kHz	
1	1	-	-	-	-	

Table 6. Master Clock Frequency Select

b-2. Set-up of BICK and LRCK input and output

Please select SW 3_7 (DIR_I/O) according to the setup of audio format of AK4112B (Refer to Table 7).

Output signal	SW3_7 (DIR_I/O)	
Slave mode	0	Default
Master mode	1	

Table 7. DIR_I/O set-up

c. Set-up of Audio data format

It sets up by SW 1_2, SW 1_3 and SW1_4 in parallel mode. Please set up DIF2-0 bit in serial mode.

Mode	DIF2 pin (SW1_4)	DIF1 pin (SW1_3)	DIF0 pin (SW1_2)	DAUX	SDTO	LRCK		BICK		
	DIF2 bit	DIF1 bit	DIF0 bit				I/O		I/O	
0	0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
1	0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
2	0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
3	0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
4	1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
5	1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
6	1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
7	1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 8. Audio data format

d. Set-up of CM1 and CM0

The operation mode of PLL is selected by CM1 and CM0. In parallel mode, it can be selected by SW3_1 and JP18. In serial mode, it can be selected by CM1-0 bits.

CM1 pin (SW3_1)	CM0 pin (JP18)	(UNLOCK)	PLL	X'tal	Clock source	SDTO source	
CM1 bit	CM0 bit						
0	0 (CM0="L")	-	ON	ON (Note)	PLL (RX)	RX	Default
0	1 (CDTO/CM0="H")	-	OFF	ON	X'tal	DAUX	
1	0 (CM0="L")	0	ON	ON	PLL (RX)	RX	
		1	ON	ON	X'tal	DAUX	
1	1 (CDTO/CM0="H")	-	ON	ON	X'tal	DAUX	

ON: Oscillation (Power-up), OFF: STOP (Power-Down)

Note: When the X'tal is not used as clock comparison for fs detection (XTL0, 1= "1,1"), the X'tal is OFF.

Table 9. Clock Operation Mode Select

(2) Evaluation for TX
S/PDIF in (optical or BNC)– AK4112B – S/PDIF out (optical or BNC)

a. Set-up of a Bi-phase output signal

As for TX, only the loop back mode of RX corresponds. In serial mode, it can be selected by OPS1-0 bits. This mode is not supported in parallel mode.

Connector	JP13 (TX)
Optical (PORT4)	OPT
BNC (J4)	BNC

Table 10. Set-up of TX

■ Serial control

The AK4112B can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT6 (uP-I/F) with PC by 10-line flat cable packed with the AKD4112B-B. Take care of the direction of connector. There is a mark at pin#1. The pin layout of PORT6 is as Figure 3.

Mode	SW1_6	JP18
Parallel	H	CDTO/CM0="H" or CM0="L"
Serial	L	SDA and CM0="L" short

Table 11. Set-up of parallel mode and serial mode

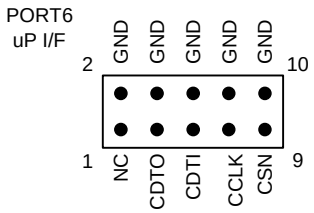


Figure 3. PORT6 pin layout

This evaluation board encloses control software. A software operation procedure is included in an evaluation board manual.

■ **Toggle switch set-up**

SW2	PDN	Reset switch for AK4112B. Set to "H" during normal operation. Bring to "L" once after the power is supplied.

■ **LED indication**

LE1	INT0	Bright when ERF pin goes to "H".
LE2	INT1	Bright when AUTO pin goes to "H".

■ **DIP switch (SW1) set-up: -off- means "L"**

No.	Switch Name	Function	Default
1	IPS0	Don't care	OFF
2	DIF0	Set-up of DIF0 pin. (parallel mode)	OFF
3	DIF1	Set-up of DIF1 pin. (parallel mode)	OFF
4	DIF2	Set-up of DIF2 pin. (parallel mode)	OFF
5	IPS1/IIC	Don't care	OFF
6	P/SN	Set-up of P/SN pin. "OFF": Serial mode, "ON": parallel mode	OFF
7	TEST	Don't care	OFF
8	ACKS	Don't care	OFF

■ **DIP switch (SW3) set-up: -off- means "L"**

No.	Switch Name	Function	Default
1	CM1	Set-up of CM1 pin. (parallel mode)	OFF
2	OCKS1	Set-up of OCKS1 pin. (parallel mode)	OFF
3	OCKS0	Set-up of OCKS0 pin. (parallel mode)	OFF
4	PSEL	Don't care	OFF
5	XTL0	Don't care	OFF
6	XTL1	Don't care	OFF
7	DIR_I/O	Set-up of the transmission direction of 74AC245 "OFF": When inputting from PORT2, "ON": When outputting from PORT2	ON
8	DIT_I/O	Don't care	OFF

■ **Jumper set up.**

No.	Jumper Name	Function
1	D3V/VD	Set-up of Power supply source for 74AC245. D3V : D3V (default) VD : VD
2	RX1	Set-up of RX1 input circuit. OPT : Optical (default) BNC : BNC
5,6,7	RX2-4	Set-up of RX2-4 input circuit.
11,12	DIR MCLK , DIT MCLK	MCKO set-up for PORT5(DIT) and PORT2(DIR) MCKO1 : MCKO1 of AK4112B (default) MCKO2 : MCKO2 of AK4112B
13	TX0	Set-up of TX0 output circuit. OPT : Optical (default) BNC : BNC
18	SDA/CDTO	Set-up of CM0 and Serial mode. Parallel: CM0="L"short → CM0 pin="L" CDTO/CM0="H"short → CM0 pin="H" Serial : SDA and CM0="L"short (default)
19 (Sub)	RX2/DIF0	Set-up depending serial/parallel mode RX2: Serial mode (default) DIF0: Parallel mode
21 (Sub)	RX3/DIF1	Set-up depending serial/parallel mode RX3: Serial mode (default) DIF1: Parallel mode
22 (Sub)	RX4/DIF2	Set-up depending serial/parallel mode RX4: Serial mode (default) DIF2: Parallel mode

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4112B-B according to previous term.

2. Connect IBM-AT compatible PC with AKD4112B-B by 10-line type flat cable (packed with AKD4112B-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4112B-B Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4396.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ Explanation of each buttons

1. [Port Reset] : Set up the USB interface board (AKDUSBIF-A) .
2. [Write default] : Initialize the register of AK4112B.
3. [All Write] : Write all registers that is currently displayed.
4. [Function1] : Dialog to write data by keyboard operation.
5. [Function3] : The sequence of register setting can be set and executed.
6. [Function4] : The sequence that is created on [Function3] can be assigned to buttons and executed.
7. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
8. [SAVE] : Save the current register setting.
10. [OPEN] : Write the saved values to all register.
11. [Write] : Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4112B, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4112B, click [OK] button. If not, click [Cancel] button.

3. [Save] and [Open]

3-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

3-2. [Open]

The register setting data saved by [Save] is written to AK4112B. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

4. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

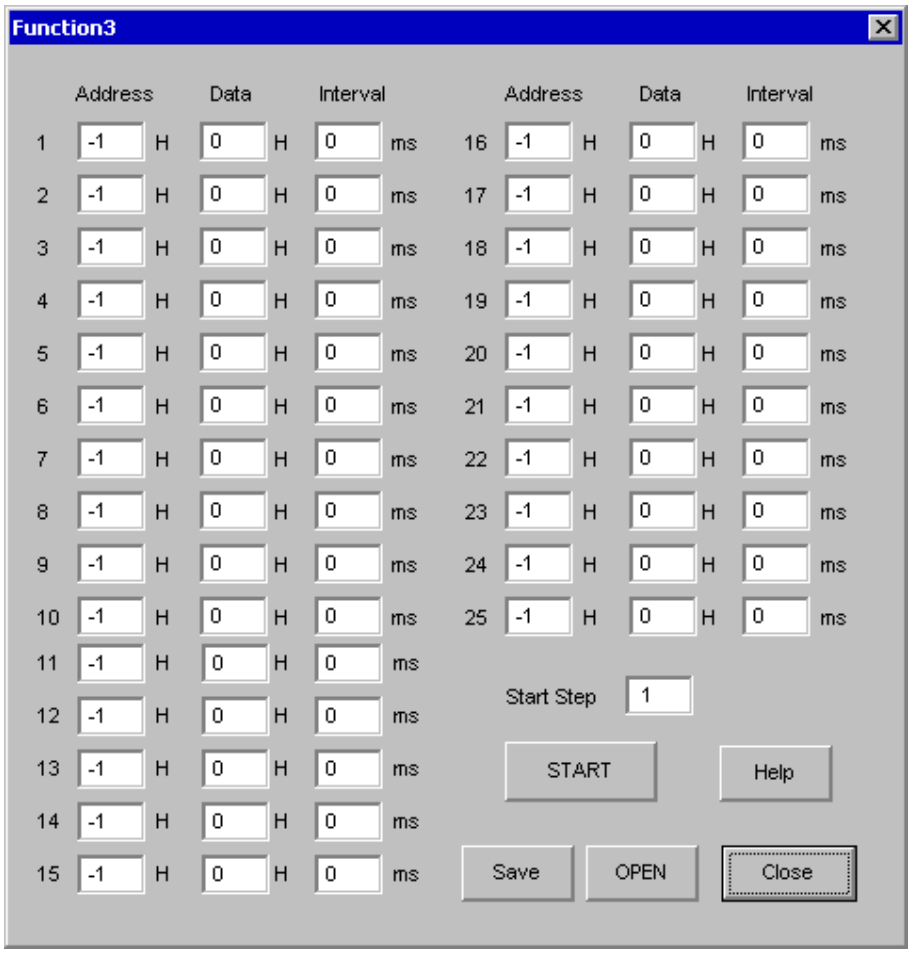


Figure 4. Window of [F3]

5. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 5 opens.

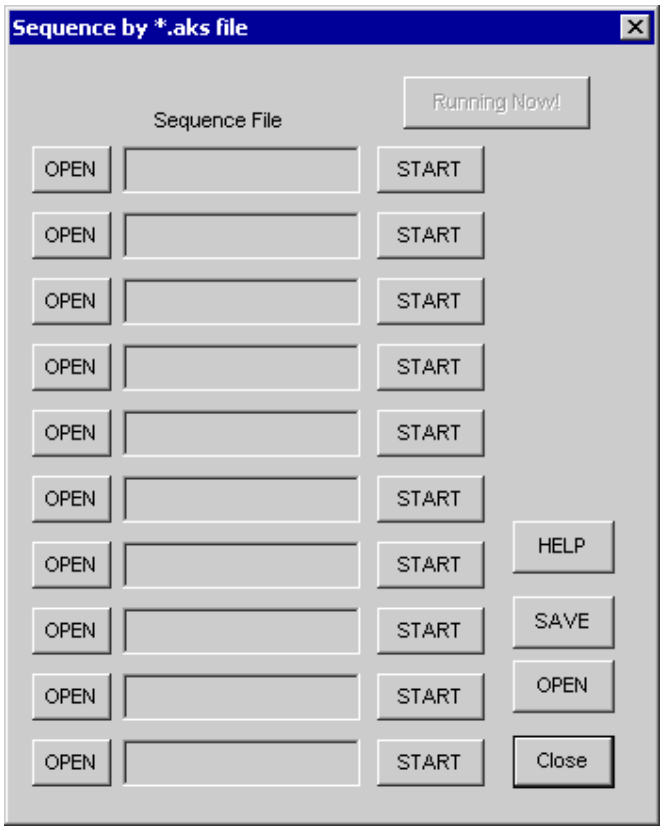


Figure 5. [F4] window

5-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 6.

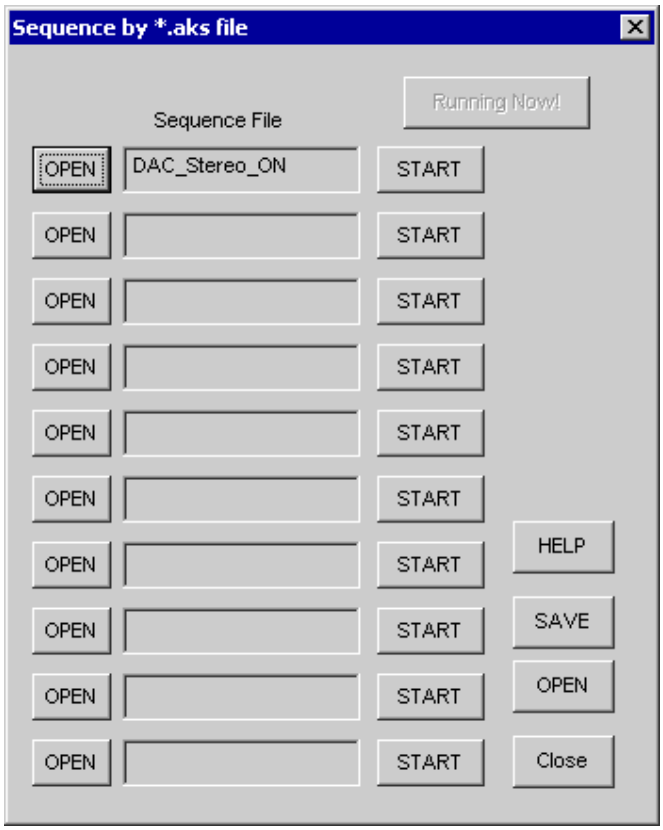


Figure 6. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

5-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

5-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

6. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 7opens.

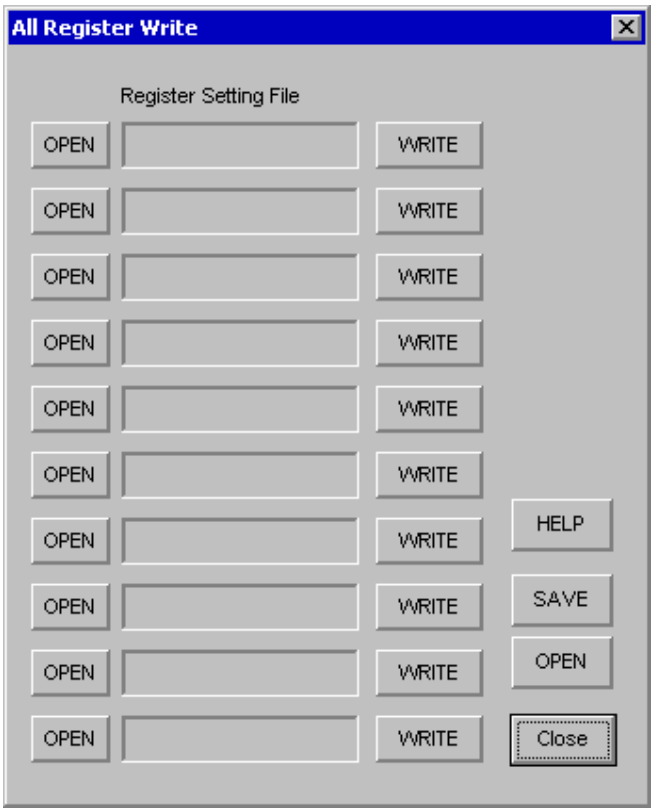


Figure 7. [F5] window

6-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

6-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

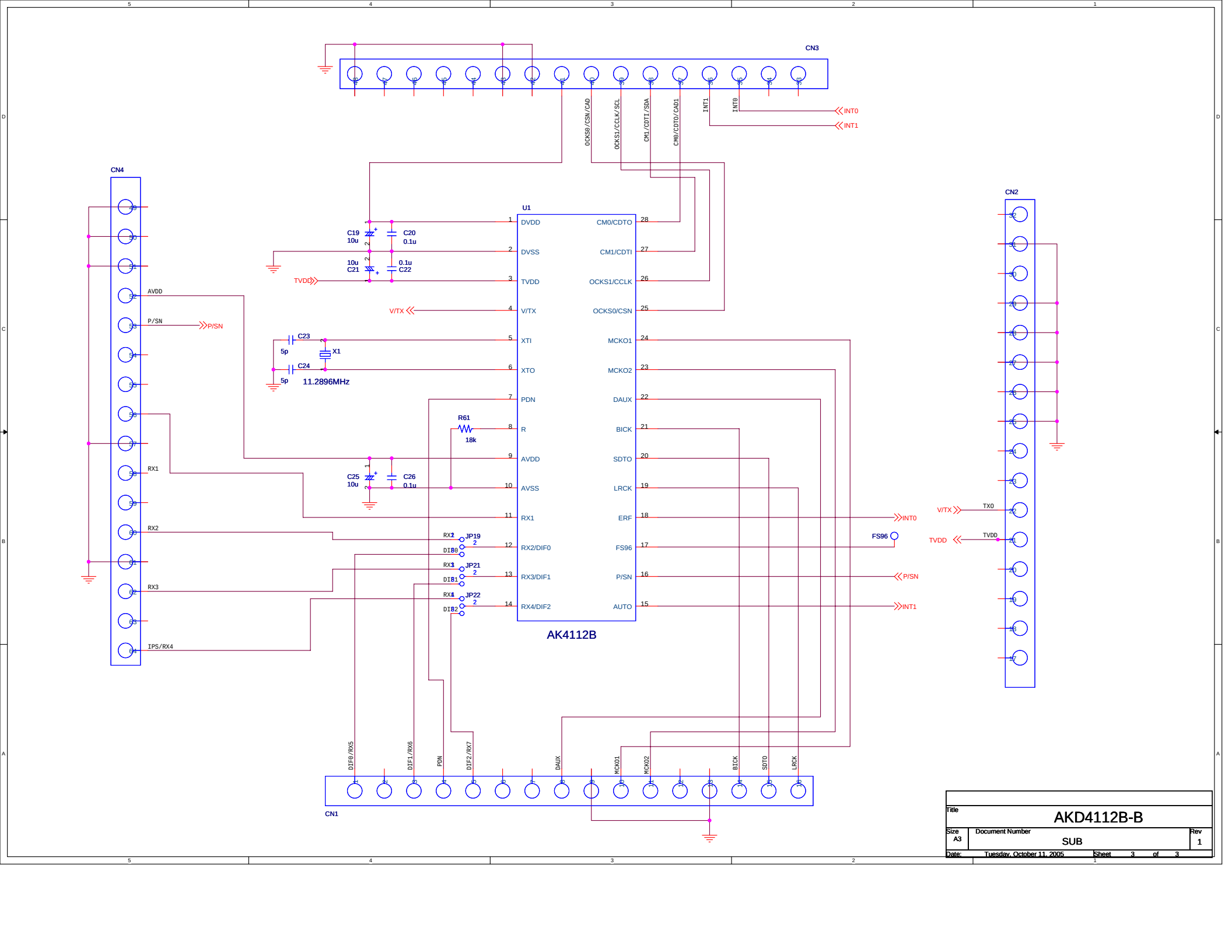
(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

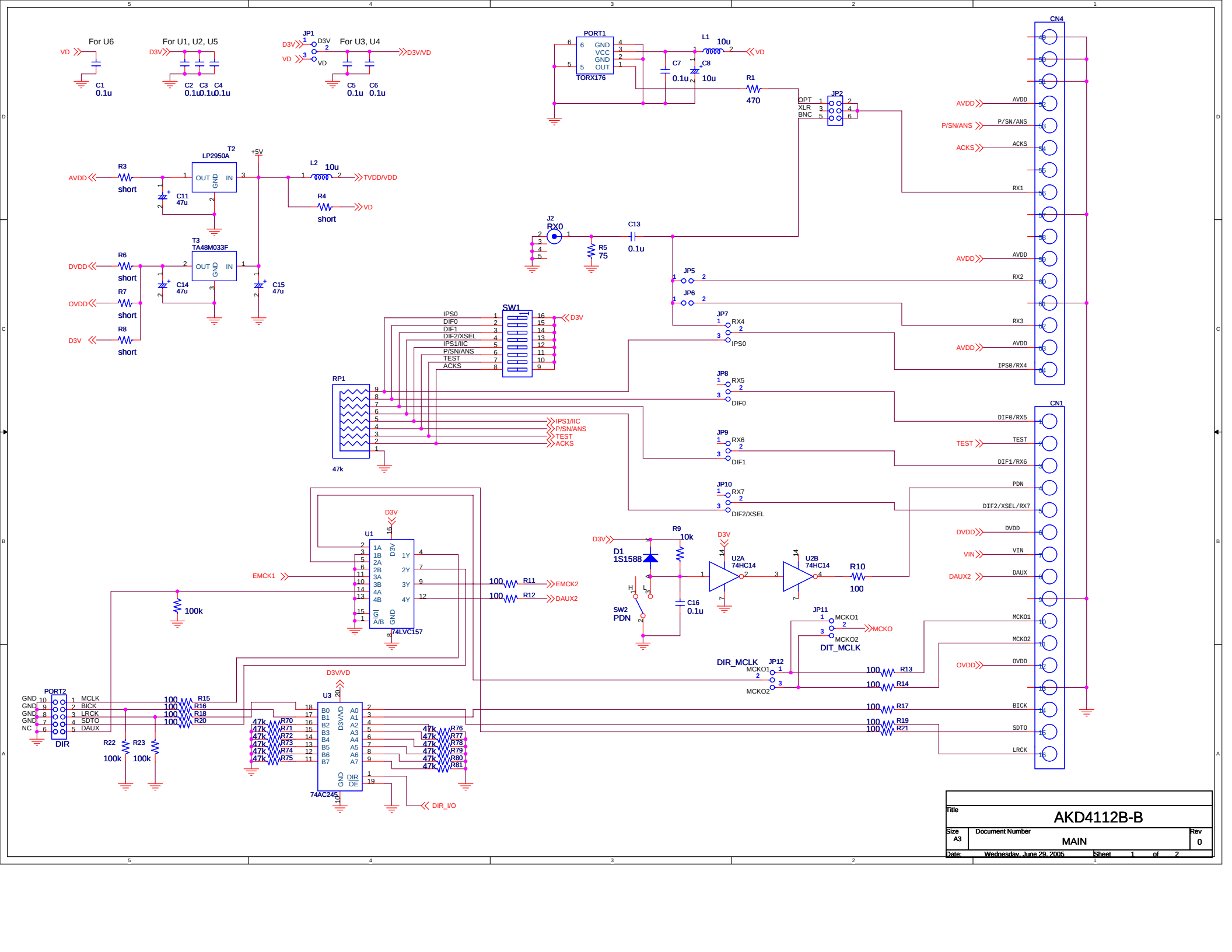
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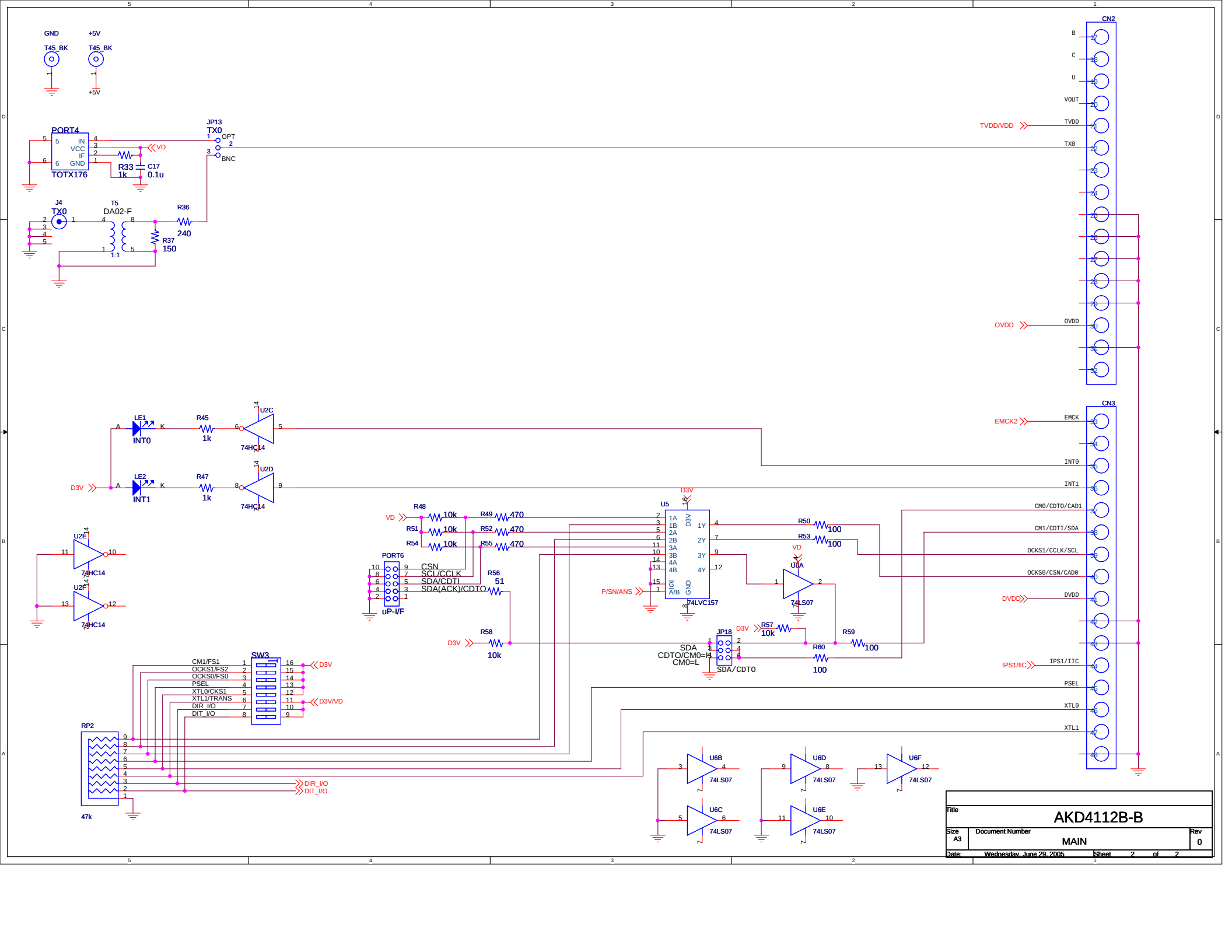
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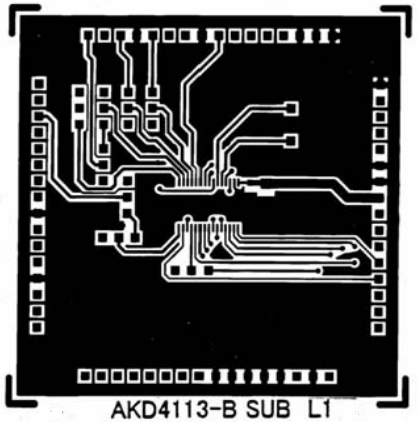
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CN3
INT0
INT1
CN4
CN2
U1
AK4112B
C19 10u
C20 0.1u
C21 10u
C22 0.1u
C23 5p
C24 5p
X1
11.2896MHz
C25 10u
C26 0.1u
R61 18k
JP19
JP21
JP22
DVDD
DVSS
TVDD
V/TX
XTI
XTO
PDN
R
AVDD
AVSS
RX1
RX2/DIF0
RX3/DIF1
RX4/DIF2
CM0/CDTO
CM1/CDTI
OCKS1/CCLK
OCKS0/CSN
MCKO1
MCKO2
DAUX
BICK
SDTO
LRCK
ERF
FS96
P/SN
AUTO
CN1
AVDD
P/SN
RX1
RX2
RX3
IPS/RX4
TXO
FS96
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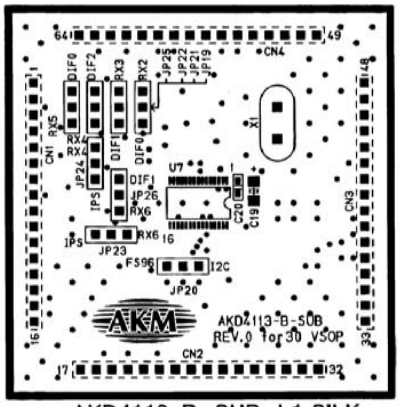
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Size A3	Document Number MAIN	Rev 0
Date: Wednesday, June 29, 2005	Sheet 1 of 2	


GND
+5V
T45_BK
T45_BK
PORT4
IN
VCC
IF
GND
TOTX176
VD
R33
1k
C17
0.1u
JP13
TX0
OPT
BNC
J4
TX0
T5
DA02-F
1:1
R36
240
R37
150
CN2
B
C
U
VOUT
TVDD
TX0
OVDD
TVDD/VDD
OVDD
CN3
EMCK
INT0
INT1
CM0/CDTO/CAD1
CM1/CDTI/SDA
OCKS1/CCLK/SCL
OCKS0/CSN/CAD0
DVDD
IPS1/IIC
PSEL
XTL0
XTL1
EMCK2
DVDD
IPS1/IIC
LE1
INT0
LE2
INT1
R45
1k
R47
1k
U2C
U2D
74HC14
D3V
U2E
U2F
74HC14
R48
R49
R51
R52
R54
R55
10k
470
PORT6
CSN
SCL/CCLK
SDA/CDTI
SDA(ACK)/CDTO
uP-I/F
R56
51
R58
10k
U5
74LVC157
P/SN/ANS
R50
R53
100
U6A
74LS07
VD
R57
10k
R59
100
R60
100
JP18
SDA
CDTO/CM0=H
CM0=L
SDA/CDTO
SW3
CM1/FS1
OCKS1/FS2
OCKS0/FS0
PSEL
XTL0/CKS1
XTL1/TRANS
DIR_I/O
DIT_I/O
D3V
D3V/VD
RP2
47k
U6B
U6C
U6D
U6E
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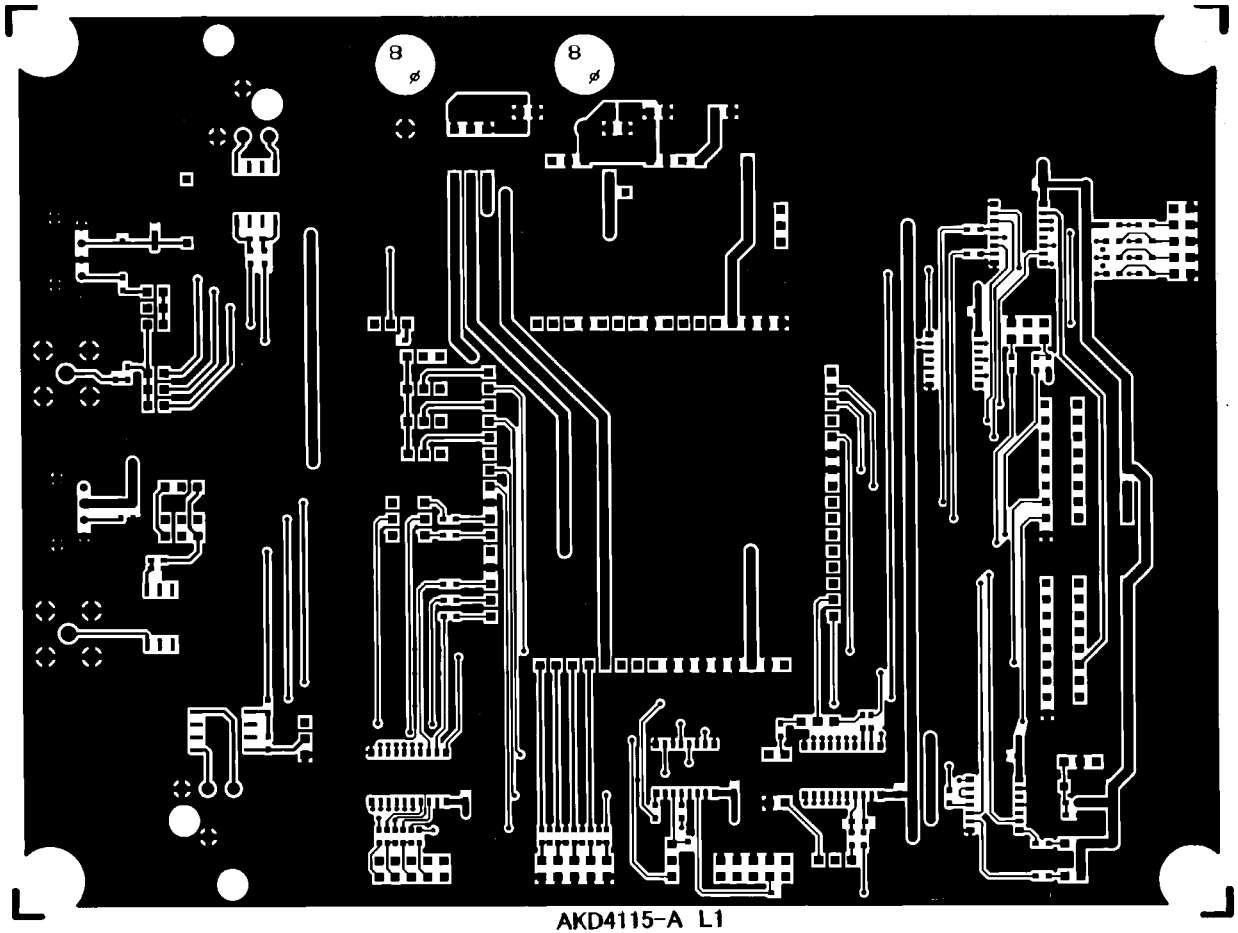
AKD4113-B SUB L1

AKD4113-B SUB L2



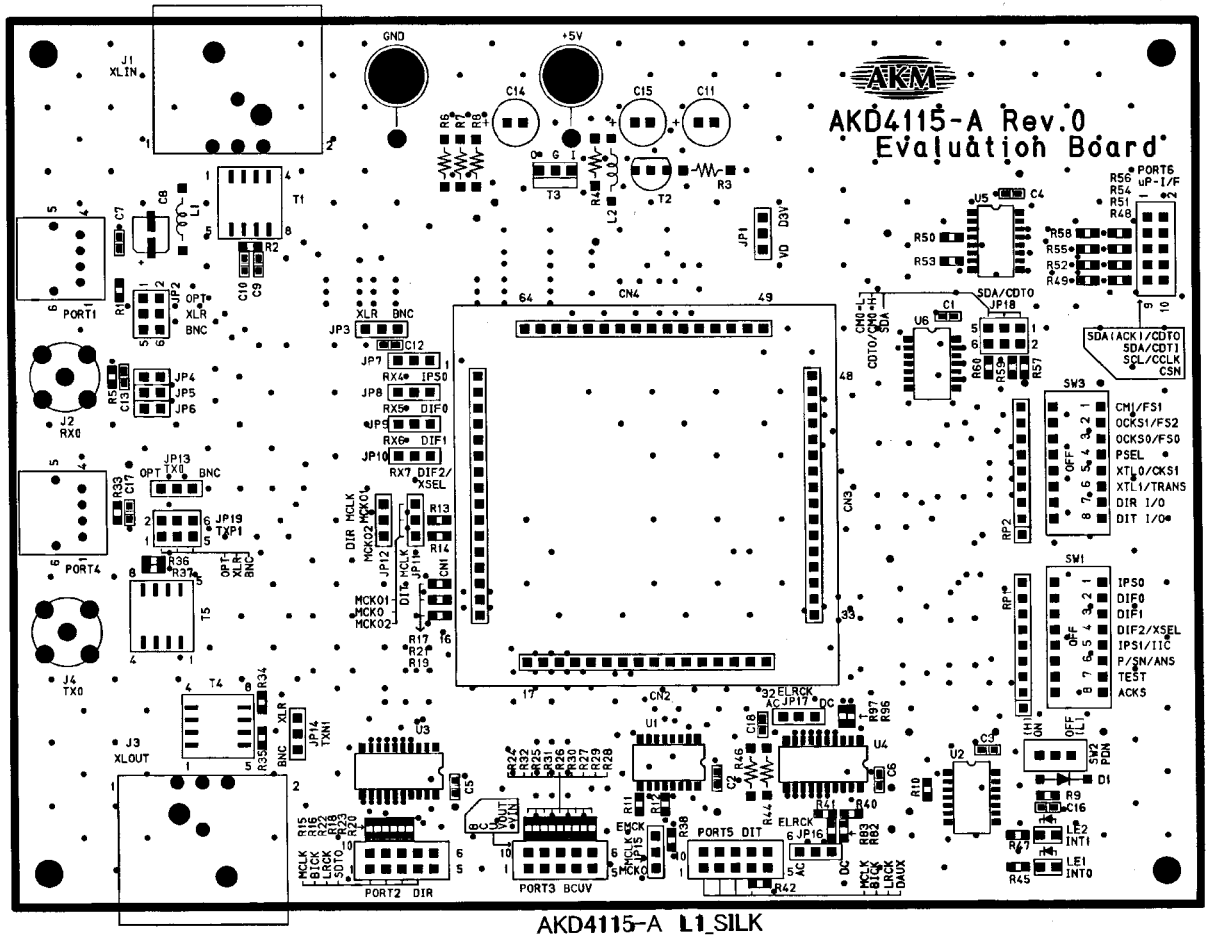
AKD4113-B SUB L1_SILK

AKD4113-B SUB L2_SILK

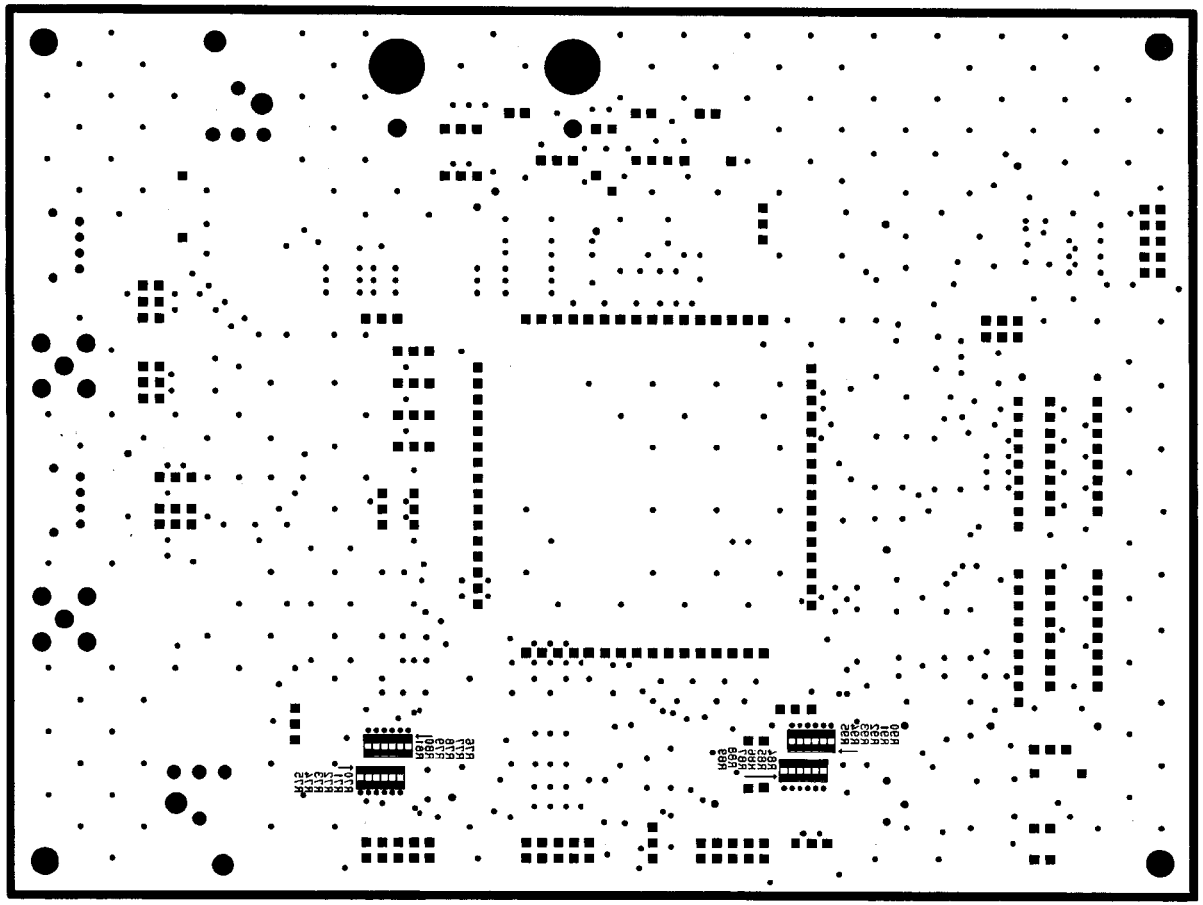


AKD4115-A L1

AKD4115-A L2



AKD4115-A L1_SILK



AKD4115-A L2_SILK