

CD4093B Types

CMOS

Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

■ CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

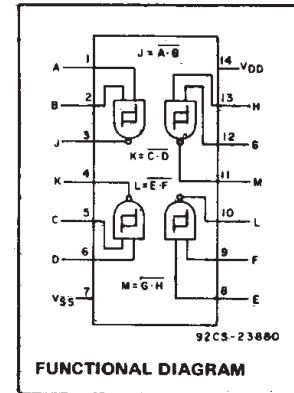
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at $V_{DD} = 5\text{ V}$ and 2.3 V at $V_{DD} = 10\text{ V}$
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temp. Range)	3	18	V

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) $-0.5\text{ V to }+20\text{ V}$

INPUT VOLTAGE RANGE, ALL INPUTS $-0.5\text{ V to }V_{DD} + 0.5\text{ V}$

DC INPUT CURRENT, ANY ONE INPUT $\pm 10\text{ mA}$

PACKAGE THERMAL IMPEDANCE, θ_{JA} (See Note 1):

E package 80°C/W

M package 86°C/W

NS package 76°C/W

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING-TEMPERATURE RANGE (T_A) $-55^\circ\text{C to }+125^\circ\text{C}$

STORAGE TEMPERATURE RANGE (T_{stg}) $-65^\circ\text{C to }+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ inch ($1.59 \pm 0.79\text{ mm}$) from case for 10s max $+265^\circ\text{C}$

NOTE 1: Package thermal impedance is calculated in accordance with JESD 51-7.



* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK

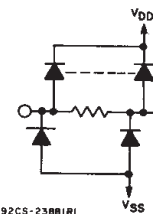


Fig. 1 – Logic diagram—1 of 4 Schmitt triggers.

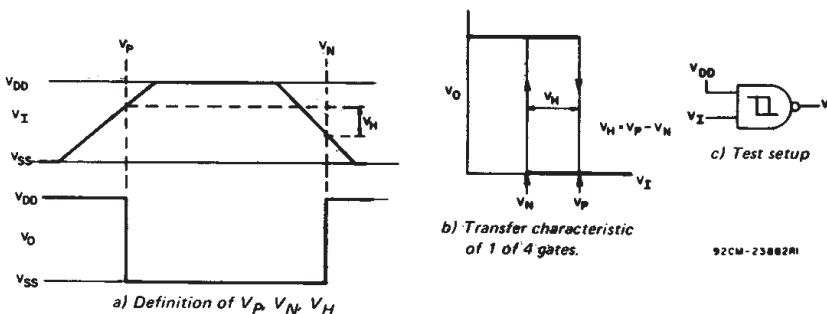


Fig. 2 – Hysteresis definition, characteristic, and test setup.

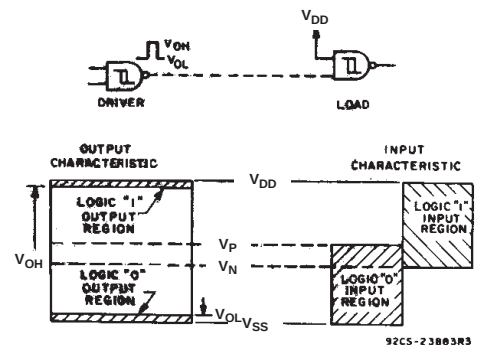


Fig. 3 – Input and output characteristics.

CD4093B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								MIN.	TYP.	MAX.	
Quiescent Device Current, I _{DD} Max.	—	0.5	5	1	1	30	30	—	0.02	1	μA
	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
	—	0.20	20	20	20	600	600	—	0.04	20	
Positive Trigger Threshold Voltage V _p Min.	—	a	5	2.2	2.2	2.2	2.2	2.2	2.9	—	V
	—	a	10	4.6	4.6	4.6	4.6	4.6	5.9	—	
	—	a	15	6.8	6.8	6.8	6.8	6.8	8.8	—	
	—	b	5	2.6	2.6	2.6	2.6	2.6	3.3	—	
	—	b	10	5.6	5.6	5.6	5.6	5.6	7	—	
	—	b	15	6.3	6.3	6.3	6.3	6.3	9.4	—	
V _p Max.	—	a	5	3.6	3.6	3.6	3.6	—	2.9	3.6	V
	—	a	10	7.1	7.1	7.1	7.1	—	5.9	7.1	
	—	a	15	10.8	10.8	10.8	10.8	—	8.8	10.8	
	—	b	5	4	4	4	4	—	3.3	4	
	—	b	10	8.2	8.2	8.2	8.2	—	7	8.2	
	—	b	15	12.7	12.7	12.7	12.7	—	9.4	12.7	
Negative Trigger Threshold Voltage V _N Min.	—	a	5	0.9	0.9	0.9	0.9	0.9	1.9	—	V
	—	a	10	2.5	2.5	2.5	2.5	2.5	3.9	—	
	—	a	15	4	4	4	4	4	5.8	—	
	—	b	5	1.4	1.4	1.4	1.4	1.4	2.3	—	
	—	b	10	3.4	3.4	3.4	3.4	3.4	5.1	—	
	—	b	15	4.8	4.8	4.8	4.8	4.8	7.3	—	
V _N Max.	—	a	5	2.8	2.8	2.8	2.8	—	1.9	2.8	V
	—	a	10	5.2	5.2	5.2	5.2	—	3.9	5.2	
	—	a	15	7.4	7.4	7.4	7.4	—	5.8	7.4	
	—	b	5	3.2	3.2	3.2	3.2	—	2.3	3.2	
	—	b	10	6.6	6.6	6.6	6.6	—	5.1	6.6	
	—	b	15	9.6	9.6	9.6	9.6	—	7.3	9.6	
Hysteresis Voltage V _H Min.	—	a	5	0.3	0.3	0.3	0.3	0.3	0.9	—	V
	—	a	10	1.2	1.2	1.2	1.2	1.2	2.3	—	
	—	a	15	1.6	1.6	1.6	1.6	1.6	3.5	—	
	—	b	5	0.3	0.3	0.3	0.3	0.3	0.9	—	
	—	b	10	1.2	1.2	1.2	1.2	1.2	2.3	—	
	—	b	15	1.6	1.6	1.6	1.6	1.6	3.5	—	
V _H Max.	—	a	5	1.6	1.6	1.6	1.6	—	0.9	1.6	V
	—	a	10	3.4	3.4	3.4	3.4	—	2.3	3.4	
	—	a	15	5	5	5	5	—	3.5	5	
	—	b	5	1.6	1.6	1.6	1.6	—	0.9	1.6	
	—	b	10	3.4	3.4	3.4	3.4	—	2.3	3.4	
	—	b	15	5	5	5	5	—	3.5	5	

^a Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to V_{DD}.

^b Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

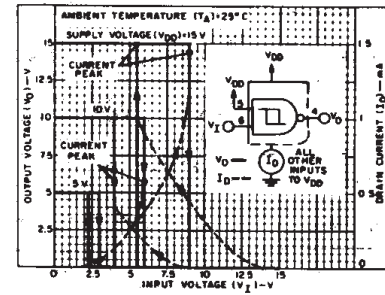


Fig. 4 — Typical current and voltage transfer characteristics.

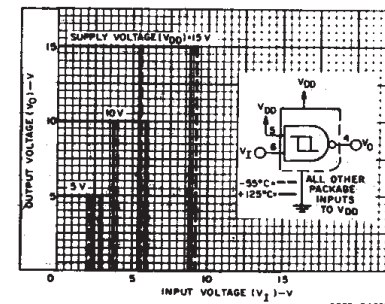


Fig. 5 — Typical voltage transfer characteristics as a function of temperature.

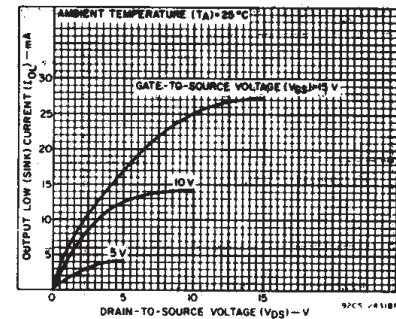


Fig. 6 — Typical output low (sink) current characteristics.

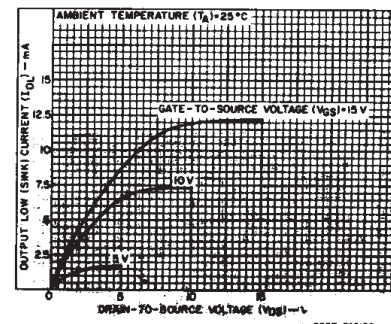


Fig. 7 — Minimum output low (sink) current characteristics.

CD4093B Types

STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								MIN.	TYP.	MAX.	
Output Low (Sink) Current, I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage Low-Level, V _{OL} Max.	—	0.5	5	0.05				—	0	0.05	V
	—	0.10	10	0.05				—	0	0.05	
	—	0.15	15	0.05				—	0	0.05	
Output Voltage High-Level, V _{OH} Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0.10	10	9.95				9.95	10	—	
	—	0.15	15	14.95				14.95	—	—	
Input Current, I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V _{DD} VOLTS	TYP.		MAX.
Propagation Delay Time: t _{PHL} , t _{PLH}		5	190	380	ns
		10	90	180	
		15	65	130	
Transition Time, t _{THL} , t _{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C _{IN}	Any Input		5	7.5	pF

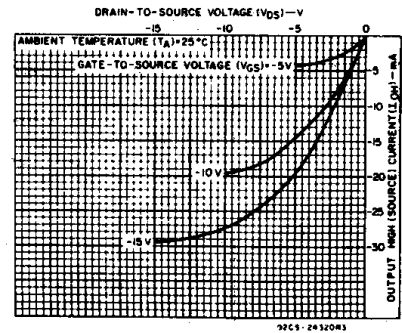


Fig. 8 - Typical output high (source) current characteristics.

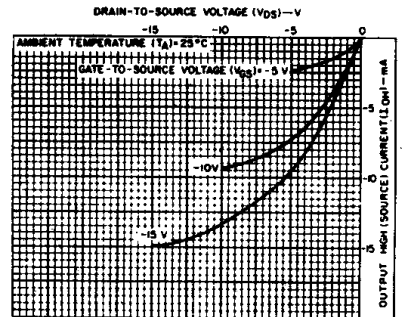


Fig. 9 - Minimum output high (source) current characteristics.

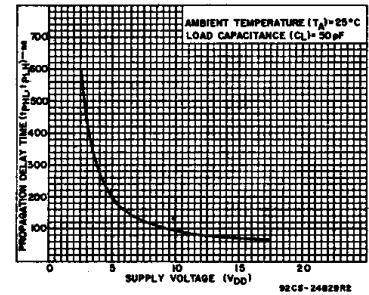


Fig. 10 - Typical propagation delay time vs. supply voltage.

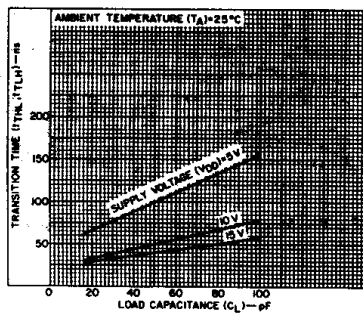


Fig. 11 - Typical transition time vs. load capacitance.

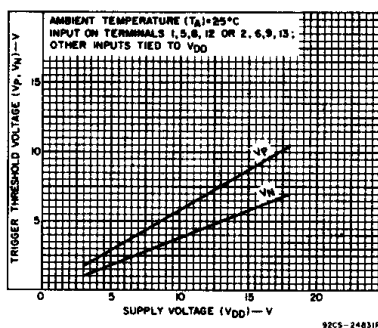


Fig. 12 - Typical trigger threshold voltage vs. V_{DD} .

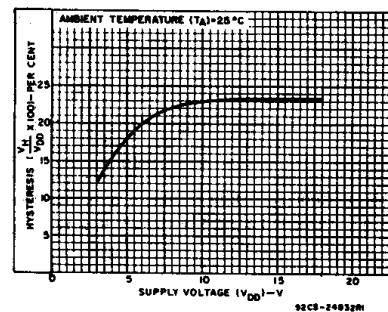


Fig. 13 - Typical per cent hysteresis vs. supply voltage.

CD4093B Types

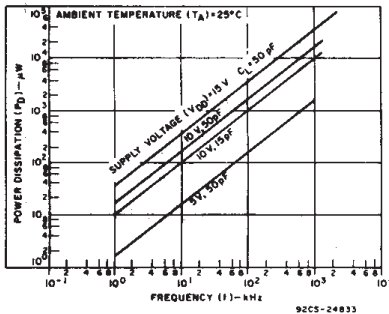


Fig. 14 - Typical power dissipation vs. frequency characteristics.

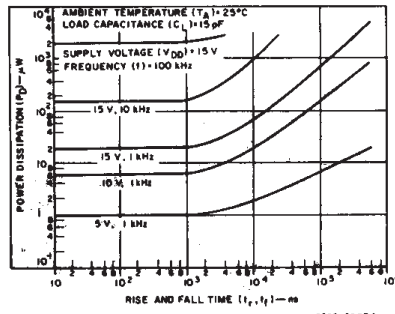


Fig. 15 - Typical power dissipation vs. rise and fall times.

APPLICATIONS

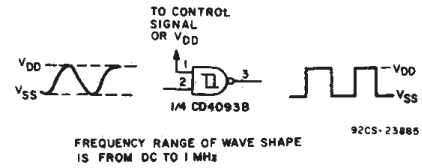


Fig. 16 - Wave shaper.

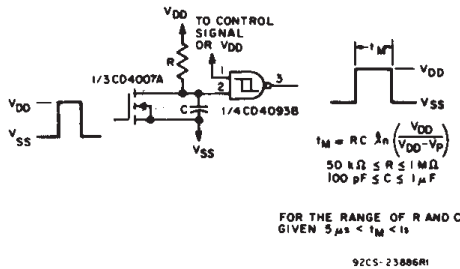


Fig. 17 - Monostable multivibrator.

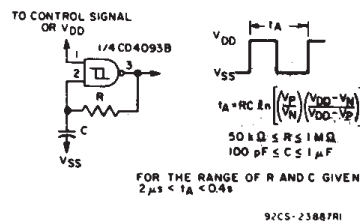


Fig. 18 - Astable multivibrator.

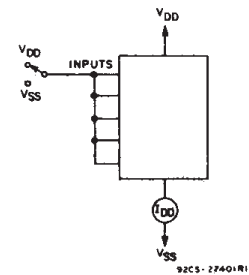


Fig. 19 - Quiescent device current test circuit.

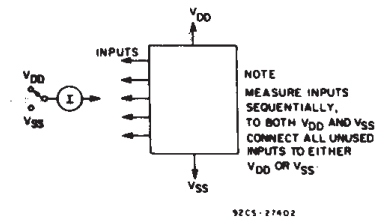


Fig. 20 - Input current test circuit.

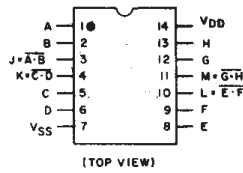


Fig. 21 - Contact Debouncer

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
7704602CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704602CA CD4093BF3A	Samples
CD4093B-W	ACTIVE	WAFERSALE	YS	0		TBD	Call TI	Call TI			Samples
CD4093BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4093BE	Samples
CD4093BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4093BE	Samples
CD4093BF	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4093BF	Samples
CD4093BF3A	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704602CA CD4093BF3A	Samples
CD4093BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093BM	Samples
CD4093BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093B	Samples
CD4093BNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4093B	Samples
CD4093BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM093B	Samples
CD4093BPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM093B	Samples
CD4093BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM093B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4093BPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM093B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4093B, CD4093B-MIL :

- Catalog: [CD4093B](#)
- Automotive: [CD4093B-Q1](#), [CD4093B-Q1](#)
- Military: [CD4093B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4093BM96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4093BMT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD4093BNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4093BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4093BM96	SOIC	D	14	2500	367.0	367.0	38.0
CD4093BMT	SOIC	D	14	250	367.0	367.0	38.0
CD4093BNSR	SO	NS	14	2000	367.0	367.0	38.0
CD4093BPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

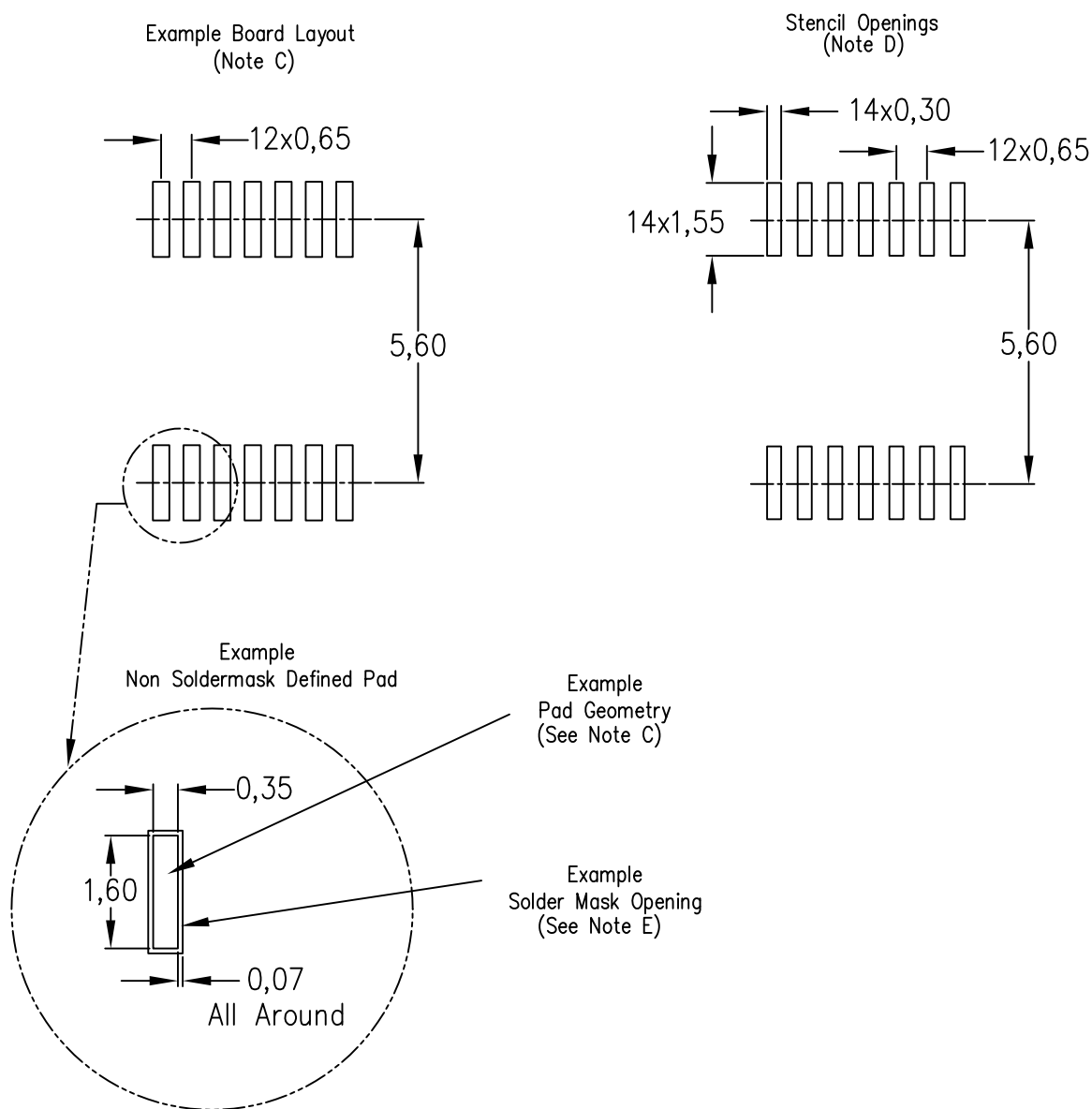
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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