SOT223 N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN4310G

ISSUE 3 - FEBRUARY 1996

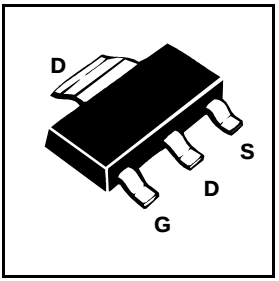
FEATURES

* Very low $R_{DS(ON)}$ = .54Ω

APPLICATIONS

* DC - DC Converters
* Solenoids/Relay Drivers for Automotive

PARTMARKING DETAIL - ZVN4310



ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current at T_{amb}=25°C	I_D	1.67	A
Pulsed Drain Current	I_{DM}	12	A
Gate Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	**3**	**W**
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

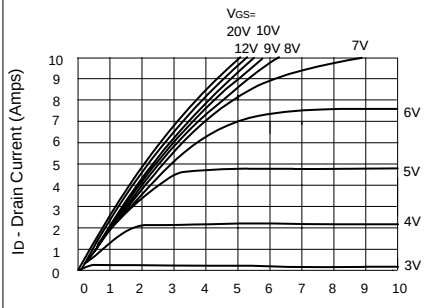
ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	100			V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	1		3	V	I_D=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}			20	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			10 100	µA µA	V_{DS}=100V, V_{GS}=0V V_{DS}=80V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	9			A	V_{DS}=25V, V_{GS}=10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		0.4 0.5	0.54 0.75	Ω Ω	V_{GS}=10V, I_D=3.3A V_{GS}=5V, I_D=1.5A
Forward Transconductance (1)	g_{fs}	0.6			S	V_{DS}=25V,I_D=3.3A
Input Capacitance (2)	C_{iss}			350	pF	V_{DS}=25 V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}			140	pF	
Reverse Transfer Capacitance (2)	C_{rss}			20	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$			8	ns	V_{DD}≈25V, V_{GEN}=10V, I_D=3A R_{GS} =50Ω
Rise Time (2)(3)	t_r			25	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$			30	ns	
Fall Time (2)(3)	t_f			16	ns	

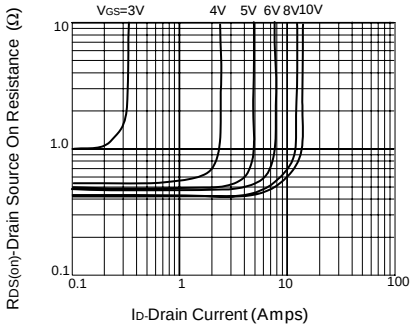
(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2% (2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator
Spice parameter data is available upon request for this device

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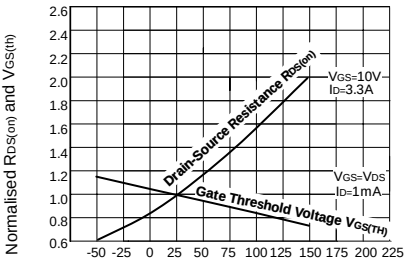
TYPICAL CHARACTERISTICS



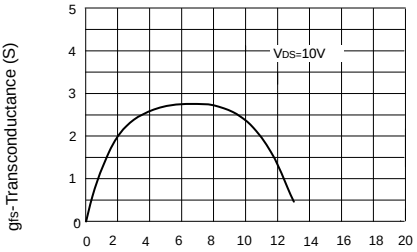
Saturation Characteristics



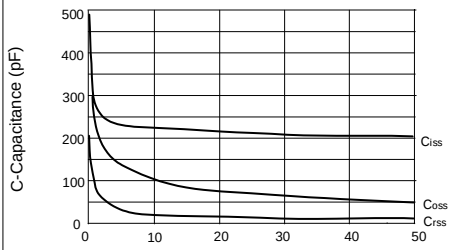
On-resistance v drain current



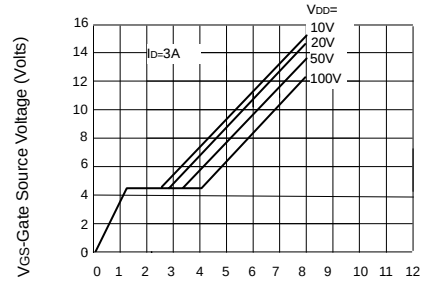
Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v Temperature



Transconductance v drain current



Capacitance v drain-source voltage



Gate charge v gate-source voltage