M37100M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37100M8-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 80-pin plastic molded QFP. This single-chip microcomputer is useful for the high-tech channel-selection system for TVs and VCRs. In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

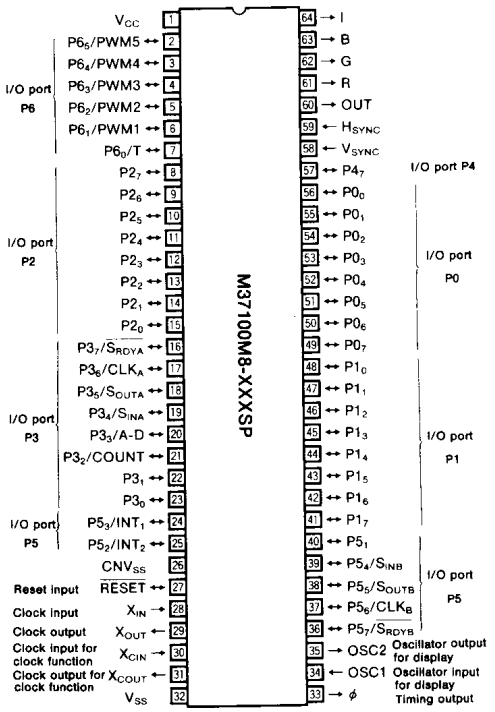
FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ..... 16384 bytes
  - RAM ..... 320 bytes
- Instruction execution time
  - ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V$\pm$10%
- Power dissipation normal operation mode
  - (at 4MHz frequency, CRT display off) 27.5mW
- Subroutine nesting ..... 96levels (Max.)
- Interrupt 9types, 5vectors
- 8-bit timer ..... 3 (2 when used as serial I/O$_A$)
- Programmable I/O ports
  - (Ports P0, P1, P2, P3, P4, P5, P6) 46
- Serial I/O (8-bit) 2
- PWM function ..... 14-bit$\times$1
  - 6-bit$\times$2
- Comparator 1
- Generating function for clock input of EAROM
- Two clock generating circuits
  - (One is for main clock, the other is for clock function)
- 63-character on screen display function
  - Number of character ..... 21 characters$\times$3 lines
  - Character configuration ..... 12$\times$16 dots
  - Kinds of character 96
  - Horizontal character border function

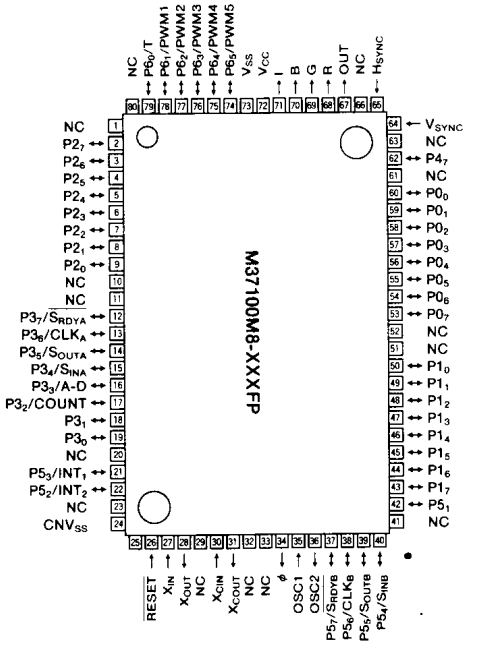
APPLICATION

TV, VCR

PIN CONFIGURATION (TOP VIEW)



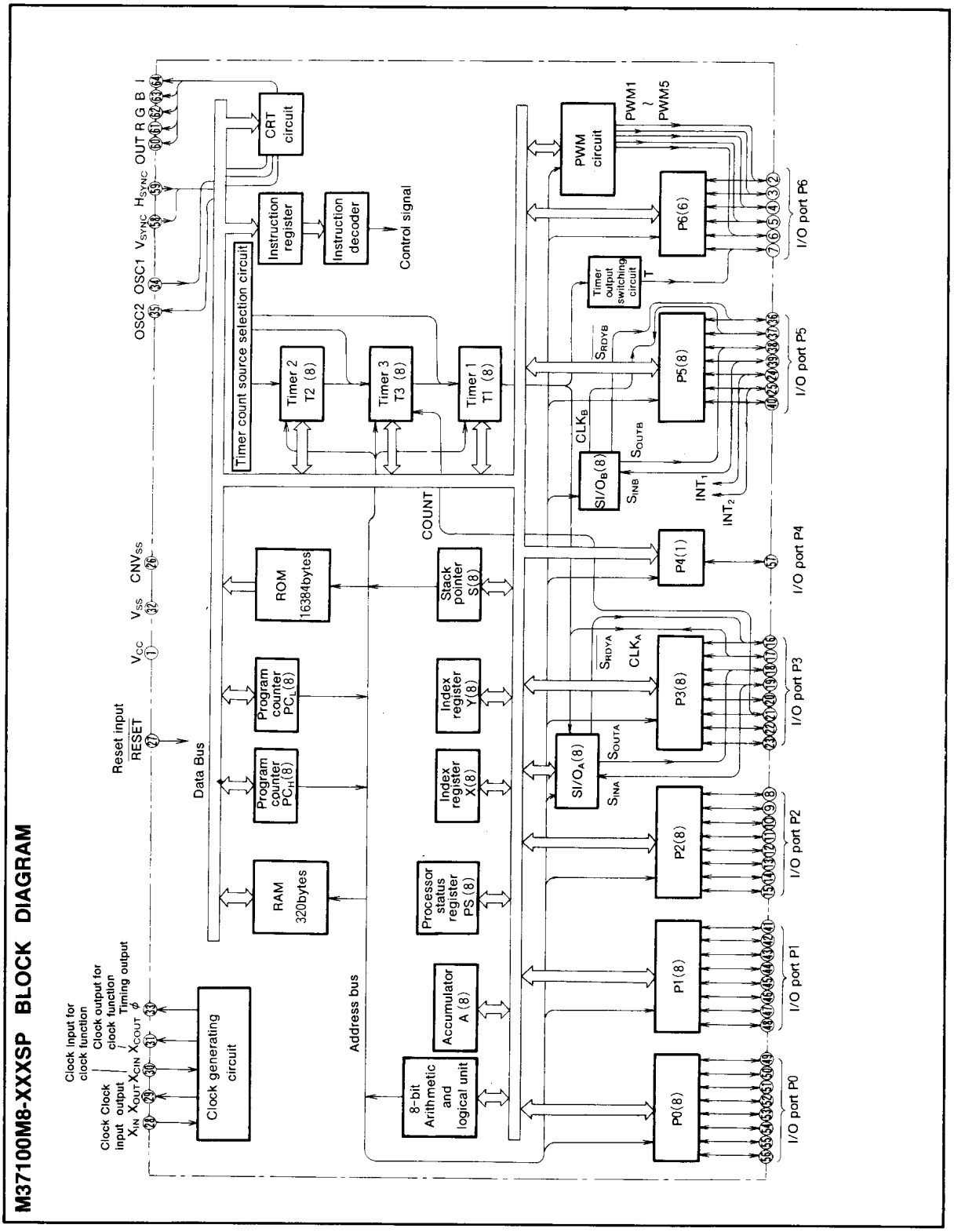
Outline 64P4B



Outline 80P6

NC : No connection

M37100M8-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS OF M37100M8-XXXSP/FP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		16384bytes
	RAM		320bytes
Input/Output ports	P0	I/O	8-bitX1 (middle-voltage N-channel open drain)
	P1, P2	I/O	8-bitX2
	P3	I/O	8-bitX1
	$P4_7$	I/O	1-bitX1
	I, B, G, R, OUT	Output	1-bitX5 (for CRT display function)
	V_{SYNC}, H_{SYNC}	Input	1-bitX2 (for CRT display function)
	$P5_2$, $P5_3$	I/O	2-bitX1 (can be used as an input for either $\overline{INT_2}$ or $\overline{INT_1}$)
	$P5_1$, $P5_4$~$P5_7$	I/O	5-bitX1
	$P6_0$, $P6_1$	I/O	2-bitX1
	$P6_2$~$P6_5$	I/O	4-bitX1 (middle-voltage N-channel open drain)
Serial I/O			8-bitX2
Timers			8-bit timerX3 (X2, when used as serial I/O_A)
Subroutine nesting			96levels (max.)
Interrupt			2 external interrupts, 6 internal interrupts, 1 software interrupt
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator), both circuits have option feedback resistors.
Supply voltage			5V±10%
Power dissipation	at high-speed operation	CRT display function ON	38.5mW (clock frequency X_{IN}=4MHz, f_{CRT}=6MHz)
		CRT display function OFF	27.5mW (clock frequency X_{IN}=4MHz)
	at low-speed operation	CRT display function OFF	0.33mW (clock frequency X_{CIN}=32kHz)
	at stop mode		I_{CC}=1μA (when clock is stopped)
Input/Output characteristics	Input/Output voltage		12V (input/output P0, $P6_2$~$P6_5$, input $\overline{RESET}$, CNV_{SS}) −0.3~V_{CC}+0.3V(P1, P2, P3, $P4_7$, P5, $P6_0$, $P6_1$)
	Output current		0.5mA (P0, P1, P2, P3, P5, $P6_2$ ~ $P6_5$: N-channel open drain input/output) 0.5mA, −0.5mA ($P4_7$: CMOS input/output, R, G, B, I, OUT, $P6_0$~$P6_1$: CMOS output)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M37100M8-XXXSP		64-pin shrink plastic molded DIP
	M37100M8-XXXFP		80-pin plastic molded QFP
CRT display function	Number of character		21 charactersX3lines.
	Kinds of character		96 (12X16 dots)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins and external condensers are connected. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin. In single-chip mode, the output can be controlled by selecting the option.
X_{CIN}	Clock input for clock function	Input	These are the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins and external condensers are connected. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is middle-voltage N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 but the output structure is N-channel open drain. It can be built in pull-up transister at each pin by selecting the option.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P1.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1. When serial I/O_A is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDYA}}$, CLK_A, S_{OUTA}, and S_{INA} pins, respectively. $P3_3$, works as an analog input for comparator and $P3_2$ works as a counter input.
$P4_7$	I/O port P4	I/O	Port $P4_7$ is an 1-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
I, B, G, R, OUT	CRT output	Output	This is an 5-bit output pin for CRT display. The output polarity can be changed by selecting the option. At reset, inactive polarity is selected. The output structure is CMOS output.
H_{SYNC}	H_{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display. The input polarity can be changed by selecting the option.
V_{SYNC}	V_{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display. The input polarity can be changed by selecting the option.
$P5_2$, $P5_3$	I/O port P5	I/O	These ports have basically the same functions as port P1, and are in common with interrupt input pins.
$P5_1$, $P5_4$~$P5_7$			These ports have basically the same functions as port P1. When serial I/O_B is used, $P5_7$, $P5_6$, $P5_5$ and $P5_4$ work as $\overline{S_{RDYB}}$, CLK_B, S_{OUTB} and S_{INB} pins, respectively.
$P6_0$~$P6_5$	I/O port P6	I/O	Port P6 is a 6-bit I/O port and has basically the same functions as port P0. The output structure of $P6_0$, $P6_1$ is CMOS output and the output structure of $P6_2$~$P6_5$ is middle-voltage N-channel open drain. $P6_0$, $P6_1$, $P6_2$, $P6_3$, $P6_4$, $P6_5$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, PWM3, PWM4 and PWM5), respectively.
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function. To control generating frequency, external condensers and registers are connected.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M37100M8-XXXSP/FP is shown in Figure 1. Addresses $C000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 16384 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt section). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $017F_{16}$ are the RAM address area and consist of 320 bytes.

In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

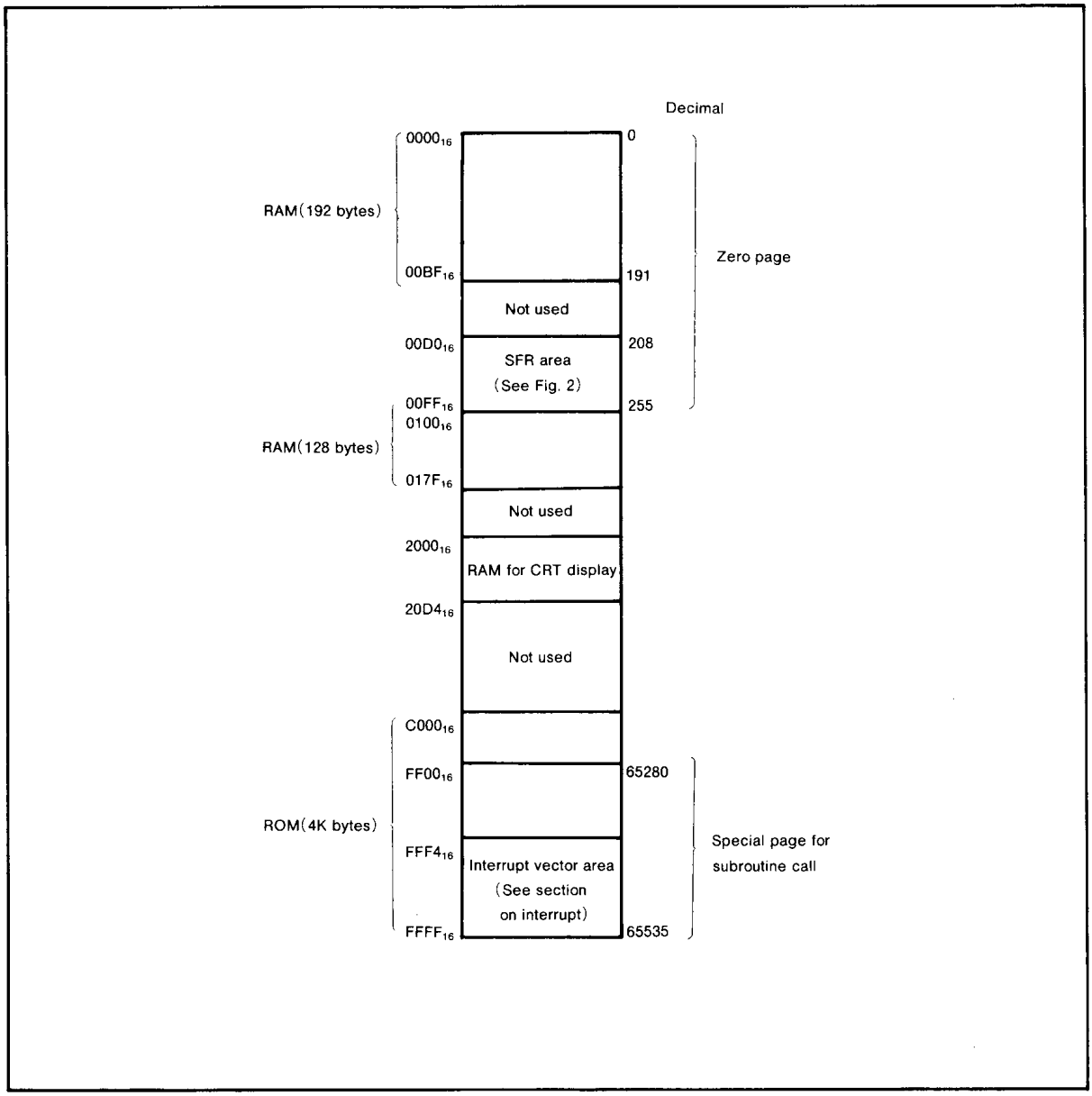


Fig. 1 Memory map

$00D0_{16}$	Horizontal position register
$00D1_{16}$	Vertical position register of block 1
$00D2_{16}$	Vertical position register of block 2
$00D3_{16}$	Vertical position register of block 3
$00D4_{16}$	Color register 0
$00D5_{16}$	Color register 1
$00D6_{16}$	Color register 2
$00D7_{16}$	Color register 3
$00D8_{16}$	CRT control register
$00D9_{16}$	Display block counter
$00DA_{16}$	Serial I/O_B mode register
$00DB_{16}$	Special mode register
$00DC_{16}$	Serial I/O_B register
$00DD_{16}$	Counter 0
$00DE_{16}$	
$00DF_{16}$	
$00E0_{16}$	Port P0
$00E1_{16}$	Port P0 directional register
$00E2_{16}$	Port P1
$00E3_{16}$	Port P1 directional register
$00E4_{16}$	Port P2
$00E5_{16}$	Port P2 directional register
$00E6_{16}$	
$00E7_{16}$	A-D control register

$00E8_{16}$	Port P3
$00E9_{16}$	Port P3 directional register
$00EA_{16}$	Port P4
$00EB_{16}$	Port P4 directional register
$00EC_{16}$	Port P5
$00ED_{16}$	Port P5 directional register
$00EE_{16}$	Port P6
$00EF_{16}$	Port P6 directional register
$00F0_{16}$	PWM1-H register
$00F1_{16}$	PWM1-L register
$00F2_{16}$	PWM2 register
$00F3_{16}$	PWM3 register
$00F4_{16}$	PWM4 register
$00F5_{16}$	PWM control register
$00F6_{16}$	Serial I/O_A mode register
$00F7_{16}$	Serial I/O_A register
$00F8_{16}$	PWM5 register
$00F9_{16}$	PWM output control register
$00FA_{16}$	Timer 1
$00FB_{16}$	Interrupt control register 2
$00FC_{16}$	Timer 2
$00FD_{16}$	Timer 3
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 3.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

STACK POINTER (S)

The stack pointer (S) is an 8-bit register. It is used during subroutine calls and interrupts.

When there is an interrupts, the high-order contents of the program counter is pushed into the address formed by setting the high-order eight bits to 00_{16} and the low-order eight bits to the content of the stack pointer. Next the stack pointer is decremented by one and the low-order content of the program counter is pushed into the address formed by setting the high-order eight bits to 00_{16} and the low-order eight bits to the content of the stack pointer. Then the stack pointer is again decremented by one, the content of the processor status register is pushed into the address formed by setting the high-order eight bits to 00_{16} and the low-order eight bits to the content of the stack pointer, and then the stack pointer is decremented by one once more.

The push operation described above is performed automatically when an interrupt occurs. The RTI instruction is used to return from an interrupt routine.

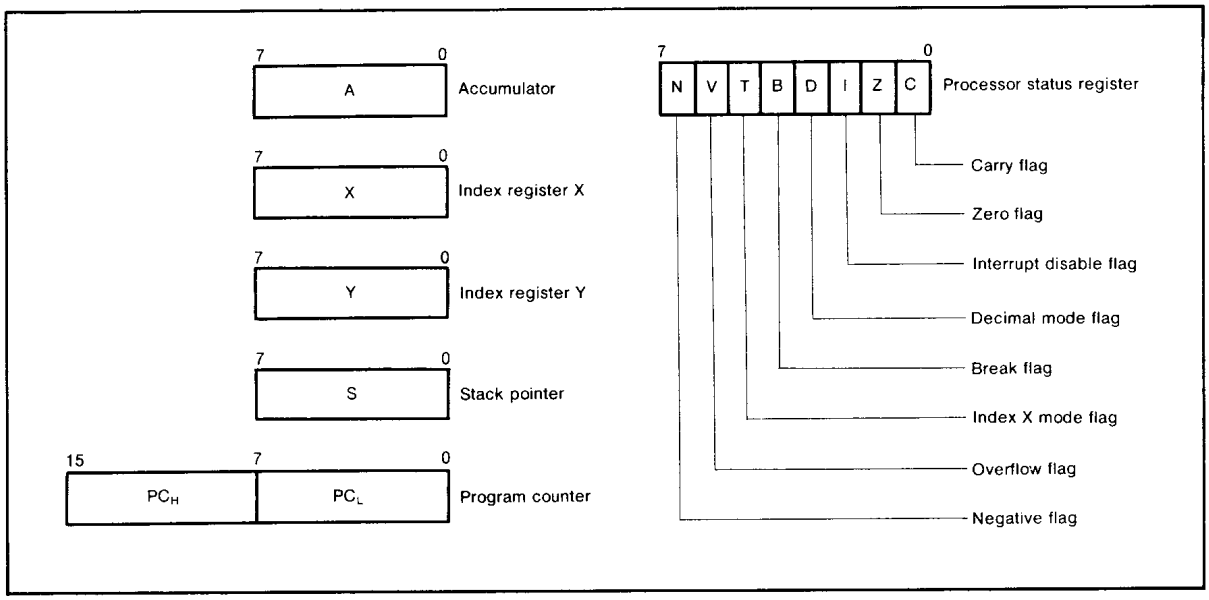


Fig. 3 Register structure

When an RTI instruction is executed, control is returned by reversing the above operation while incrementing the stack pointer by one. The PHA instruction is used to push the accumulator because it is not saved automatically. When the PHA instruction is executed, the content of the accumulator is pushed into the address formed by setting the high-order eight bits to 00_{16} and the low-order eight bits to the content of the stack pointer. Then the content of the stack pointer is decremented by one. The PLA instruction is used to restore the accumulator. When the PLA instruction is executed, the stack pointer is incremented by one and the content of the address formed by setting the high-order eight bits to 00_{16} and the low-order eight bits to the content of the stack pointer is stored in the accumulator. The processor status register is pushed and restored in the same manner with the PHP and PLP instructions. With subroutine calls, only the program counter is pushed. Therefore, registers that must be preserved must be pushed by the program. Use the RTS instruction to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is compleated. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break Flag (B)

The operation of a BRK instruction is similar to an interrupt. The BRK instruction is a non-maskable software interrupt that is used during program debugging. The break flag can be checked only by checking the content of the processor status register (PS) saved during an interrupt. The content of the processor status register (PS) is saved after setting flag B to "1" when the BRK instruction is used as an interrupt. It is cleared to "0" for other interrupts.

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a singed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is clear by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or clearing the negative flag.

INTERRUPTS

Interrupts can be caused by 9 different events consisting of two external, six internal, and one software event.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

Falling edge active or rising edge active for each of the INT_1 and INT_2 external interrupts can be selected by bits 4 and 5 of the PWM control register. Whether the INT_1 and INT_2 external interrupts or the CRT display and serial I/O_B interrupts are to be accepted can be selected by bits 0 and 1 of interrupt control register 2.

Whether the timer 1 or serial I/O_A interrupt is to be accepted can be selected by bit 2 of the serial I/O_A mode register.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits and the interrupt enable bits are in interrupt control register 1 and timer control register. Figure 4 shows the structure of the interrupt control registers 1 and 2 and timer control register.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be clear with a program, but not set. The interrupt enable bit can be set and clear with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_1 or CRT display interrupt	2	$FFFD_{16}$, $FFFC_{16}$	INT_1 external interrupt (phase programmable)
Timer 3 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	
Timer 2 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	
Timer 1 or serial I/O_A interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
INT_2 or serial I/O_B interrupt (BRK instruction interrupt)	6	$FFF5_{16}$, $FFF4_{16}$	INT_2 external interrupt (phase programmable) BRK instruction interrupt (non-maskable software interrupt)

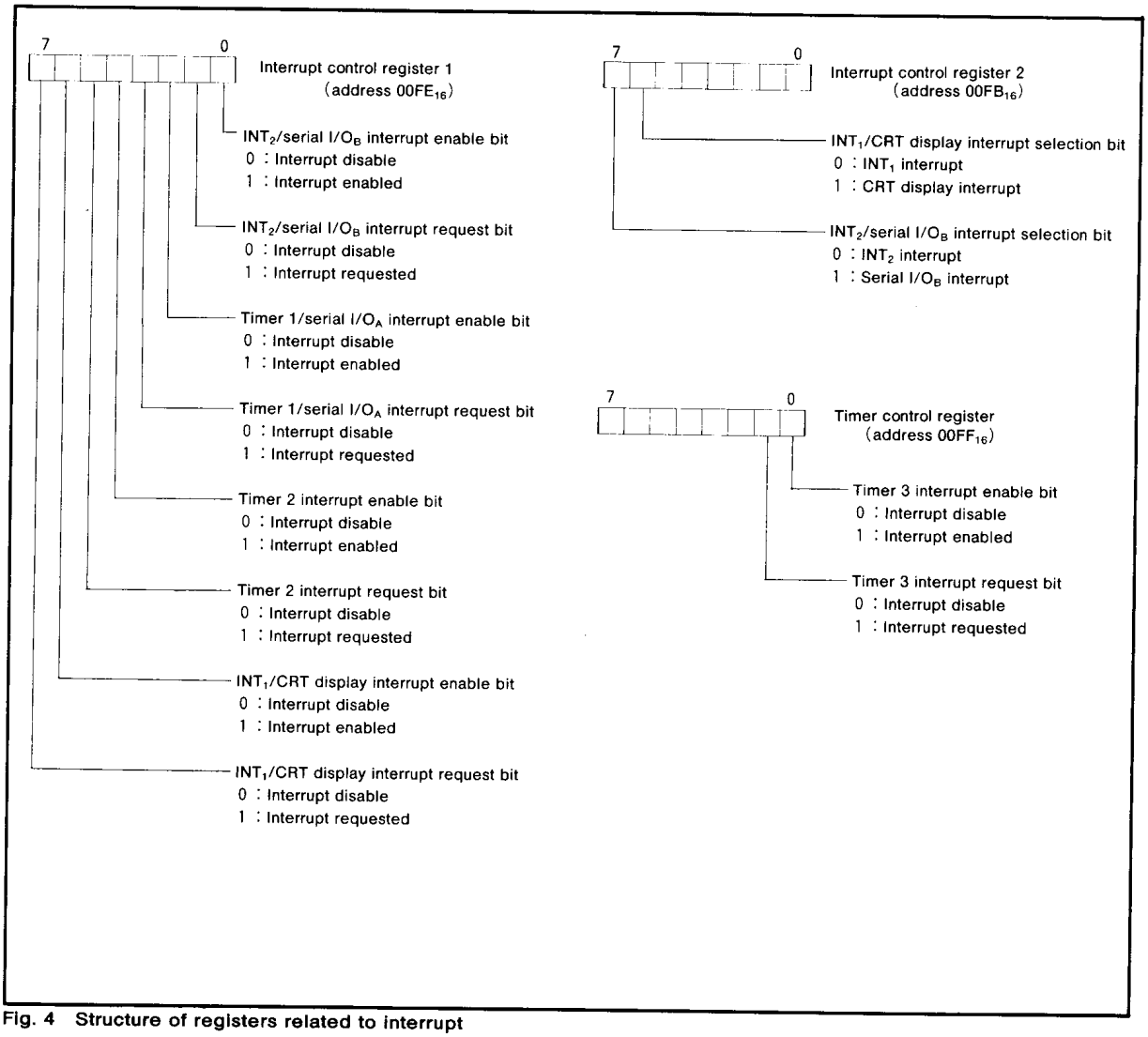


Fig. 4 Structure of registers related to interrupt

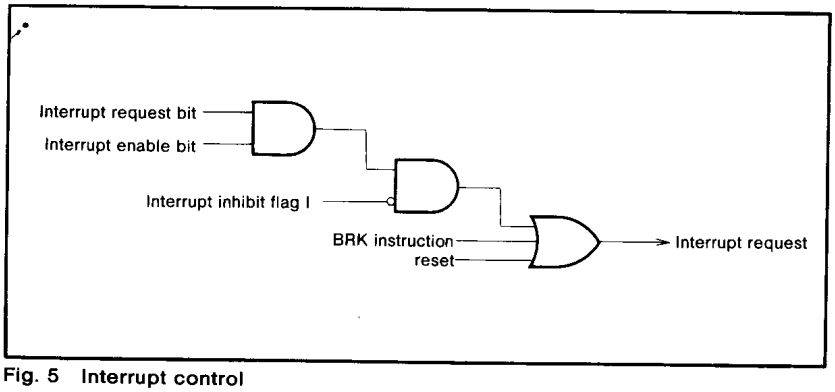


Fig. 5 Interrupt control

TIMER

The M37100M8-XXXSP/FP has three timers; timer 1, timer 2 and timer 3.

A block diagram of timer 1 through 3 is shown in Figure 7.

The count source for timer 1 through 3 can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 6. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

The timer interrupt request bit which is in the interrupt control register 1 or timer control register (located at addresses $00FE_{16}$ and $00FF_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer 2 is controlled by bit 5 of the timer control register. If the bit 5 is "0", the timer starts counting, and the bit 5 is "1", the timer stops.

At a reset or stop mode, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3.

After a STP instruction is executed, timer 3, timer 2, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) must be set to "0".

For more details on the STP instruction, refer to the oscillation circuit section.

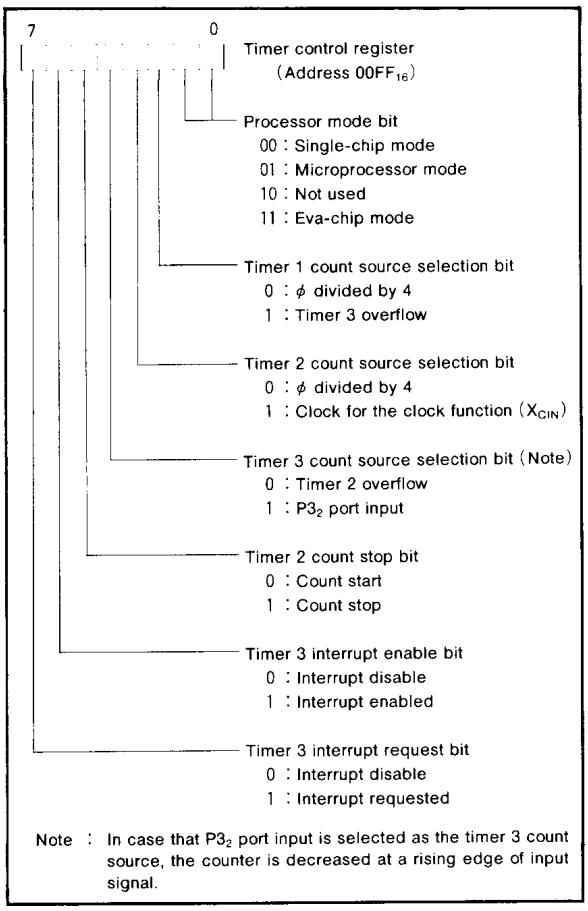


Fig. 6 Structure of timer control register

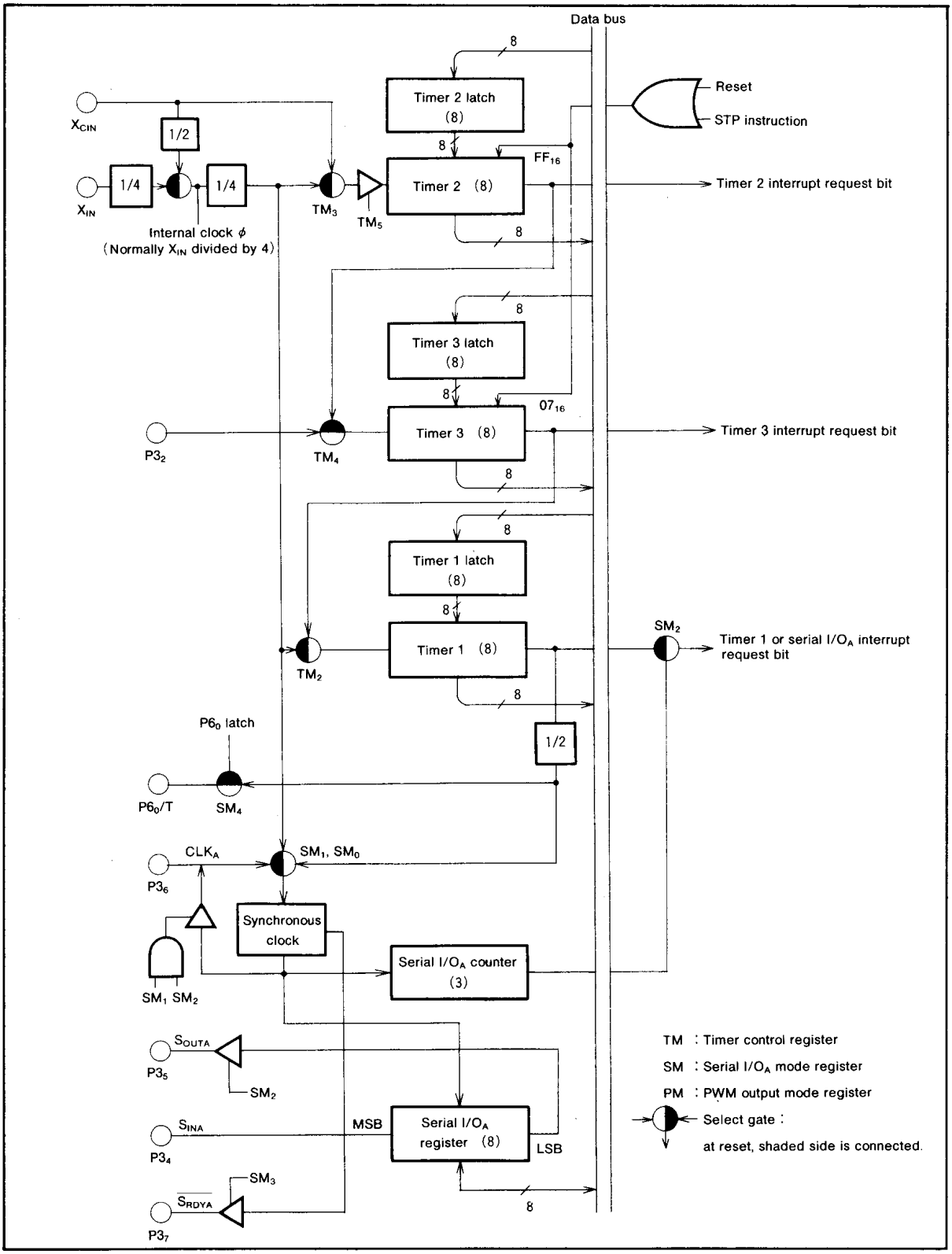


Fig. 7 Block diagram of timer 1 through 3

SERIAL I/O

M37100M8-XXXSP/FP has two serial I/O (serial I/O_A and serial I/O_B).

SERIAL I/O_A

The block diagram of serial I/O_A is shown in Figure 8. In the serial I/O_A mode the receive ready signal ($\overline{S_{RDYA}}$), synchronous input/output clock (CLK_A), and the serial I/O_A (S_{OUTA}, S_{INA}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O_A mode register (address $00F6_{16}$) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal divided by two from timer 1 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

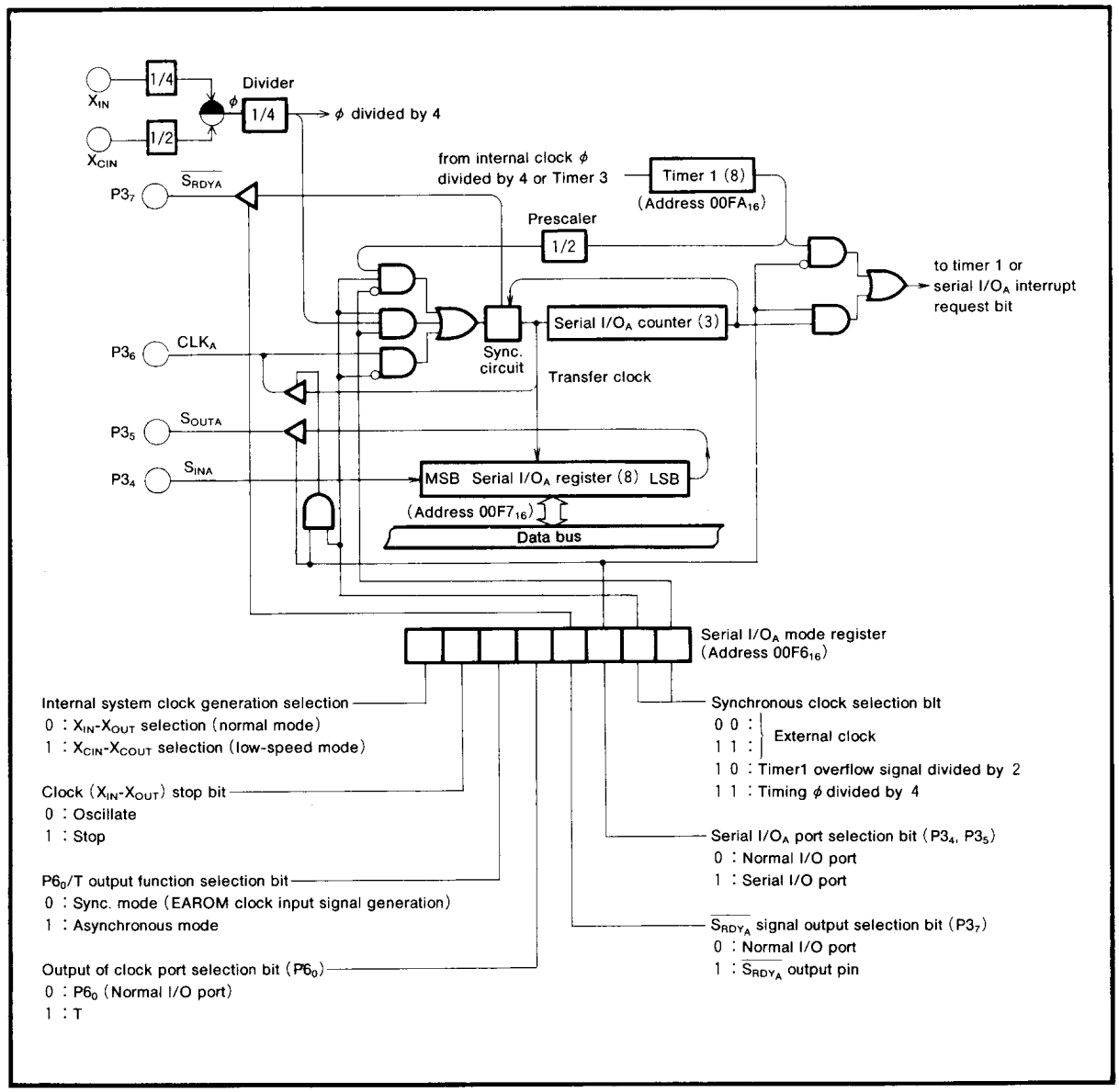


Fig. 8 Block diagram of serial I/O_A

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O_A or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal syncnronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output, and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O_A, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O_A counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDYA}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O_A differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDYA}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_A register. After the falling edge of write signal, the $\overline{S_{RDYA}}$ signal becomes low signaling that the M37100M8-XXXSP is ready to receive the external serial data. The $\overline{S_{RDYA}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_A counter is set to 7 when data is stored in the serial I/O_A register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O_A register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_A register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M37100M8-XXXSP's are shown in Figure 10.

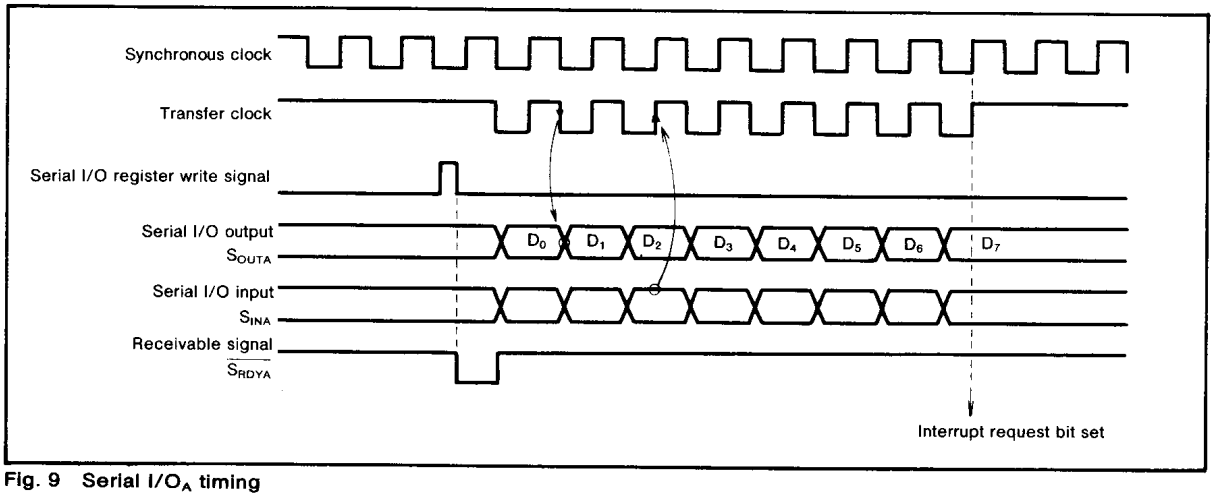


Fig. 9 Serial I/O_A timing

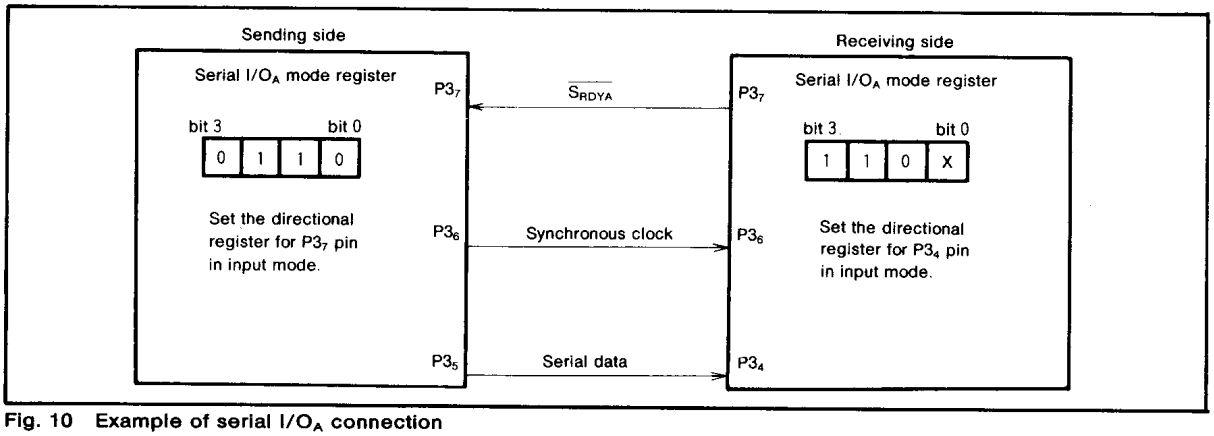


Fig. 10 Example of serial I/O_A connection

SERIAL I/O_B

The block diagram of serial I/O_B is shown in Figure 11. In the serial I/O_B mode the receive ready signal ($\overline{S_{RDYB}}$), synchronous input/output clock (CLK_B), and the serial I/O_B (S_{OUTB}, S_{INB}) pins are used as $P5_7$, $P5_6$, $P5_5$, and $P5_4$, respectively. The serial I/O_B mode register (address $00DA_{16}$) is an 8-bit register. Bit 1 of this register is used to select a synchronous clock source. When this bit is "0", an external clock from $P3_6$ is selected. When this bit is "1", the overflow signal divided by two from clock counter 0 becomes the synchronous clock.

Clock counter 0 is a 8-bit down counter to provide synchronous clock for serial I/O_B. This counter divides internal clock ϕ. Structure of clock counter 0 is the same of timers. Therefore, changing the timer period will change the transfer speed.

Bits 2 and 3 decide whether parts of P5 will be used as a serial I/O_B or not. When bit 2 is "1", $P5_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P5_6$. If the external synchronous clock is selected, the clock is input to $P5_6$. And $P5_5$ will be a serial output, and $P5_4$ will be a serial input. To use $P5_4$ as a serial input, set the directional register bit which corresponds to $P5_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O_B, bit 2 needs to be set to "1", if it is "0" $P5_6$ will function as a normal I/O. Bit 3 determines if $P5_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDYB}}$) or used as a normal I/O pin (bit 3="0"). Bit 4 is the special mode select bit. Serial I/O_B can be set to special mode by using this bit. Bits 0, 5, 6, and 7 are used for special mode. For details, see the section of special mode.

In the normal mode, operations of serial I/O_B are the same as that of serial I/O_A. For details, see the section of serial I/O_A.

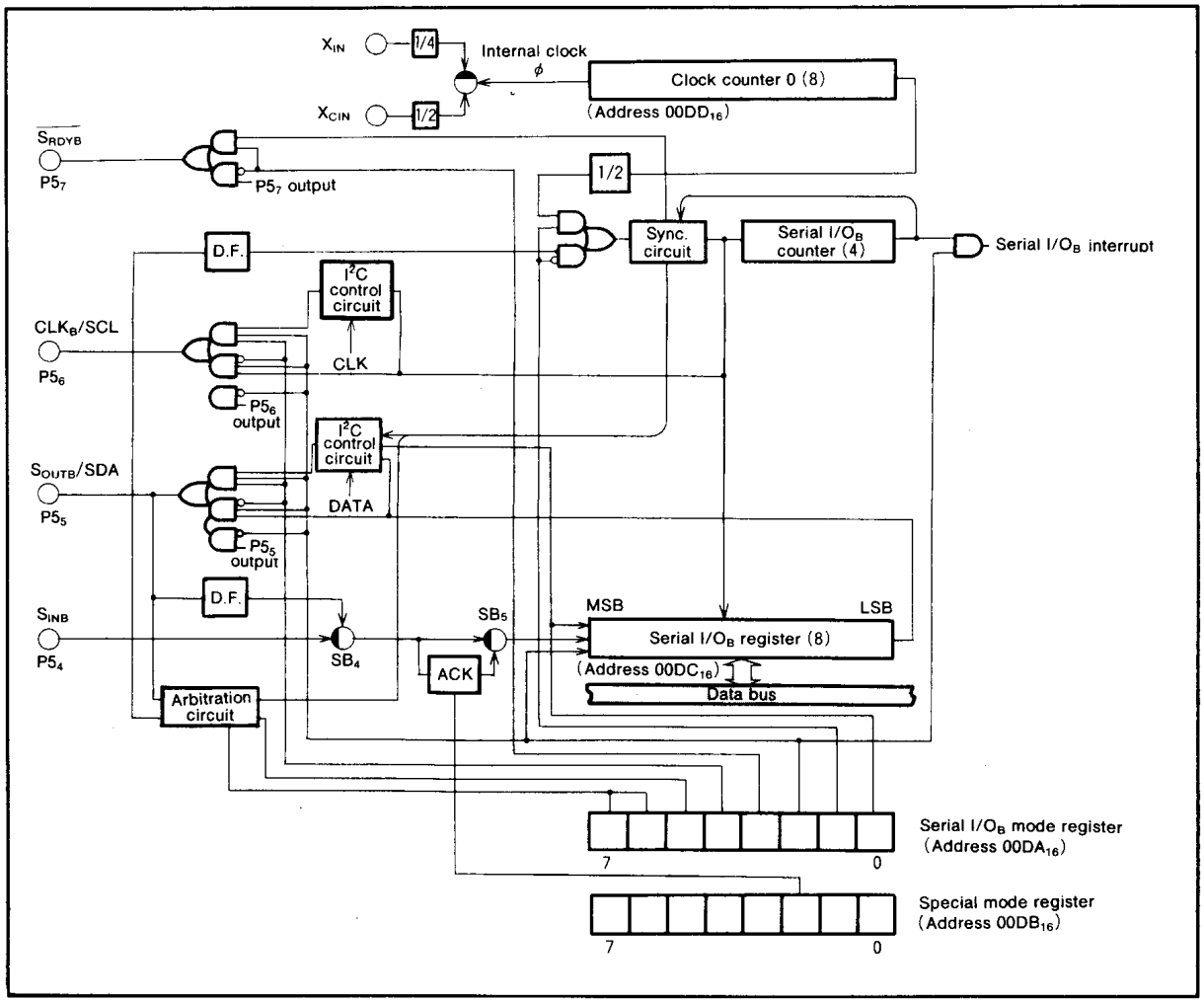


Fig. 11 Block diagram of serial I/O_B

SPECIAL MODE (I^2C BUS:INTER IC BUS*)

M37100M8-XXXSP/FP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (Inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37100M8-XXXSP/FP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 1 of interrupt control register 2 (address $00FB_{16}$) to "1" so as to serial I/O_B interrupt is selected. Then set bit 0 of interrupt control register 1 (address $00FE_{16}$) to "1" so as to serial I/O_B interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports $P5_5$ and $P5_6$. Set all bits (bits 5 and 6) corresponding to $P5_5$ and $P5_6$ of the port P5 register (address $00EC_{16}$) and the port P5 direction register (address $00ED_{16}$) to "1".

Set the transmission clock. The transmission clock uses the overflow signal divided by 2 from clock counter 0. Set appropriate value in clock counter 0. (For instance, if 4 is set in clock counter 0 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 100kHz).

Set contents of the special mode register (address $00DB_{16}$). (Usually, 03_{16}.) Set the bit 4 of serial I/O_B mode register (address $00DA_{16}$). Figure 14 shows the bit configurations of special mode register and serial I/O_B mode register.

Initial setting is completed by the above procedure.

Write data to be transmitted in the serial I/O_B register (address $00DC_{16}$).Immediately after this, clear bits 0 and 1 of special mode reigister (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 1 of the timer control register is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the serial I/O_B register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register to "0", set bit 1 clock SCL to 1, then set bit 1 data SDA to "1". This procedure transmits the stop signal.

Figure 12 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, setmaster reception ACK provided (36_{16}) in the serial I/O_B mode register (address $00DB_{16}$), and write "FF_{16}" in the serial I/O_B register (address $00DC_{16}$). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 13 shows master reception timing.

(3) Wait function

Wait function 1 is held SCL line up "L" level after falling of the 8th clock.

Wait function 2 is held SCL line up "L" level after falling of the 9th clock.

The wait function is reset by setting bit 5, 6 of the special mode register to "1".

*:Purchase of Mitsubishi Electric Corporation's I^2C components converys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

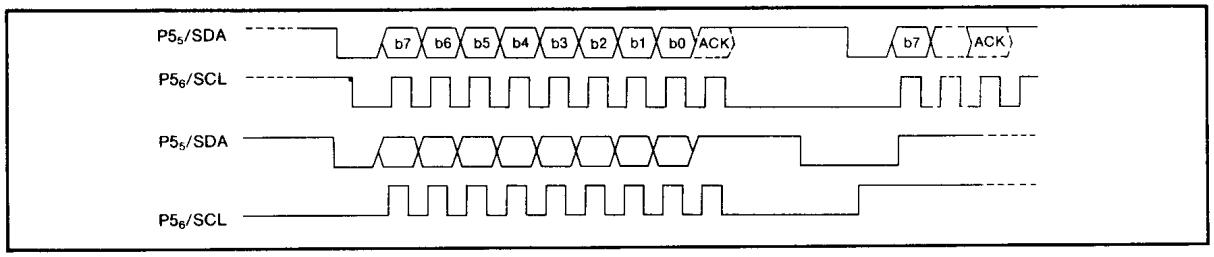


Fig. 12 Master transmission timing

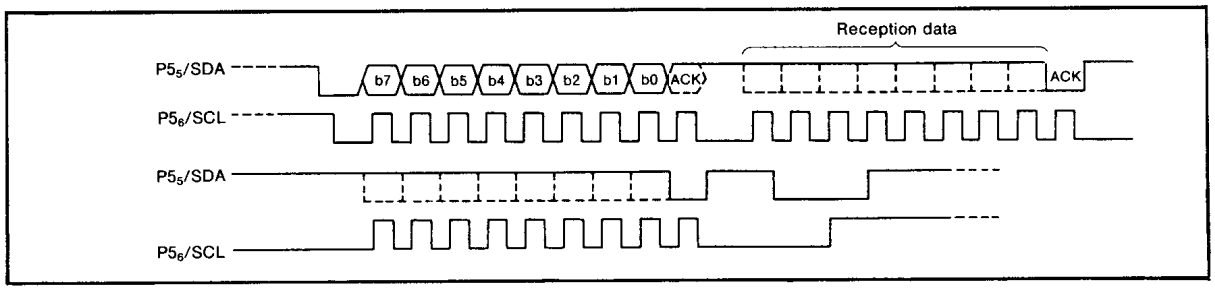


Fig. 13 Master reception timing

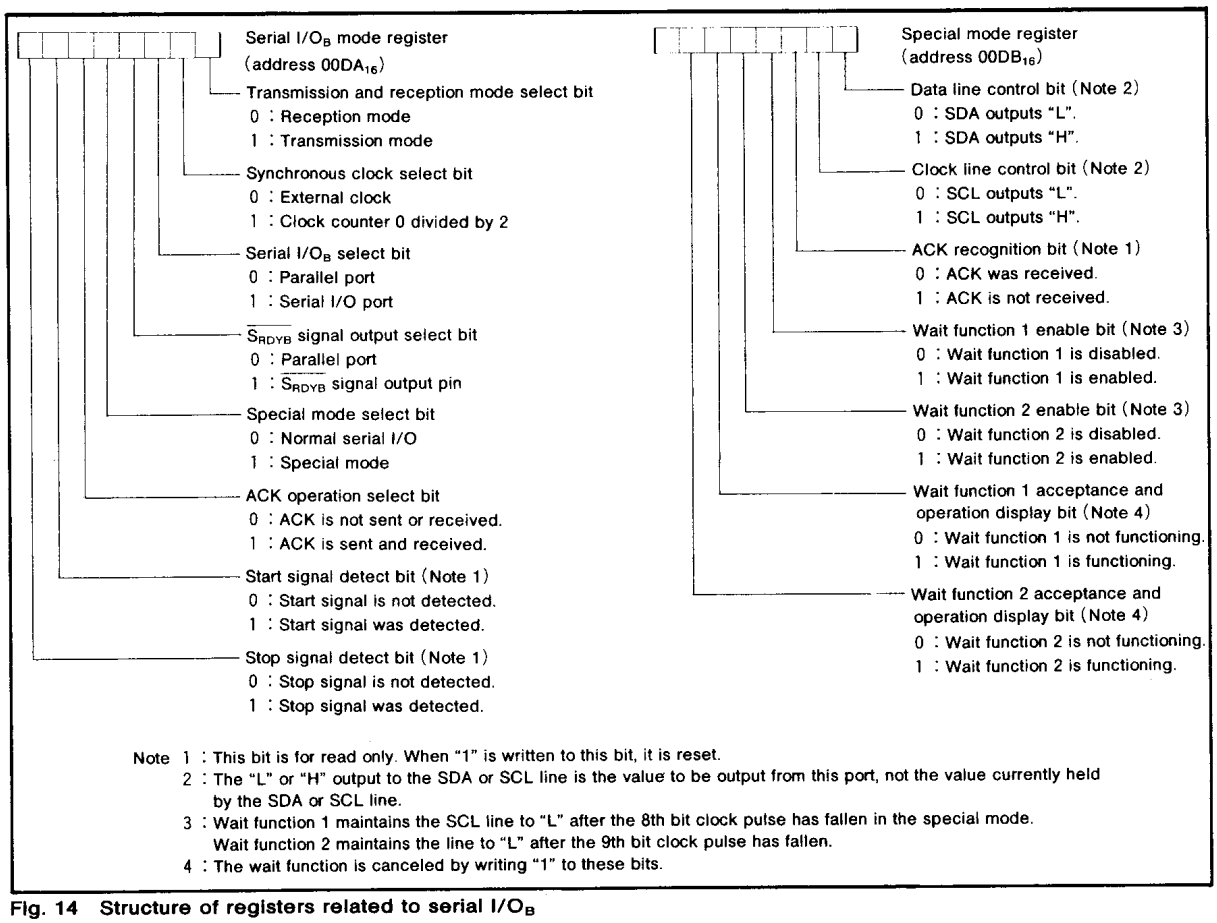


Fig. 14 Structure of registers related to serial I/O$_B$

PWM OUTPUT CIRCUIT

(1) Introduction

The M37100M8-XXXSP is equipped with one 14-bit PWM and four 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for X_{IN} = 4MHz) and a repeat period of 8192μs. PWM2, PWM3, PWM4 and PWM5 have a 6-bit resolution with minimum resolution bit width of 16μs and repeat period of 1024μs. Accuracy and operation range is certified of PWM are V_{CC} = 4.5 ~ 5.5V regardless of input frequency.

Block diagram of the PWM is shown in Figures 15.

The PWM timing generator section applies individual control signals to PWM 1~5, using clock input X_{IN} divided by 2 or X_{CIN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2, PWM3, PWM4 and PWM5 are in common with pins $P6_1$, $P6_2$, $P6_3$, $P6_4$ and $P6_5$ of port P6 (i.e. for PWM output, PWM output selection bits and the P6 directional register $D6_1$ ~ $D6_5$ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). When one of the PWM2~PWM5 is used for output, set the 6-bit in the PWM2~PWM5 register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$~$00F4_{16}$ and $00F8_{16}$ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2~PWM5) is shown in Figure 16. One period (T) is composed of 64 (2^6) segments.

There are six different pulse types configured from bits 0~5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 16 (a).

Six different pulses can be output from the PWM. Thesé can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 16 (b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 17. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N timers τ is output every short area of t=256 τ =128μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 17.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that puls τ. As a result, the short-area period t (=128μs, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data (LSB)	Area longer by τ than that of other t_m (m = 0 ~63)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 42, 50, 58
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ····· 57, 59, 61, 63

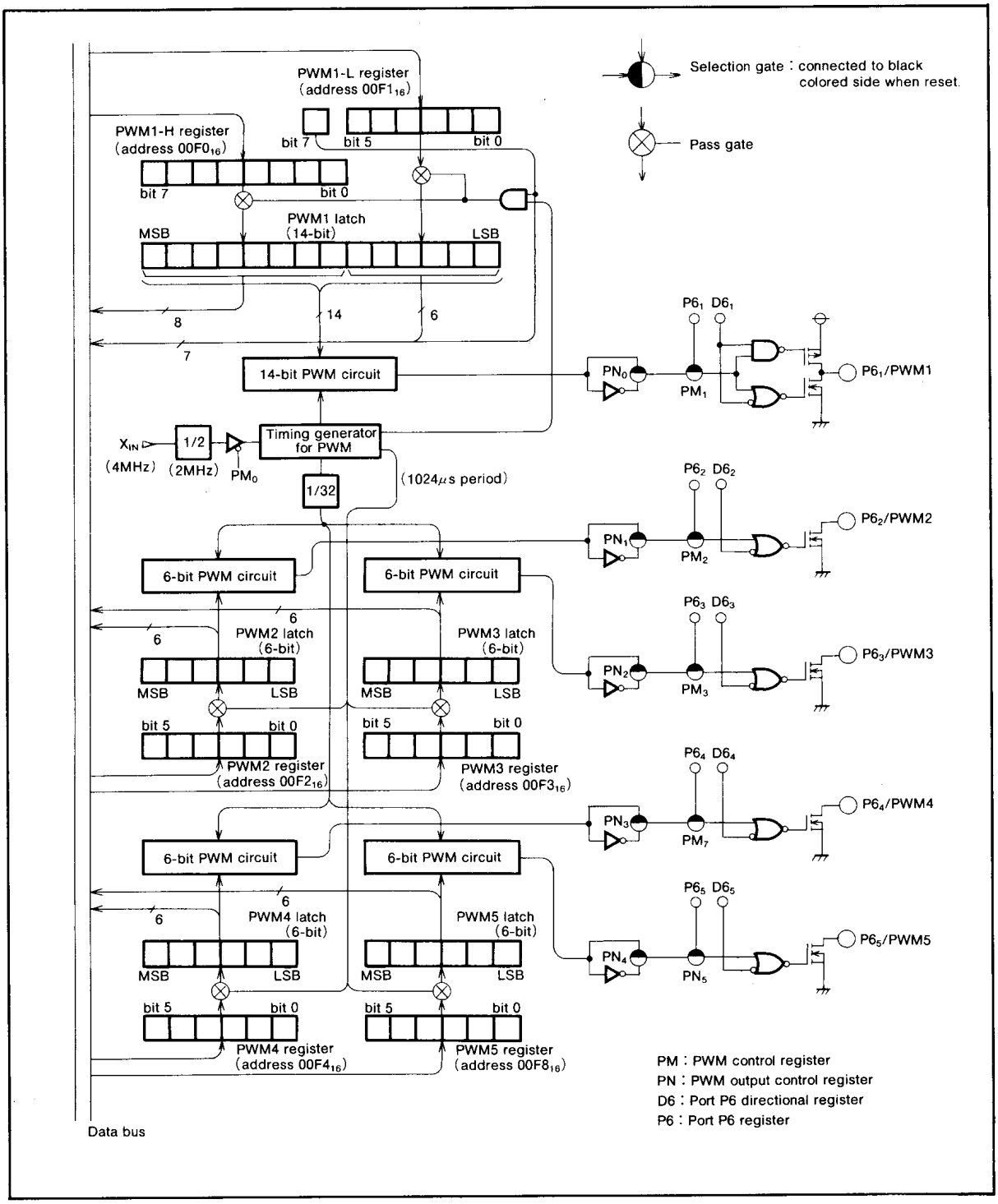


Fig. 15 Block diagram of the PWM circuit

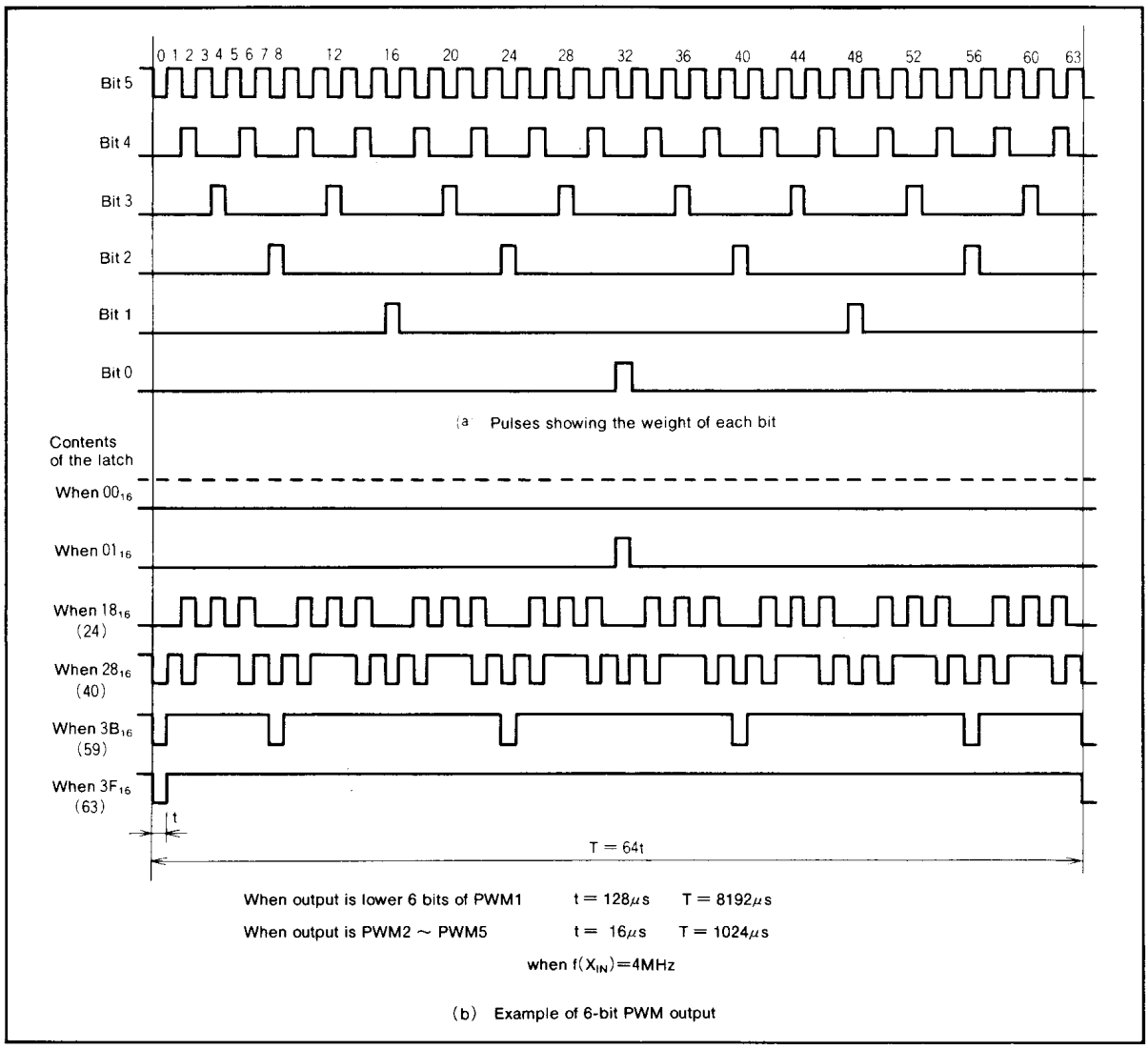


Fig. 16 6-bit PWM timing diagram

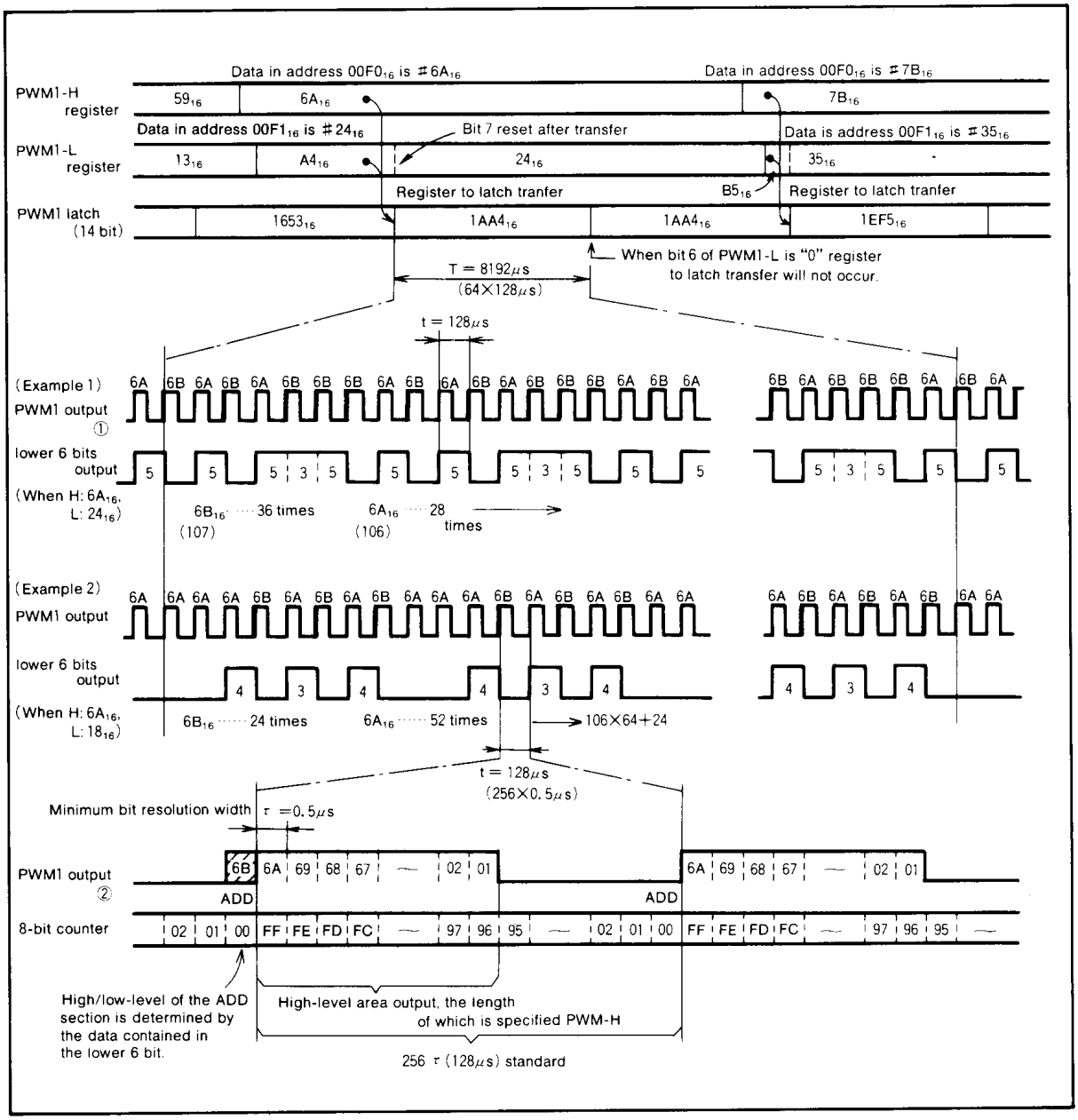


Fig. 17 14-bit PWM timing diagram

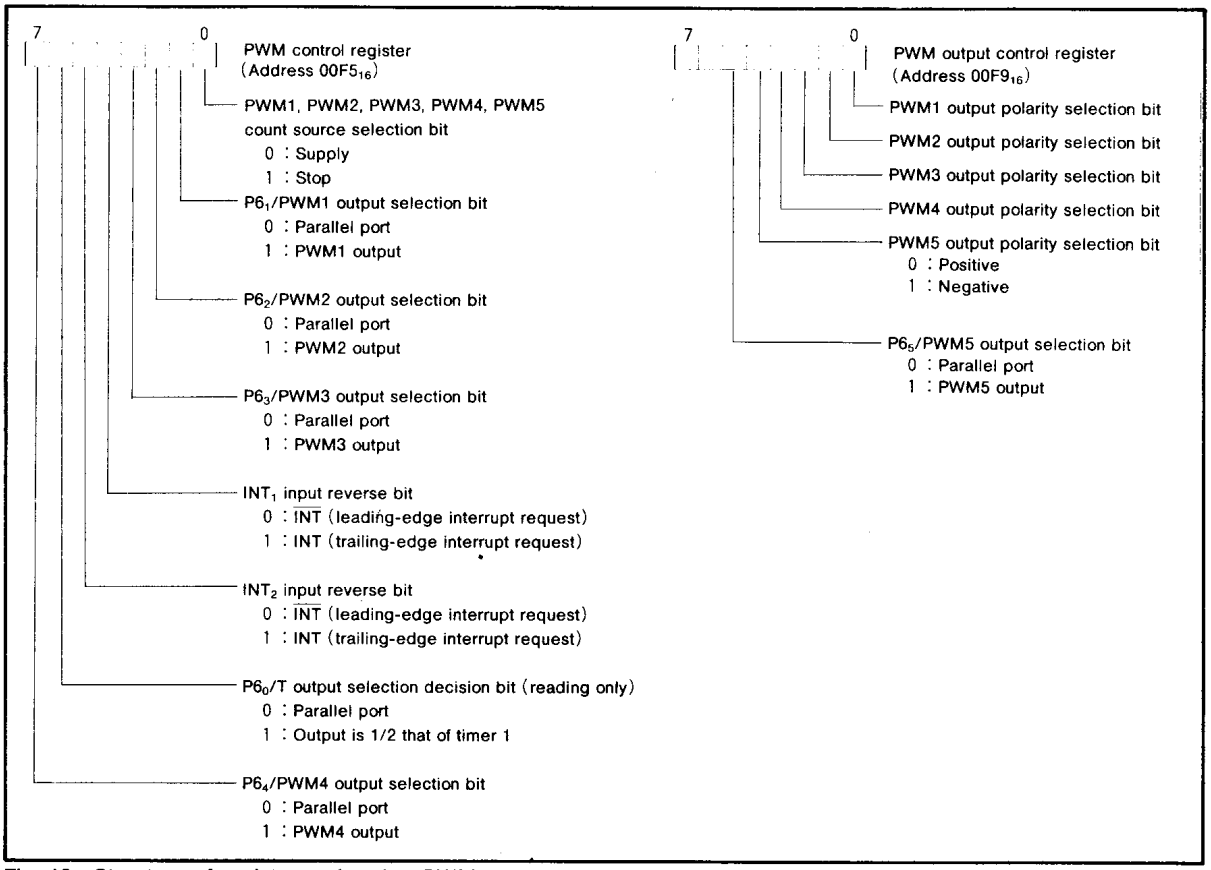


Fig. 18 Structure of registers related to PWM

PORT $P6_0$ / TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when bit 4 (SM_4) of the serial I/O_A mode register (address $00F6_{16}$) is set to "1". The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM_5) of the serial I/O_A mode register.

When SM_5 is set to "0" the synchronous mode is set. In such a case, after SM_4 has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 of the PWM control register.

From the time that the contents of SM_4 was changed to the point where switching completes, the contents of neither SM_4 nor $P6_0$ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during switching. Figure 19 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM_5 is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM_4 has been changed. Figure 19 (b) gives an example of timing in the asynchronous mode.

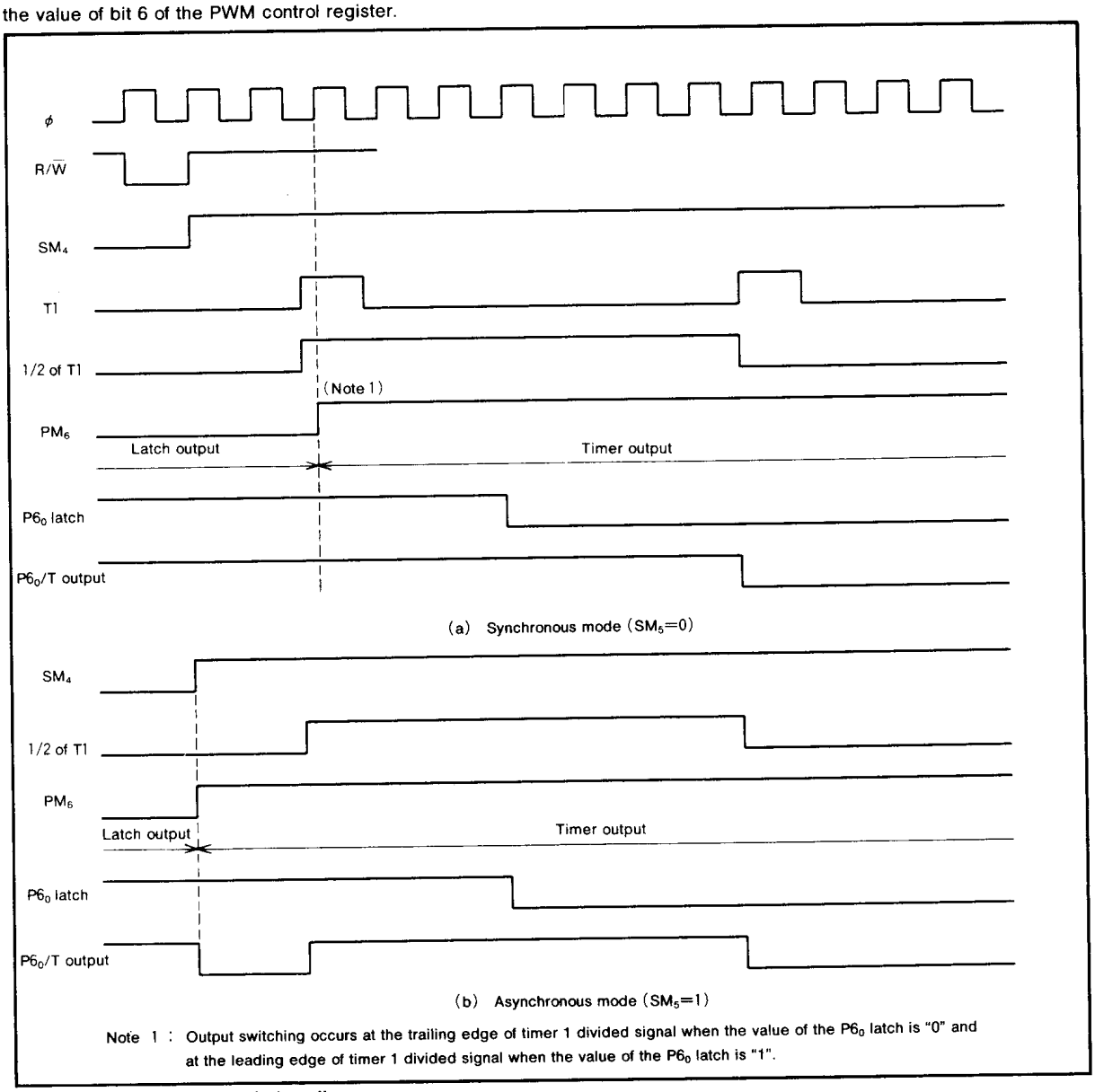


Fig. 19 $P6_0$/T switching timing diagram

COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 20. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, A-D control register (address $00E7_{16}$), and analog signal input pin ($P3_3$/A-D). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit A-D control register can generate $1/16V_{CC}$-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_3$ to "0" (port $P3_3$ enters the input mode), to allow port $P3_3$/A-D to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register (address $00E7_{16}$), bits 0 to 3. The voltage comparision starts as soon as the writing is completed. 4-cycle (required for comparating) later, the result of comparision is stored in the A-D control register, bit 4. Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the A-D control register becomes "1" regardless of the analog input voltage.

Table 3. Relationship between the contents of A-D control register and internal voltage

A-D control register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	$1/16V_{CC}-1/32V_{CC}$
0	0	1	0	$2/16V_{CC}-1/32V_{CC}$
0	0	1	1	$3/16V_{CC}-1/32V_{CC}$
0	1	0	0	$4/16V_{CC}-1/32V_{CC}$
0	1	0	1	$5/16V_{CC}-1/32V_{CC}$
0	1	1	0	$6/16V_{CC}-1/32V_{CC}$
0	1	1	1	$7/16V_{CC}-1/32V_{CC}$
1	0	0	0	$8/16V_{CC}-1/32V_{CC}$
1	0	0	1	$9/16V_{CC}-1/32V_{CC}$
1	0	1	0	$10/16V_{CC}-1/32V_{CC}$
1	0	1	1	$11/16V_{CC}-1/32V_{CC}$
1	1	0	0	$12/16V_{CC}-1/32V_{CC}$
1	1	0	1	$13/16V_{CC}-1/32V_{CC}$
1	1	1	0	$14/16V_{CC}-1/32V_{CC}$
1	1	1	1	$15/16V_{CC}-1/32V_{CC}$

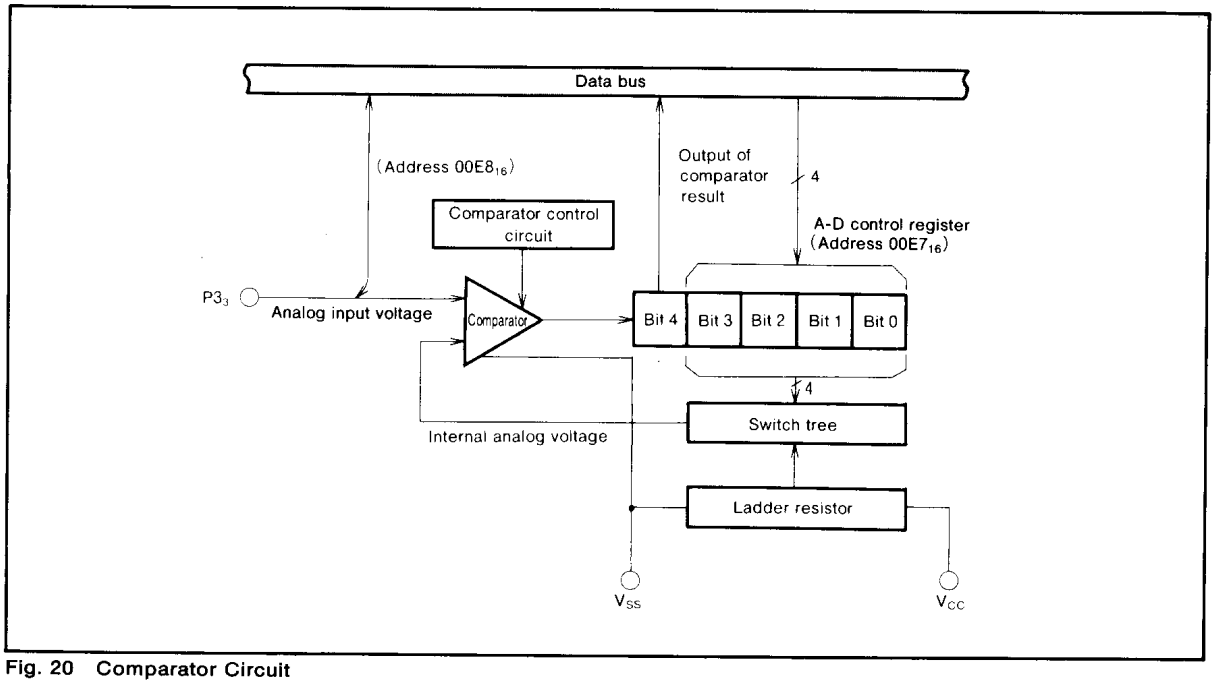


Fig. 20 Comparator Circuit

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions. The M37100M8-XXXSP incorporates a 21 columns × 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 96 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12×16 dot configuration to obtain smooth character patterns. (See Figure 21)

The following shows the procedure how to display characters on the CRT screen.

① Set the character to be displayed in display RAM.
② Set the display color by using the color register.
③ Specify the color register in which the display color is set by using the display RAM.
④ Specify the vertical position and character size by using the vertical position register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 23 shows a block diagram of the CRT display control circuit. Figure 22 shows the structure of the CRT display control register.

Table 4. Outline of CRT display functions

Parameter		Functions
Number of display character		21characters× 3 lines
Character configuration		12×16 dots (See Figure 21)
Kinds of character		96
Character size		4 size selectable
Color	Kinds of color	15(max.)
	Coloring unit	a character
Display expansion		Possible (multiple lines)

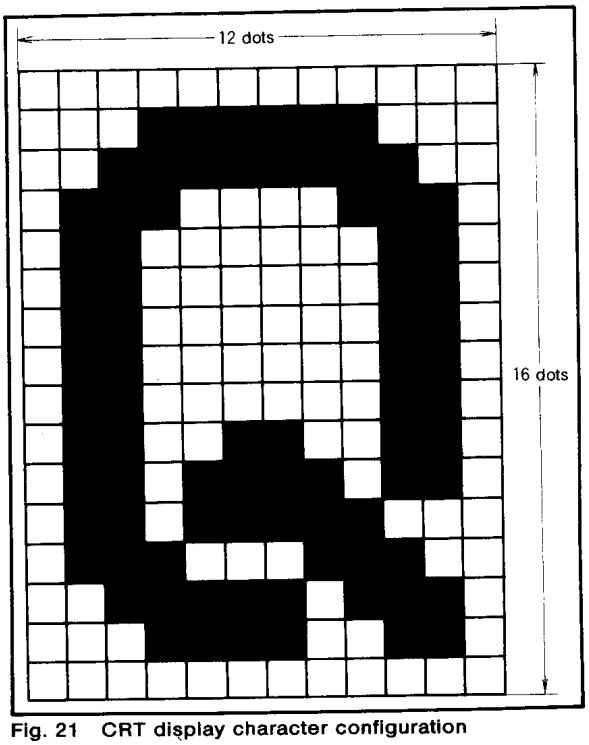


Fig. 21 CRT display character configuration

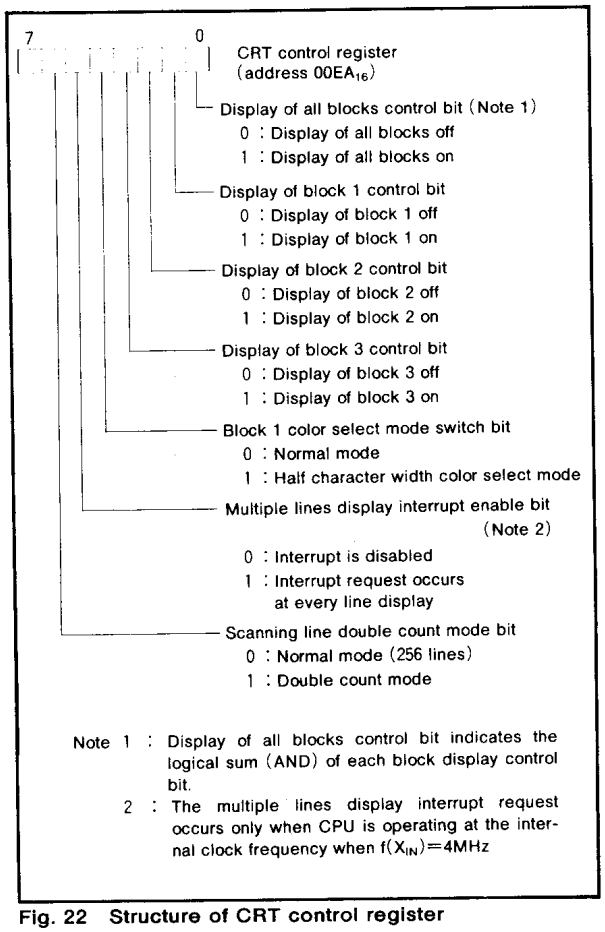


Fig. 22 Structure of CRT control register

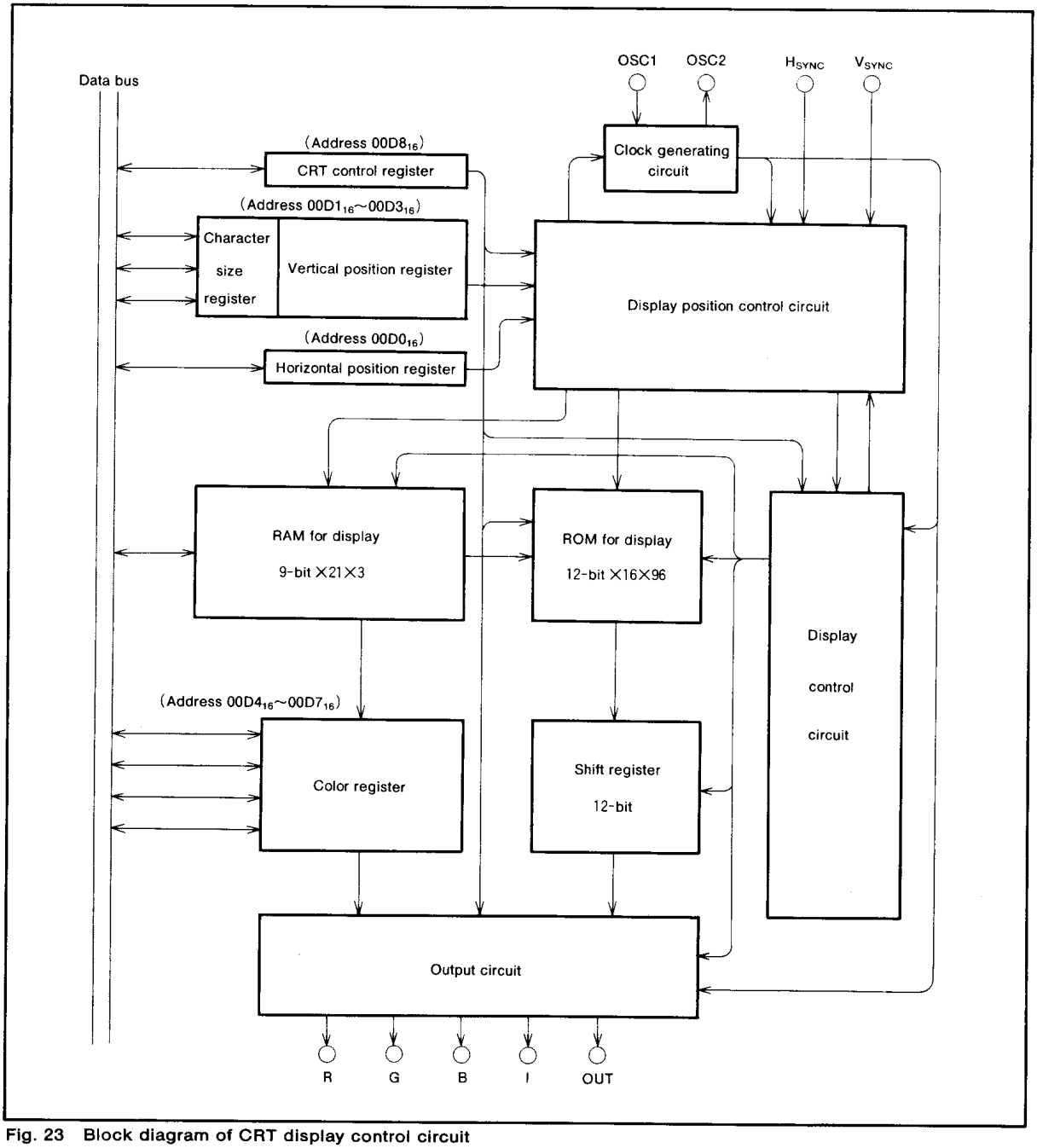


Fig. 23 Block diagram of CRT display control circuit

(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 21 characters can be displayed in one block. (See (4) RAM for Display.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc =oscillation cycle for display).

The display position in the vertical direction is selected from 64-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 26), a block of the smaller block No. (1~3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 26), the former block is overridden and the latter is displayed.

The vertical position can be specified from 64-step positions (four scanning lines per step) for each block by setting values 00_{16}~$3F_{16}$ to bits 0~5 in the vertical position register (addresses $00D1_{16}$~$00D3_{16}$). Figure 24 shows the structure of the vertical position register.

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc=oscillation cycle for display)) by setting values 00_{16}~$3F_{16}$ to bits 0~5 in the horizontal position register (address $00D0_{16}$).

Figure 25 shows the structure of the horizontal position register.

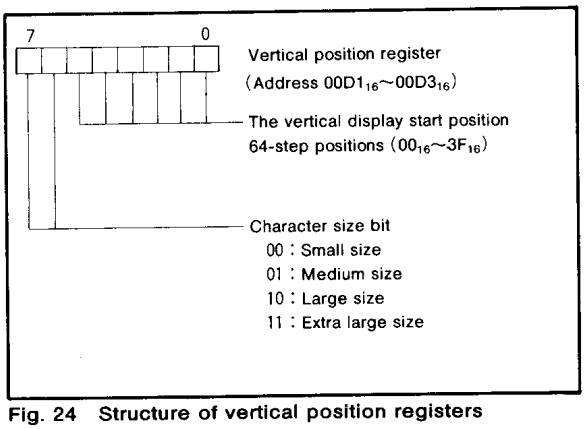


Fig. 24 Structure of vertical position registers

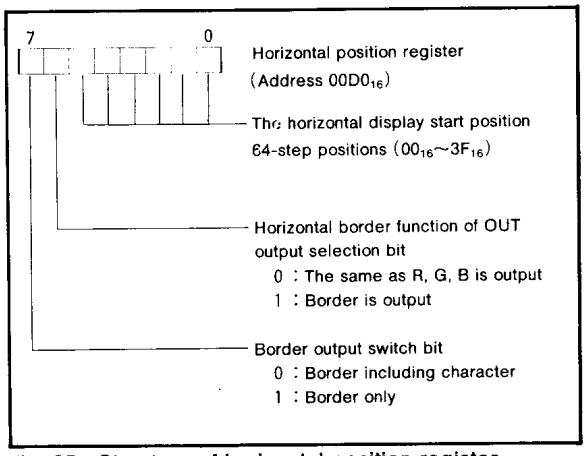
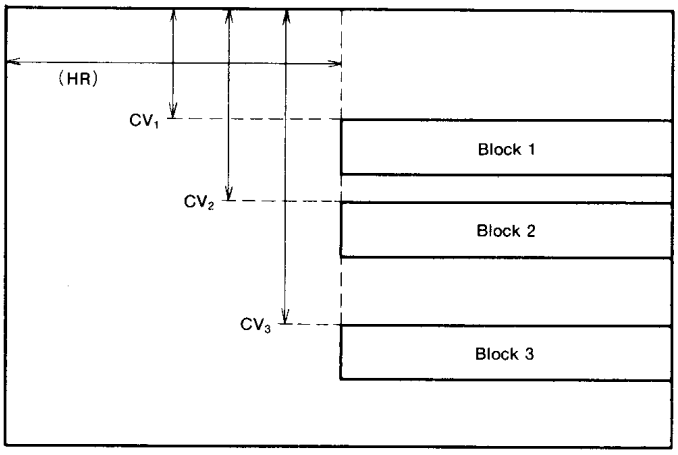
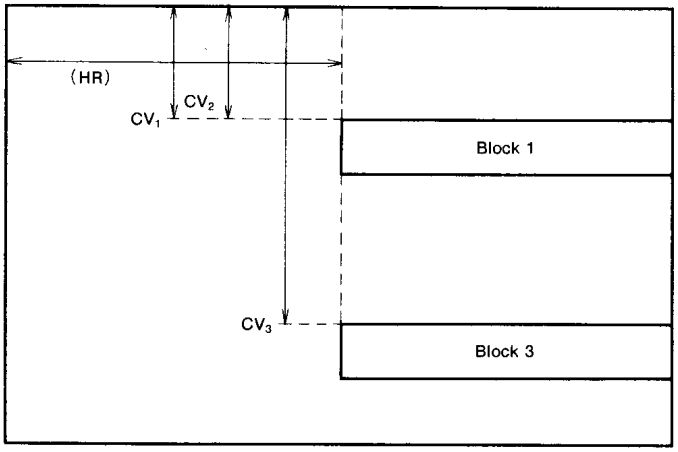


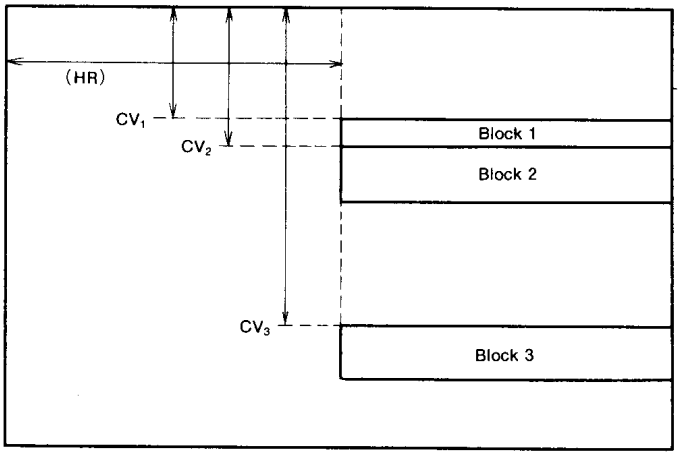
Fig. 25 Structure of horizontal position register



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed.

Fig. 26 Display position

(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the bit 6 and 7 of vertical position register to set a character size.

The character size can be selected from four sizes: minimum size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=Tc) in the width (horizontal) direction. The minimum size consists of [one scanning line] × [1 Tc]; the medium size consists of [two scanning lines] × [2 Tc]; the large size consists of [three scanning lines] × [3 Tc]; and the extra large size consists of [four scanning lines] × [4 Tc]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

Table 5. The relationship between the set values of the character size bits and the character sizes

Set values of the character size bits		Character size	Width (horizontal) direction	Height (vertical) direction
Bit 7	Bit 6			
0	0	Small	1 T_C	1
0	1	Medium	2 T_C	2
1	0	Large	3 T_C	3
1	1	Extra large	4 T_C	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block. (See Figure 27)

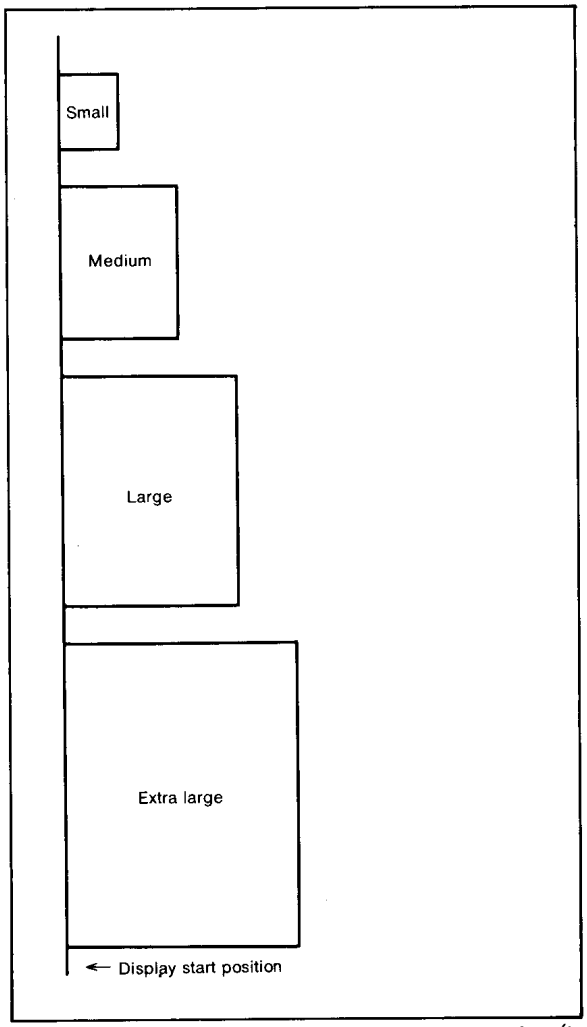


Fig. 27 Display start position of each character size (horizontal direction)

(4) RAM for Display

The CRT display RAM is allocated at addresses 2000_{16}～$20D4_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 6 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0～6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16}. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.

The structure of the CRT display RAM is shown in Figure 28.

Table 6. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1 st Column	2000_{16}	2080_{16}
	2 nd Column	2001_{16}	2081_{16}
	3 rd Column : 19th Column	2002_{16} : 2012_{16}	2082_{16} : 2092_{16}
	20th Column	2013_{16}	2093_{16}
	21th Column	2014_{16}	2094_{16}
Not used		2015_{16} ≀ $201F_{16}$	2095_{16} ≀ $209F_{16}$
Block 2	1 st Column	2020_{16}	$20A0_{16}$
	2 nd Column	2021_{16}	$20A1_{16}$
	3 rd Column : 19th Column	2022_{16} : 2032_{16}	$20A2_{16}$: $20B2_{16}$
	20th Column	2033_{16}	$20B3_{16}$
	21th Column	2034_{16}	$20B4_{16}$
Not used		2035_{16} ≀ $203F_{16}$	$20B5_{16}$ ≀ $20BF_{16}$
Block 3	1 st Column	2040_{16}	$20C0_{16}$
	2 nd Column	2041_{16}	$20C1_{16}$
	3 rd Column : 19th Column	2042_{16} : 2052_{16}	$20C2_{16}$: $20D2_{16}$
	20th Column	2053_{16}	$20D3_{16}$
	21th Column	2054_{16}	$20D4_{16}$
Not used		2055_{16} ≀ $207F_{16}$	

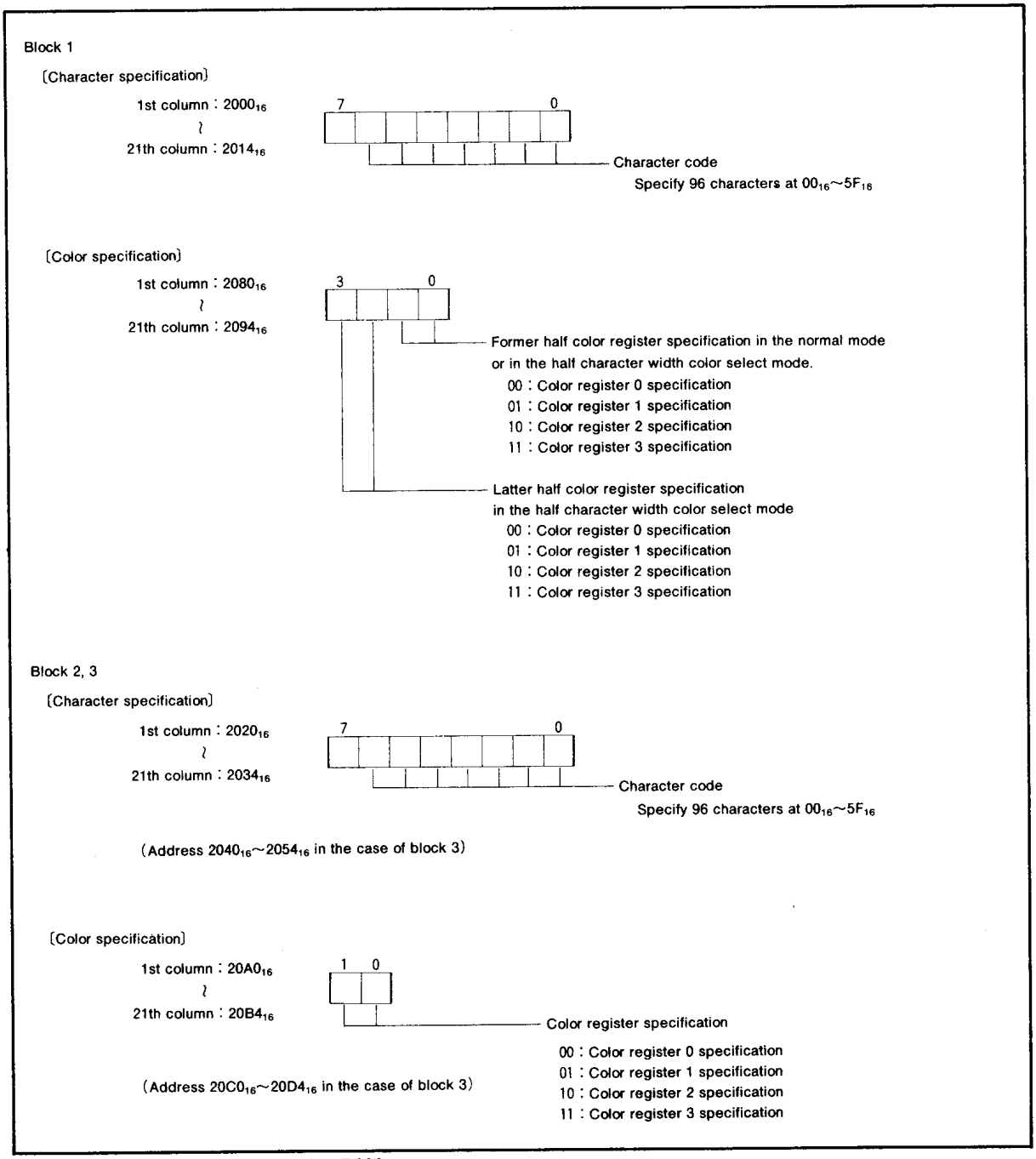


Fig. 28 Structure of the CRT display RAM

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0~CO3: addresses $00D4_{16}$~$00D7_{16}$) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0~3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 29 shows the structure of the color register.

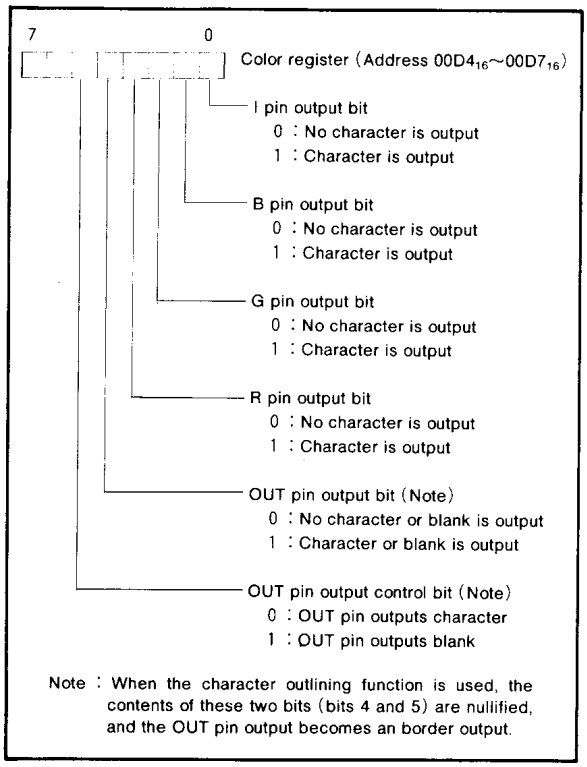


Fig. 29 Structure of color registers

(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address $00D8_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080_{16}~2094_{16}).

② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080_{16}~2094_{16}).

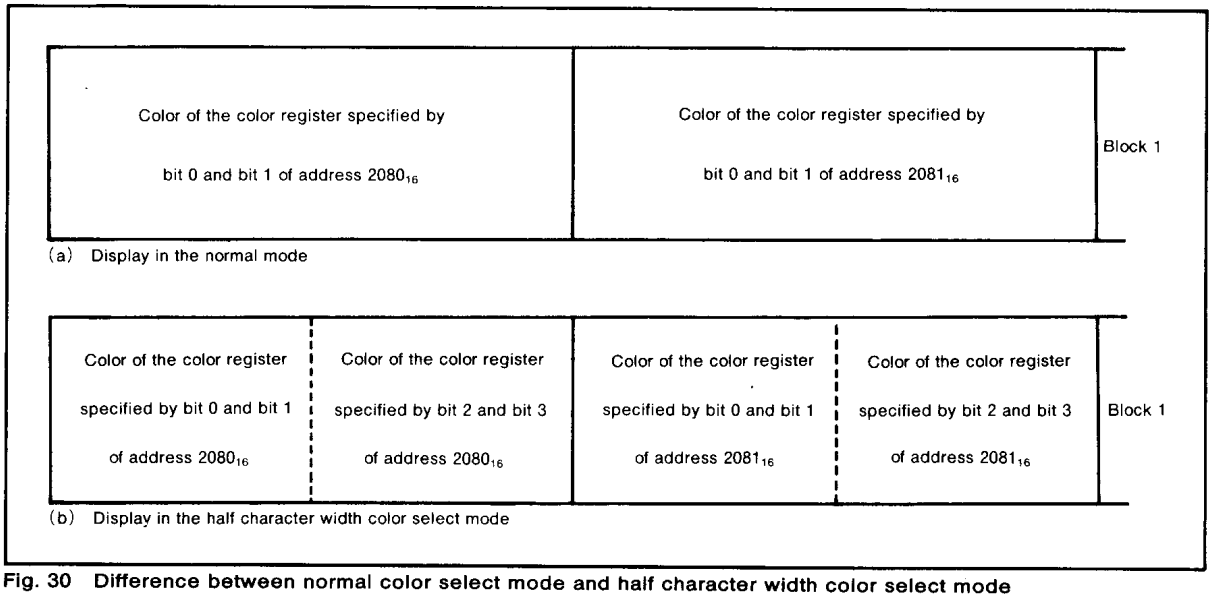


Fig. 30 Difference between normal color select mode and half character width color select mode

(7) Multiline Display

The M37100M8-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

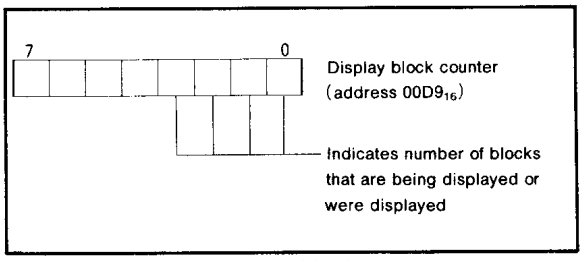


Fig. 31 Structure of display block counter

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 6 at address 00FE$_{16}$) to "1"), then execute the following processing in the CRT interrupt handling routine.

① Read the value of the display block counter.

② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.

③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 31 shows the structure of the display block counter.

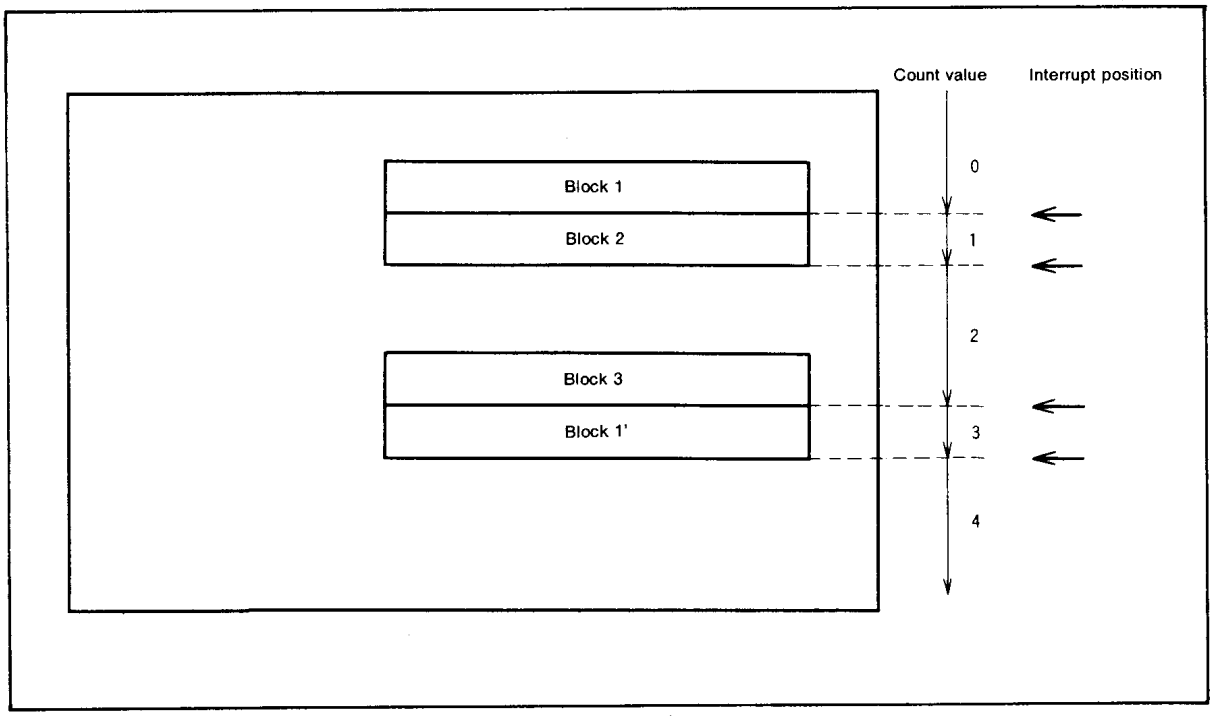


Fig. 32 Timing of CRT interrupt and count value of display block counter

(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 64 steps from 00_{16} to $3F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 32 from 00_{16} to $1F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 20_{16} to $3F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00D8_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

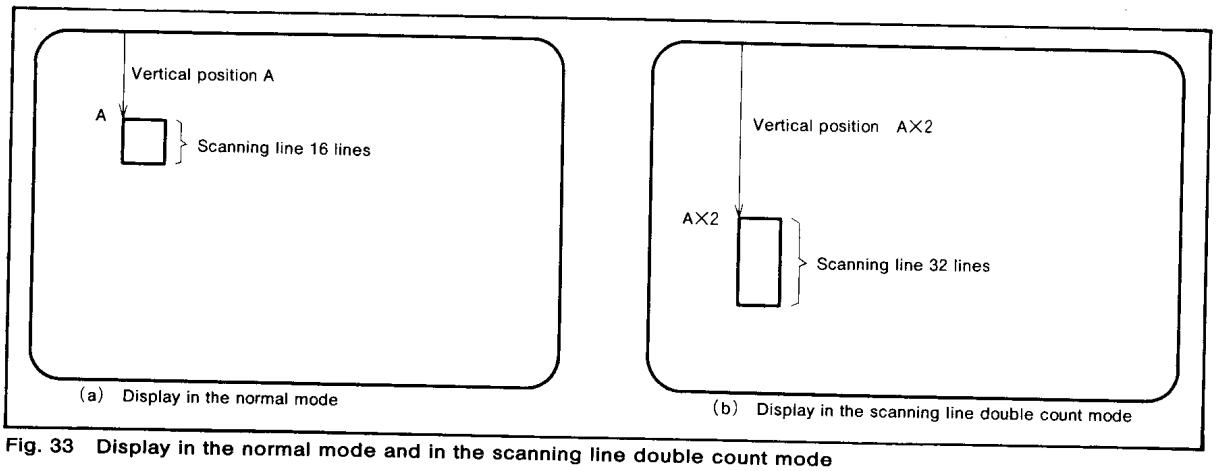


Fig. 33 Display in the normal mode and in the scanning line double count mode

(9) Horizontal Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed only horizontal direction.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the bit 6 and 7 of horizontal position register. Table 7 shows the relationship between the values set in the horizontal position register and the character border function.

Table 7. The relationship between the value set in the horizontal position register and the character border function

Horizontal position register		Functions	Example of output
Bit 7	Bit 6		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

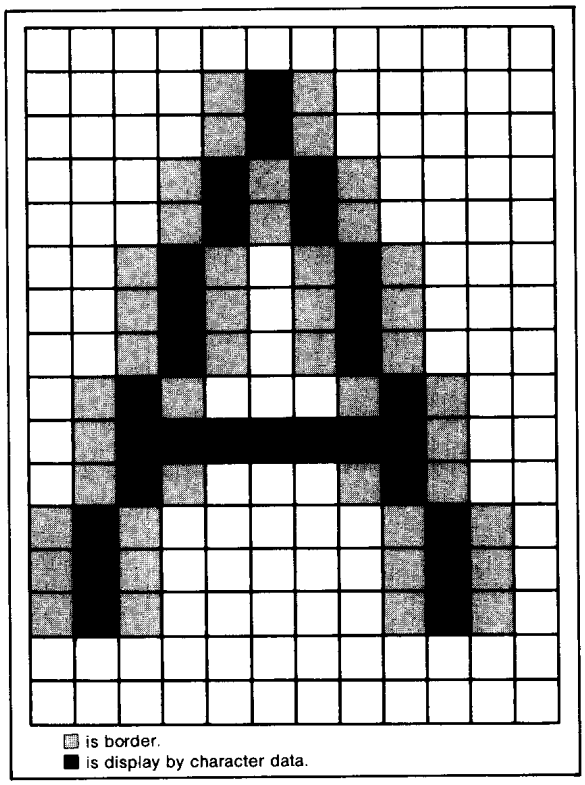


Fig. 34 Example of border

(10) Clock Oscillating Circuit for Display

The clock signal for display can be obtained by connecting a resistor and a capacitor between the I/O ports of the oscillating circuit (OSC1 and OSC2). Figure 35 shows an example of circuit.

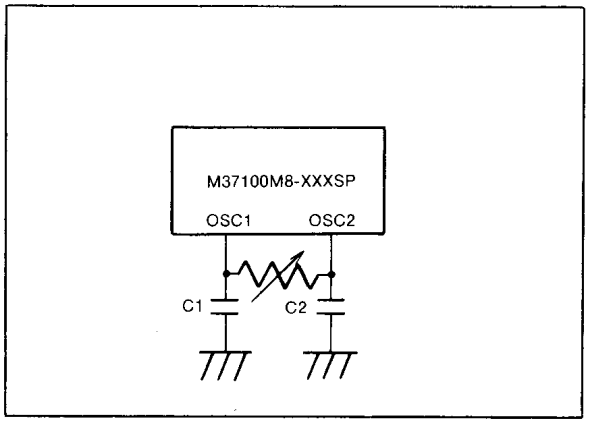


Fig. 35 Example of oscillating circuit for display

(11) Programming Notes

1. Use STA instruciton for data transfer to the following registers related to OSD functions.
   ① Horizontal position register (address $00D0_{16}$)
   ② Vertical position registers (address $00D1_{16}$~$00D3_{16}$)
   ③ Color registers (address $00D4_{16}$~$00D7_{16}$)
   ④ CRT control register (address $00D8_{16}$)
2. Do not display the display OFF blocks having different character sizes on a block display
3. The highest vertical position (the vertical display start position bits are "00_{16}") can not be used.
4. The interrupt to tell the end of block display is not caused and the display block counter is not incremented until the display of the block has been completed terminated.
5. The display block counter ($00D9_{16}$) is reset while V_{SYNC} is "H" (when the option is positive in polarity) to "FF_{16}".
6. If, during the display of a block, the display position of another block comes, the display of the subsequent block (having a larger vertical position register value) is preferred.
7. When two or more blocks are displayed in the same vertical position, the display priority is CV1, CV2, and CV3 in this order. This is not affected by turning on/off of block display.

RESET CIRCUIT

The M37100 is reset according to the sequence shown in Figure 37. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V$\pm$10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 36.

	Address	
(1) Port P0 directional register	(D0)(E1$_{16}$) ···	00$_{16}$
(2) Port P1 directional register	(D1)(E3$_{16}$) ···	00$_{16}$
(3) Port P2 directional register	(D2)(E5$_{16}$) ···	00$_{16}$
(4) Port P3 directional register	(D3)(E9$_{16}$) ···	00$_{16}$
(5) Port P4 directional register	(D4)(EB$_{16}$) ···	0
(6) Port P5 directional register	(D5)(ED$_{16}$) ···	0 0 0 0 0 0 0
(7) Port P6 directional register	(D6)(EF$_{16}$) ···	0 0 0 0 0 0 0
(8) PWM control register	(PM)(F5$_{16}$) ···	00$_{16}$
(9) Serial I/O$_A$ mode register	(SM)(F6$_{16}$) ···	00$_{16}$
(10) PWM output control register	(PN)(F9$_{16}$) ···	0 0 0 0 0 0
(11) Interrupt control register 2	(IN)(FB$_{16}$) ···	0 0
(12) Timer 2	(T2)(FC$_{16}$) ···	FF$_{16}$
(13) Timer 3	(T3)(FD$_{16}$) ···	07$_{16}$
(14) Interrupt control register 1	(IM)(FE$_{16}$) ···	00$_{16}$
(15) Timer control register	(TM)(FF$_{16}$) ···	00$_{16}$
(16) Processor status register	(PS) ···	1
(17) Program counter	(PC$_H$) ···	Contents of address FFFF$_{16}$
	(PC$_L$) ···	Contents of address FFFE$_{16}$
(18) Horizontal location register	(HR)(D0$_{16}$) ···	00$_{16}$
(19) Color register 0	(CO0)(D4$_{16}$) ···	0 0 0 0 0 0
(20) Color register 1	(CO1)(D5$_{16}$) ···	0 0 0 0 0 0
(21) Color register 2	(CO2)(D6$_{16}$) ···	0 0 0 0 0 0
(22) Color register 3	(CO3)(D7$_{16}$) ···	0 0 0 0 0 0
(23) Display control register	(CC)(D8$_{16}$) ···	0 0 0 0 0 0 0
(24) Serial I/O$_B$ mode register	(SB)(DA$_{16}$) ···	00$_{16}$
(25) Special mode register	(SC)(DB$_{16}$) ···	0 0 0 0 0 0 0
(26) Counter 0	(DD$_{16}$) ···	FF$_{16}$

Note. Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values.

Fig. 36 Internal state of microcomputer at reset

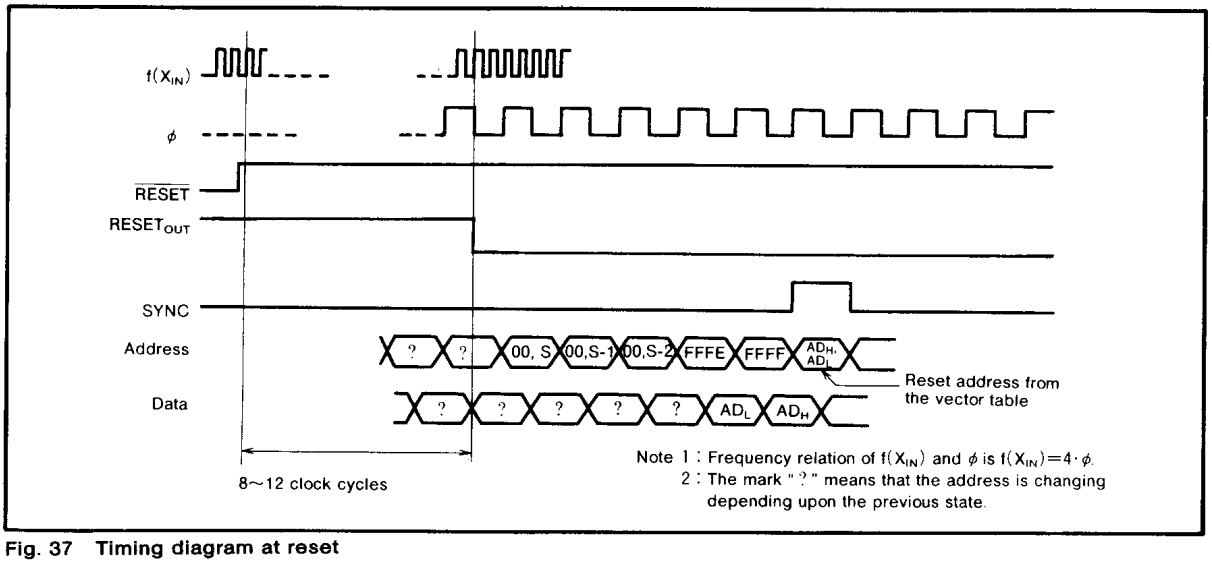


Fig. 37 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain and middle voltage output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00E0_{16}$.

Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address $00FF_{16}$), three different modes can be selected; single-chip mode, eva-chip mode and microprocessor mode.

In these modes it functions as address ($A_7 \sim A_0$) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0 but the output structure is not middle voltage. It can be built in pull-up register at each pin by selecting the option. In other modes, it functions as address ($A_{15} \sim A_8$) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P1. In other modes, it functions as data ($D_0 \sim D_7$) input/output port.

Refer to the section on processor modes for details.

(4) Port P3

In single-chip mode, port P3 has the same function as port P1. $P3_2 \sim P3_7$ have program selectable dual functions. $P3_0$, $P3_1$ function as control signals input/output port except in the single-chip mode. Refer to the section on processor modes for details.

(5) Port P4

This is an 1-bit I/O port with function similar to port P0, but the output structure is CMOS output.

This port is unaffected by the processor mode bits.

(6) Port P5

This is an 7-bit I/O port with function similar to port P1. $P5_4 \sim P5_7$ have program selectable dual functions. $P5_2$, $P5_3$ are shared with external interrupt input pins (INT_1, INT_2).

This port is unaffected by the processor mode bits.

(7) Port P6

This is an 6-bit input/output port with function similar to port P0. The output structure of $P6_0$, $P6_1$ is CMOS output and the output structure of $P6_2 \sim P6_5$ is N-channel open drain and middle voltage.

$P6_0 \sim P6_5$ have program selectable dual functions.

This port is unaffected by the processor mode bits.

(8) Function pins for CRT display function

The horizontal synchronizing signal is input from H_{SYNC}.

The vertical synchronizing signal is input from V_{SYNC}.

I, B, G, R, OUT are output pins for CRT display.

Refer to the section on CRT display functions for details.

(9) ϕ pin.

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) can be output from this pin by selecting the option.

At low-speed mode, X_{CIN} divided by 2 is output from this pin.

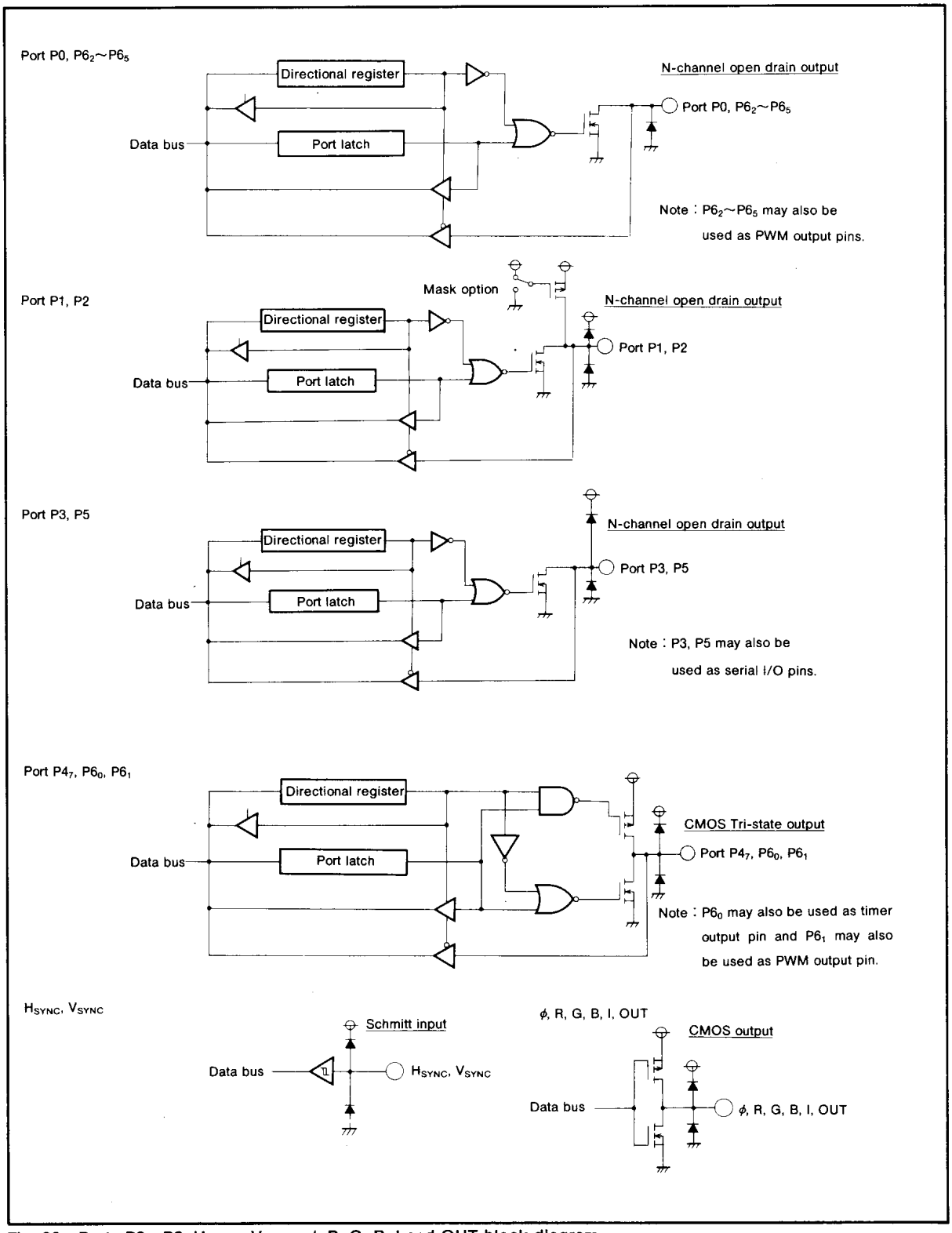


Fig. 38 Ports P0~P6, H_{SYNC}, V_{SYNC}, φ, R, G, B, I and OUT block diagram

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), three different operation modes can be selected; single-chip mode, microprocessor mode and evaluation chip (eva-chip) mode. In the microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 40 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 39.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The three different modes are explained as follows:

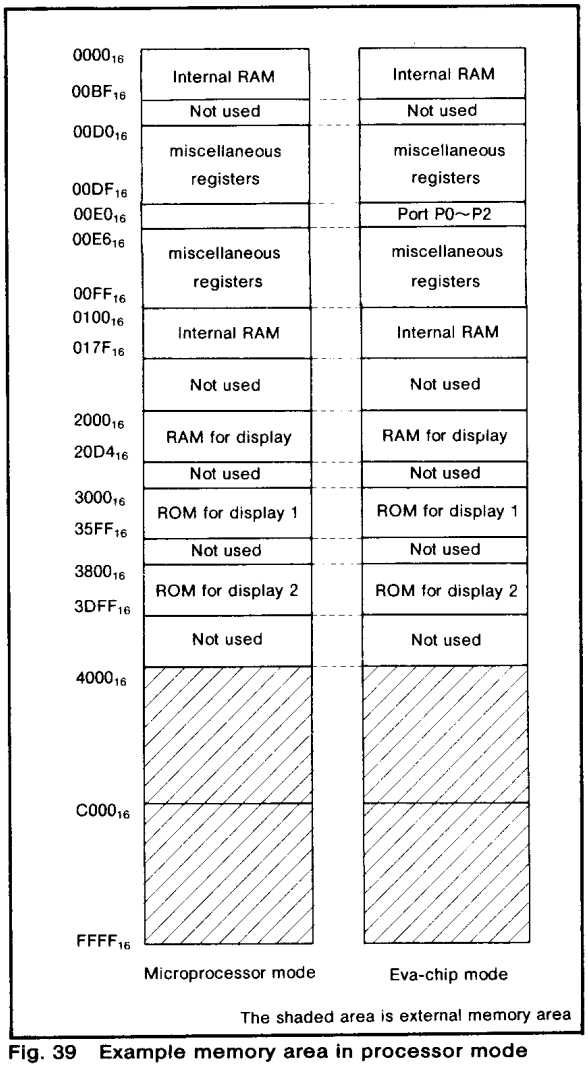


Fig. 39 Example memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Microprocessor mode [01]

The microcomputer will be placed in the microprocessor mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01".

In this mode, the internal ROM is inhibited so the external memory is required.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal output functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(3) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode.

In this mode, the internal ROM is inhibited so the external memory is required.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original output functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original output functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 8.

Note : The standards of M37100M8-XXXSP/FP is assured only in single-chip mode. Use in the microprocessor mode or the eva-chip mode only at program development.

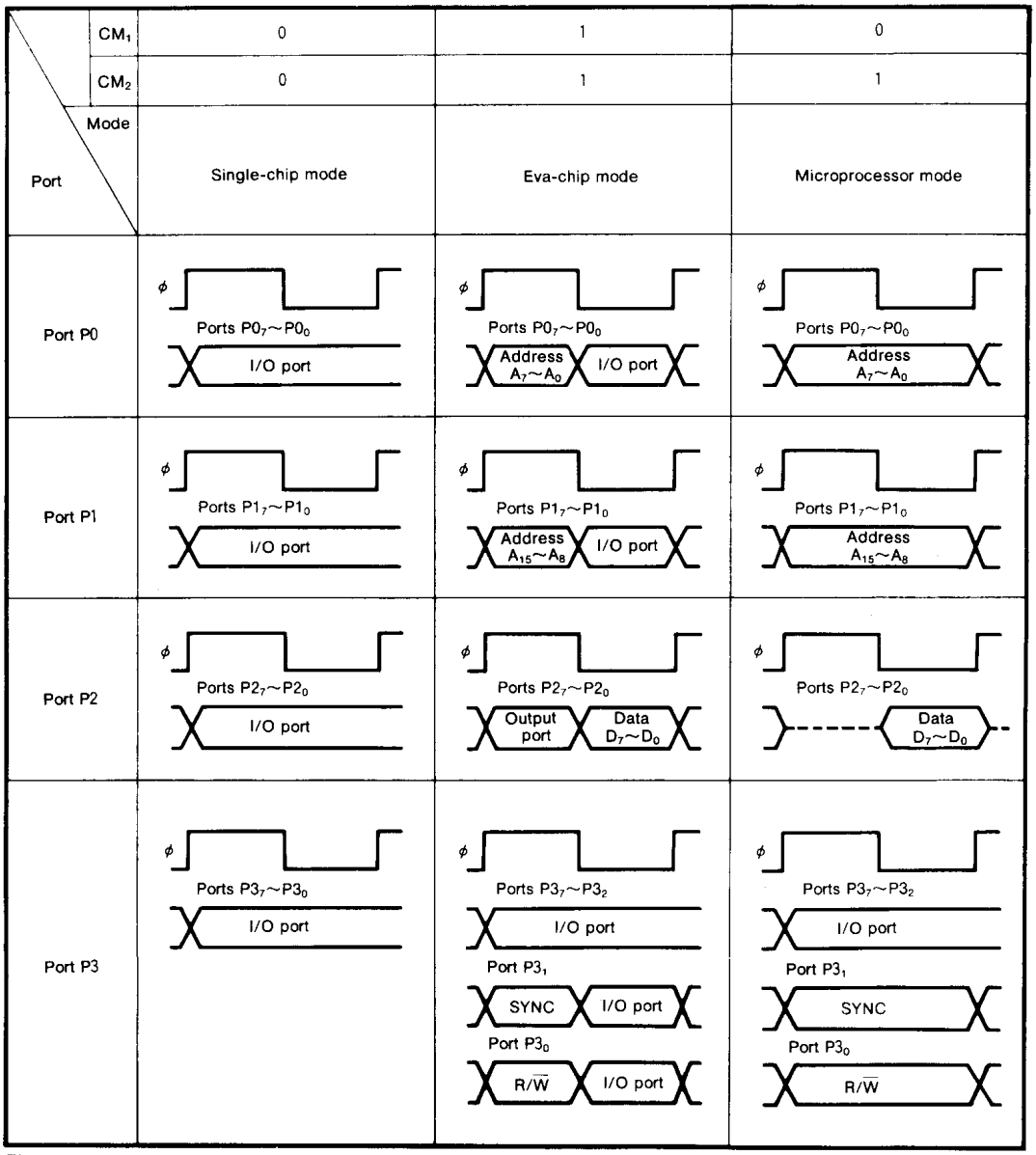


Fig. 40 Processor mode and functions of ports P0~P3

Table 8. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M37100M8-XXXSP has two internal clock generating circuits. Figure 42 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O_A mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 41 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator.

The M37100M8-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/8$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0").

Oscillation is restarted (release the stop mode) when INT_1, INT_2, or serial I/O_A or serial I/O_B interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt or canceling a reset, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($60\mu A$ or less at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O_A mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 43 shows the transition of states for the system clock.

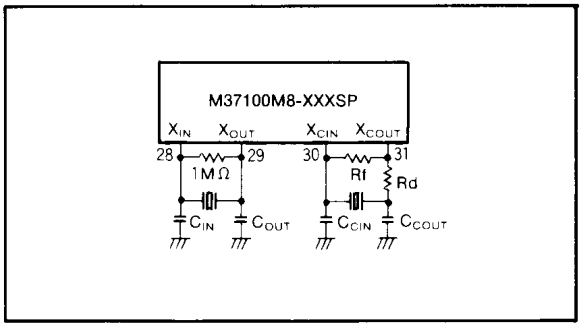


Fig. 41 Example ceramic resonator circuit

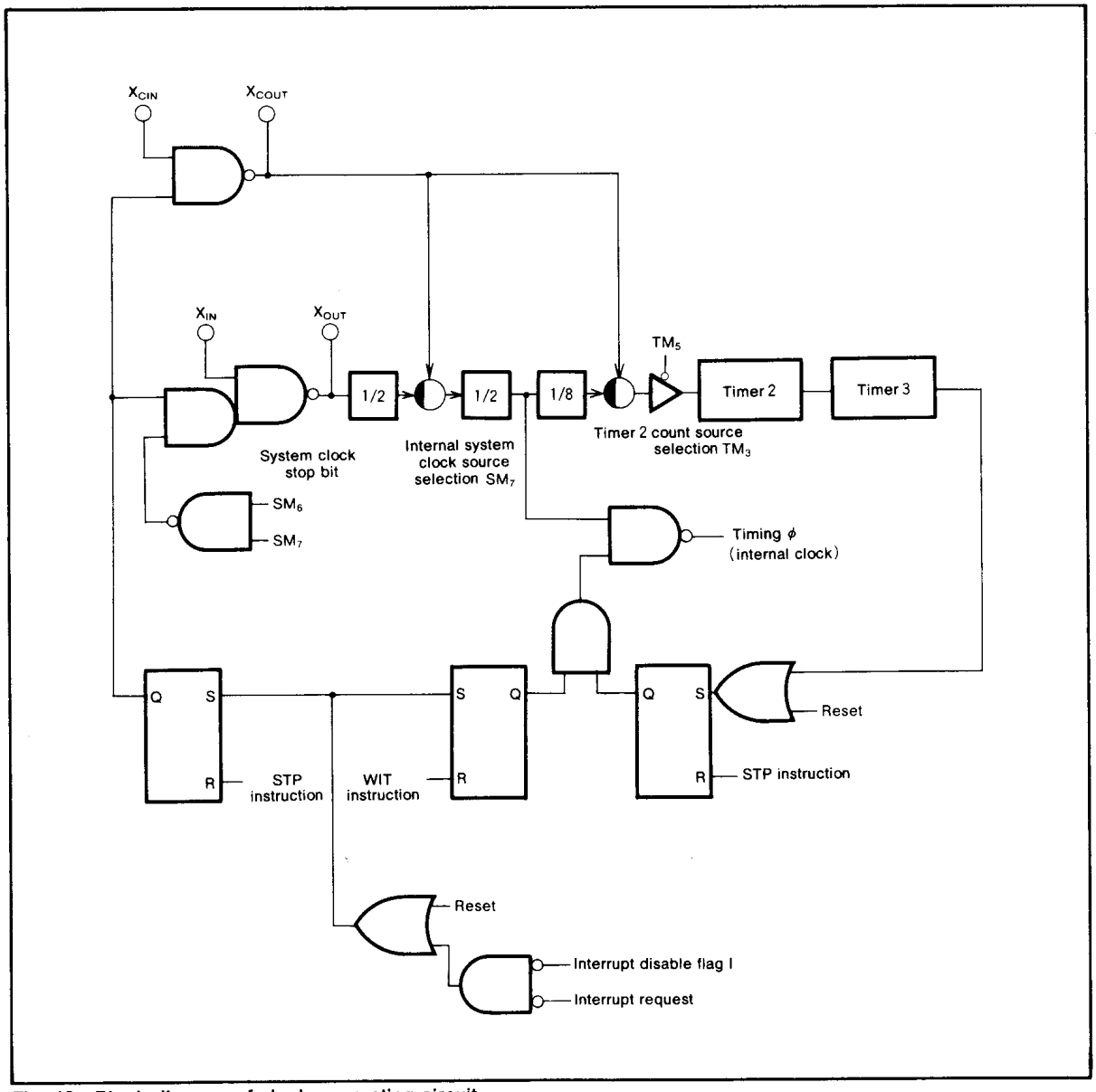
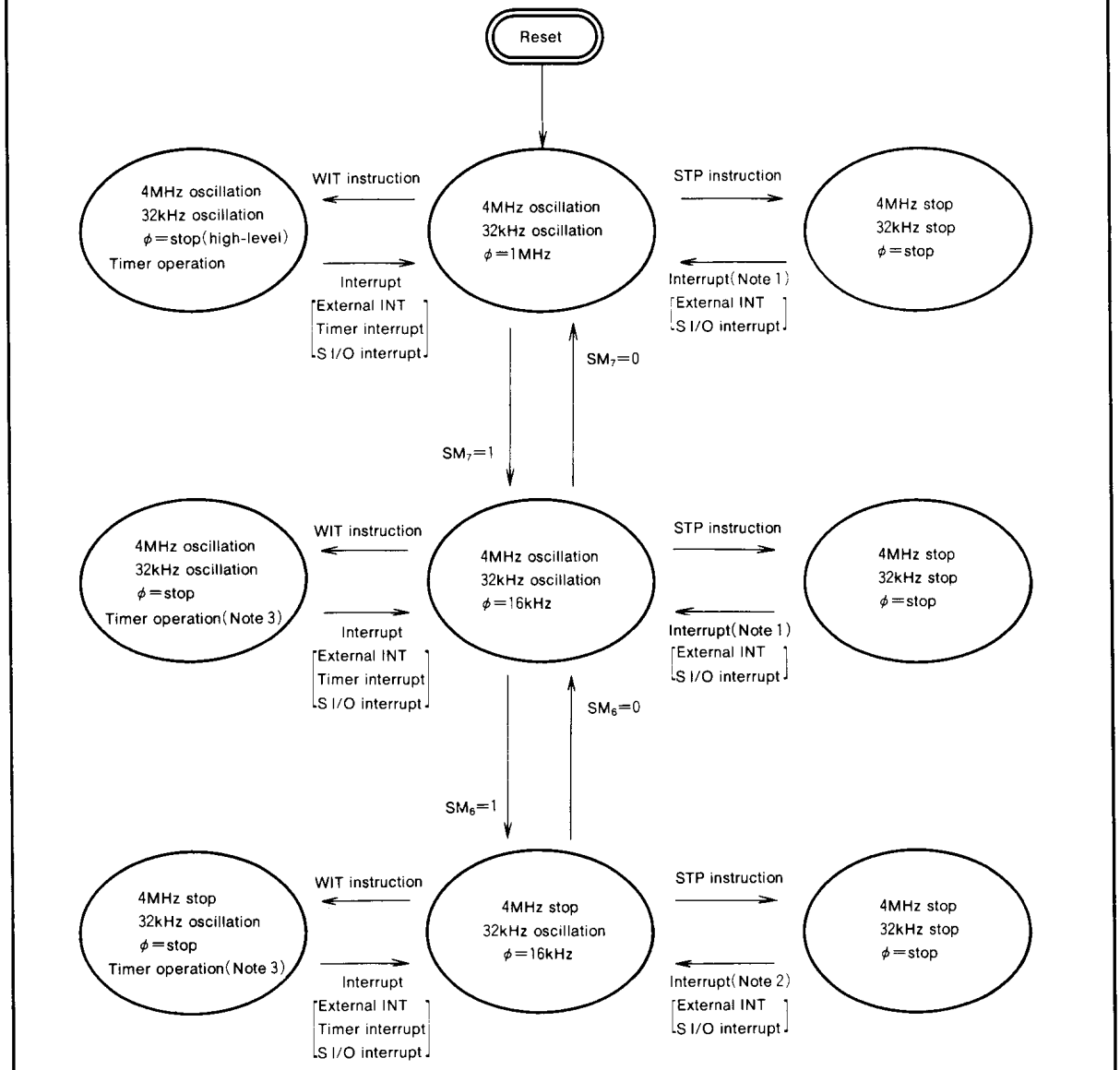


Fig. 42 Block diagram of clock generating circuit

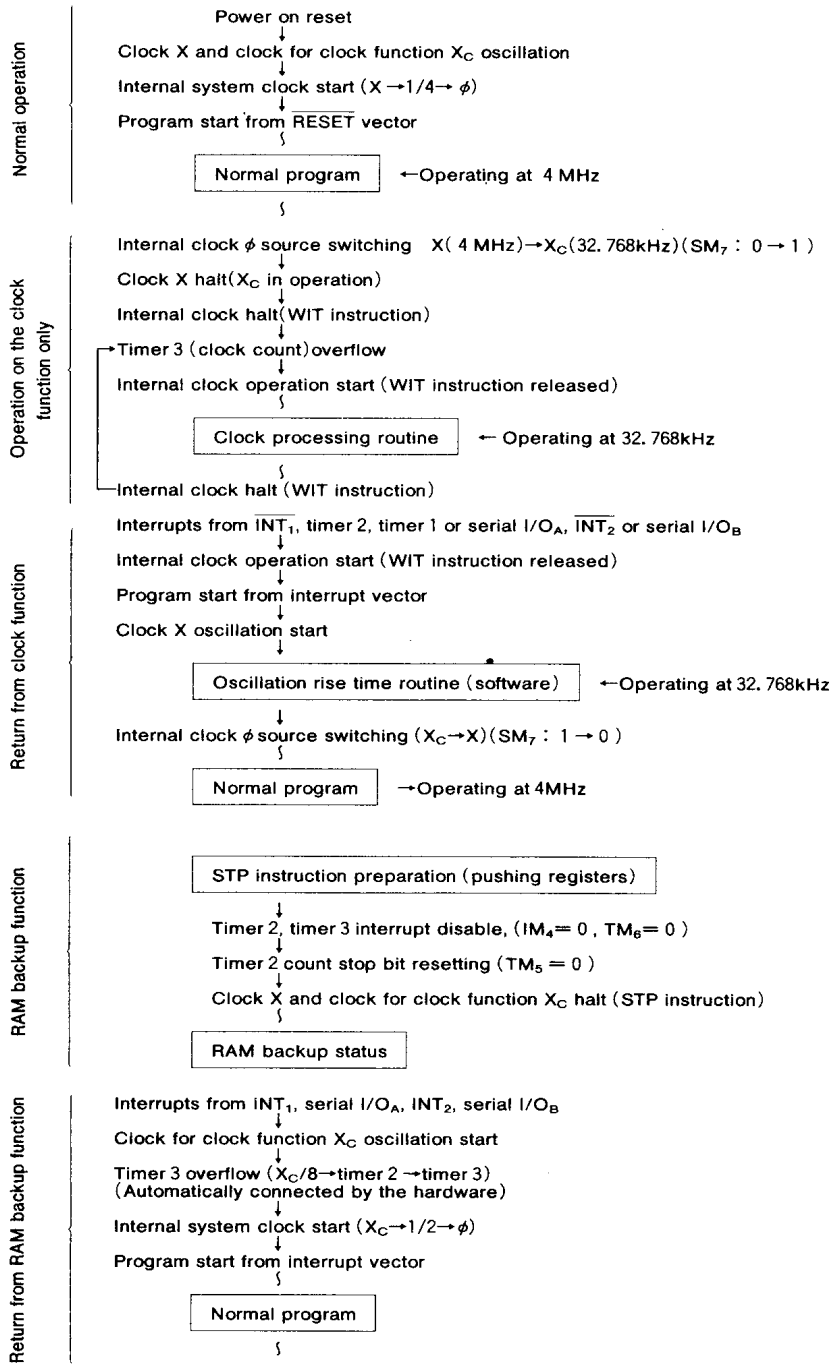


The above example assumes that signals of 4MHz and 32kHz are being applied to pins X_{IN} X_{CIN} respectively. φ signifies the internal clock.

Note 1 : Approximately 8ms of latency time are automatically generated upon release from the STP instruction due to connections of timer 2 and 3.
2 : Approximately 500ms of latency time exists after the release of the STP instruction.
3 : When the internal clock 1/8 frequency is connected as a timer count source the count source becomes 2kHz.

Fig.43 Transition of states for the system clock

<An example of flow for system>



PROGRAMMING NOTES

(1) Processor status register

1. Except for the interrupt inhibit flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
   The T flag and D flag which affect arithmetic operations, must always be initialized.
2. A NOP instruction must be used after the execution of a PLP instruciton.

(2) Interrupts

Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Decimal operations

1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction. In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
2. The N (Negative), V (Overflow), and Z (Zero) flags are ignored during decimal mode.

(4) Timers

The frequency dividing ratio of timer is $1/(n+1)$.

(5) STP instruction

The STP instruction must be executed after setting the timer 2 count stop bit (bit 5 at address $00FF_{16}$) to supply ("0").

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mask specification form
- ROM data·····EPROM 3 sets

Write the following option on the mask confirmation form

(1) Port P1 pull-up transistor bit
(2) Port P2 pull-up transistor bit
(3) X_{IN} and X_{CIN} oscillation feed-back registers
(4) CRT display signal input/output polarity
(5) ϕ output

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state.	−0.3∼6	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}		−0.3∼13	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_7$, $P5_1$∼$P5_7$, $P6_0$∼$P6_5$, H_{SYNC}, V_{SYNC}, X_{IN}, X_{CIN}, OSC1		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P6_2$∼$P6_5$		−0.3∼13	V
V_O	Output voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_7$, $P3_0$∼$P3_7$, $P5_1$∼$P5_7$, $P6_0$, $P6_1$, X_{OUT}, ϕ, X_{COUT}, OSC2, R, G, B, I, OUT		−0.3∼V_{CC}+0.3	V
I_{OH}	Circuit current $P6_0$, $P6_1$, $P4_7$, R, G, B, I, OUT		0∼10(Note 1)	mA
I_{OL1}	Circuit current $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_7$, $P5_1$∼$P5_7$, $P6_0$, $P6_1$, R, G, B, I, OUT		0∼15(Note 2)	mA
I_{OL2}	Circuit current $P0_0$∼$P0_7$, $P6_2$∼$P6_5$	$V_O \leqq 7$ V	0∼15(Note 2)	mA
		$V_O > 7$ V	0∼1(Note 2)	
P_d	Power dissipation	T_a = 25℃	1000(Note 3)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : The total of I_{OH} should be 20mA(max).
2 : The total of I_{OL1} and I_{OL2} should be 50mA(max).
3 : 600mW in case of the flat package.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Supply voltage (Note 4)	Normal speed mode $f(X_{IN})$=4MHz $f(OSC1)$=5MHz	4.5	5.0	5.5	V
		Low-speed mode $f(X_{CIN})$=32kHz	3.0	5.0	5.5	
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_7$, $P5_1$∼$P5_7$, $P6_0$∼$P6_5$, $\overline{RESET}$, X_{IN}, X_{CIN}, H_{SYNC}, V_{SYNC}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, $P3_3$∼$P3_5$, $P3_7$, $P4_7$, $P5_1$, $P5_4$, $P5_5$, $P5_7$, $P6_0$∼$P6_5$		0		0.4V_{CC}	V
V_{IL}	"L" input voltage $P3_2$, $P3_6$, $P5_2$, $P5_3$, $P5_6$, $\overline{RESET}$, X_{IN}, X_{CIN}, H_{SYNC}, V_{SYNC}		0		0.2V_{CC}	V
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_7$, $P5_1$∼$P5_7$, $P6_0$∼$P6_5$, R, G, B, I, OUT				5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P6_2$∼$P6_5$	$V_O \leqq 7$V			5	mA
		$V_O > 7$V			1	
$I_{OH(avg)}$	"H" average output current $P4_7$, $P6_0$, $P6_1$, R, G, B, I, OUT				2	mA
$f(X_{IN})$	Oscillating frequency (Note 5)		3.6	4	4.4	MHz
$f(X_{CIN})$	Oscillating frequency		29	32	35	kHz
f(OSC1)	Oscillating frequency		4	5	6	MHz

Note 4 : Apply 0.022μF or greater capacitance externally to the V_{CC} power supply pin so as to reduce power source noise.
5 : Use a ceramic resonator or a quartz crystal oscillator to generate of main clock.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−10~70℃, f(X_{IN})=4MHz)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P4_7$, $P6_0$, $P6_1$, R, G, B, I, OUT	V_{CC}=4.5V, I_{OH} =−0.5mA		2.4			V
V_{OH}	"H" output voltage ϕ	V_{CC}=4.5V I_{OH} =−2.5mA		2.4			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_7$, $P5_1$~$P5_7$, $P6_0$~$P6_5$, R, G, B, I, OUT	V_{CC}=4.5V I_{OL} =0.5mA				0.4	V
V_{OL}	"L" output voltage $P1_0$~$P1_7$	V_{CC}=4.5V I_{OL} =10mA				1.5	V
V_{OL}	"L" output voltage ϕ	V_{CC}=4.5V I_{OL} =2.5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5.0V			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$, $P3_6$, $P5_2$, $P5_3$, $P5_6$, H_{SYNC}, V_{SYNC}	V_{CC}=5.0V			0.5	1.3	V
R_U	Pull-up transister (Note 6) $P1_0$~$P1_7$, $P2_0$~ $P2_7$	V_{CC}=5.0V V_I=0V		15	30	60	kΩ
I_{OZH}	"H" input leak current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_7$, $P5_1$~$P5_7$, $P6_0$~$P6_5$, $\overline{RESET}$, H_{SYNC}, V_{SYNC}	V_{CC}=5.5V V_O=5.5V				5	μA
I_{OZH}	"H" input leak current $P0_0$~$P0_7$, $P6_0$~$P6_5$	V_{CC}=5.5V V_O=12V				10	μA
I_{OZL}	"L" input leak current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_7$, $P5_1$~$P5_7$, $P6_0$~$P6_5$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$	V_{CC}=5.5V V_O=0V				5	μA
V_{RAM}	RAM retention voltage	At stop mode		2.5		5.5	V
I_{CC}	Supply current	V_{CC}=5.5V f(X_{IN})=4MHz At system operation and CRT display off			5	10	mA
		V_{CC}=5.5V f(X_{IN})=4MHz At system operation and CRT display on			7	14	
		V_{CC}=5.5V f(X_{IN})=4MHz At wait mode			1		
		X_{IN}−X_{OUT} stop f(X_{CIN})=32kHz At system operation	V_{CC}=5.5V		60	200	μA
			V_{CC}=3V		25		
		X_{IN}−X_{OUT} stop f(X_{CIN})=32kHz At wait mode	V_{CC}=5.5V		25	100	
			V_{CC}=3V		5		
		At stop mode	V_{CC}=5.5V		1	10	
			V_{CC}=3V		0.6		

Note 6 : Pull-up transistor is mask option.