

PJ4812

25V Dual N-Channel Enhancement Mode MOSFET

FEATURES

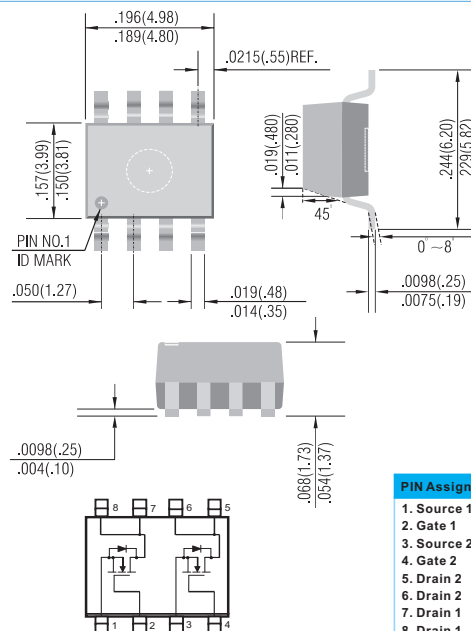
- $R_{DS(ON)}$, $V_{GS}@10V, I_{DS}@5.8A=15m\Omega$
- $R_{DS(ON)}$, $V_{GS}@4.5V, I_{DS}@4.7A=24m\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICAL DATA

- Case: SOIC-08 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 4812

SOIC-08

Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	25	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	5.8	A
Pulsed Drain Current ¹⁾	I_{DM}	24	A
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$ 2.0 $T_A=75^\circ\text{C}$ 1.2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$
Avalanche Energy with Single Pulse $I_D=23A, V_{DD}=25V, L=0.5mH$	E_{AS}	130	mJ
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, $t \leq 10$ sec

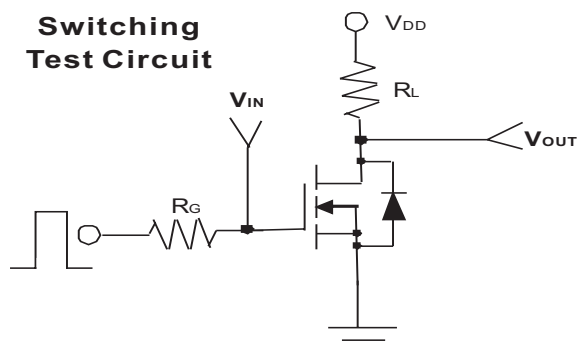
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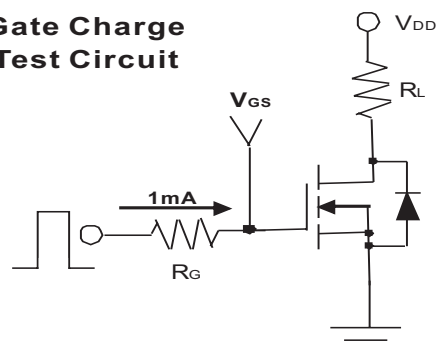
ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	25	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=4.7A$	-	19.8	24.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.8A$	-	12.0	15.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=25V, V_{GS}=0V$	-	-	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=5.8A$	20	-	-	S
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=5.8A, V_{GS}=5V$	-	15.8	-	nC
		$V_{DS}=15V, I_D=5.8A$ $V_{GS}=10V$	-	26.8	-	
Q_{gs}	-		5.0	-		
Q_{gd}	-		5.5	-		
Turn-On Delay Time	$T_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1A, V_{GEN}=10V$ $R_G=3.6\Omega$	-	12	14	ns
Turn-On Rise Time	t_{rr}		-	10	12.5	
Turn-Off Delay Time	$t_{d(off)}$		-	32	37.5	
Turn-Off Fall Time	t_f		-	6.5	8	
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1.0MHz$	-	1450	-	pF
Output Capacitance	C_{oss}		-	260	-	
Reverse Transfer Capacitance	C_{rss}		-	150	-	
Source-Drain Diode						
Max. Diode Forward Current	I_s	-	-	-	1.7	A
Diode Forward Voltage	V_{SD}	$I_s=1.7A, V_{GS}=0V$	-	0.73	1.2	V

Switching Test Circuit



Gate Charge Test Circuit



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Typical Characteristics Curves ($T_J=25^\circ\text{C}$, unless otherwise noted)

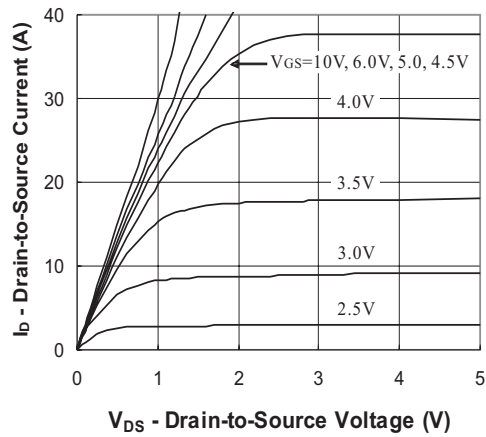


FIG.1- Output Characteristic

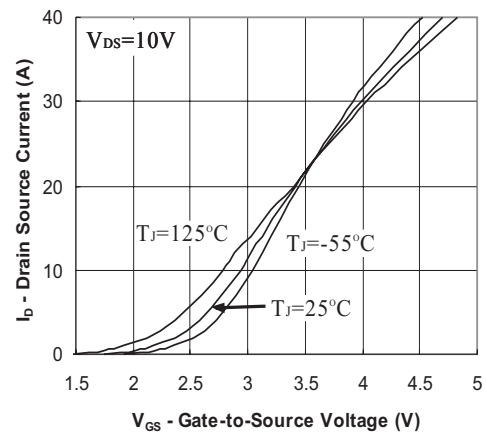


FIG.2- Transfer Characteristic

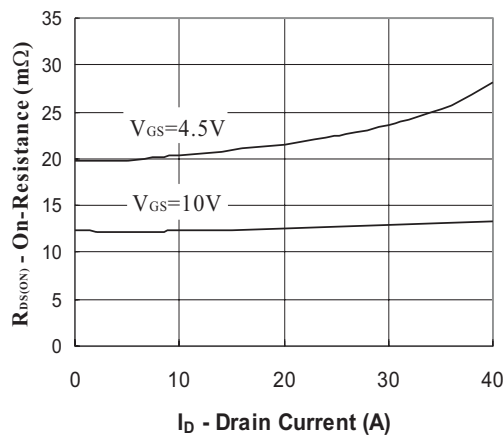


FIG.3- On Resistance vs Drain Current

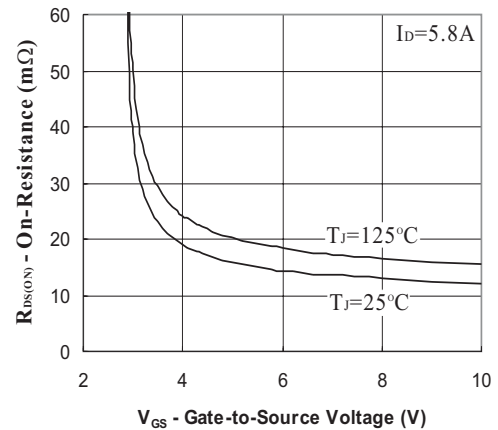


FIG.4- On Resistance vs Gate to Source Voltage

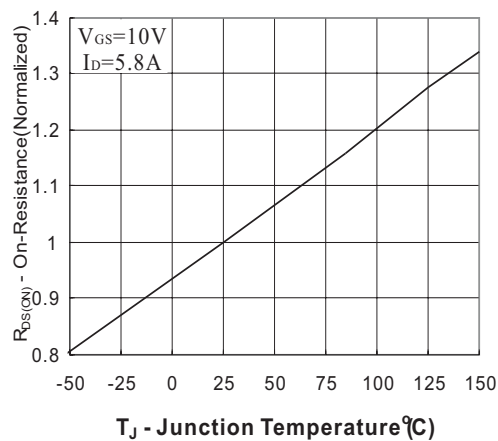


FIG.5- On Resistance vs Junction Temperature

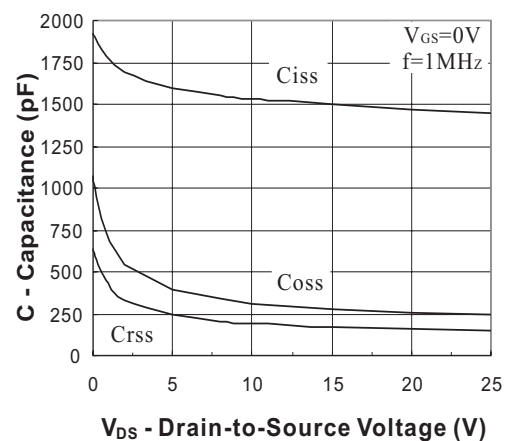


FIG.6- Capacitance

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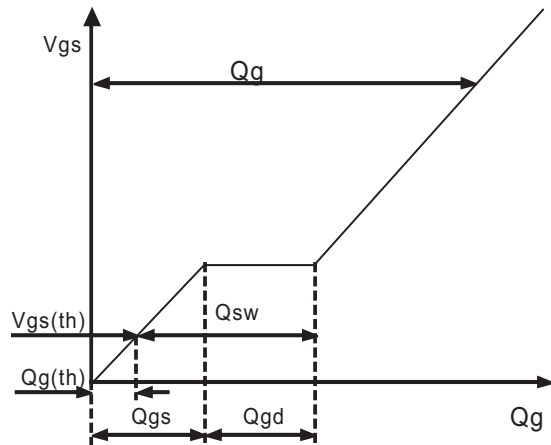


Fig. 7 - Gate Charge Waveform

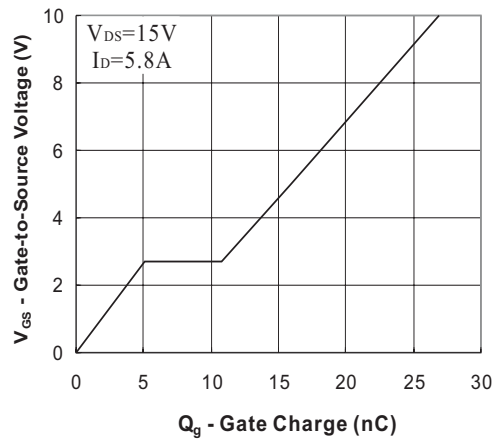


Fig. 8 - Gate Charge

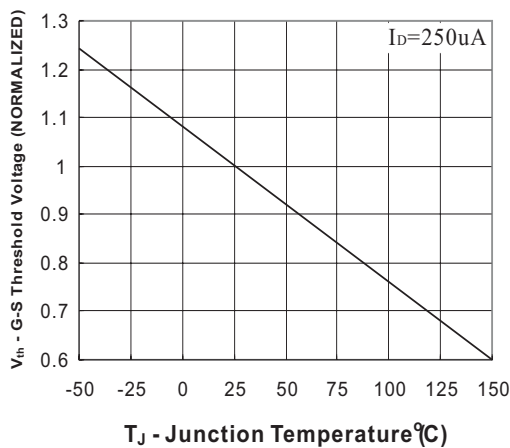


Fig. 9 - Threshold Voltage vs Temperature

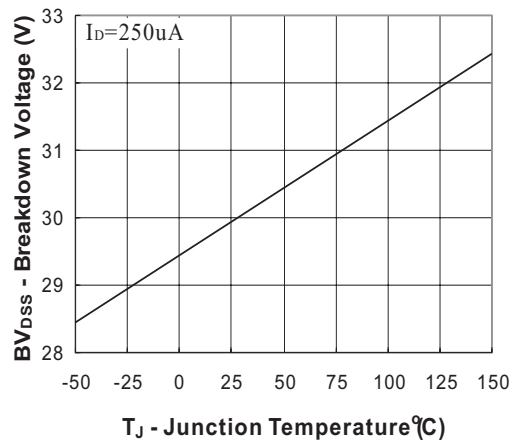


Fig. 10 - Breakdown Voltage vs Junction Temperature

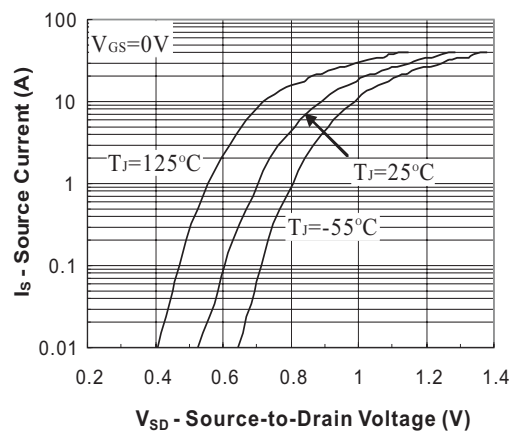
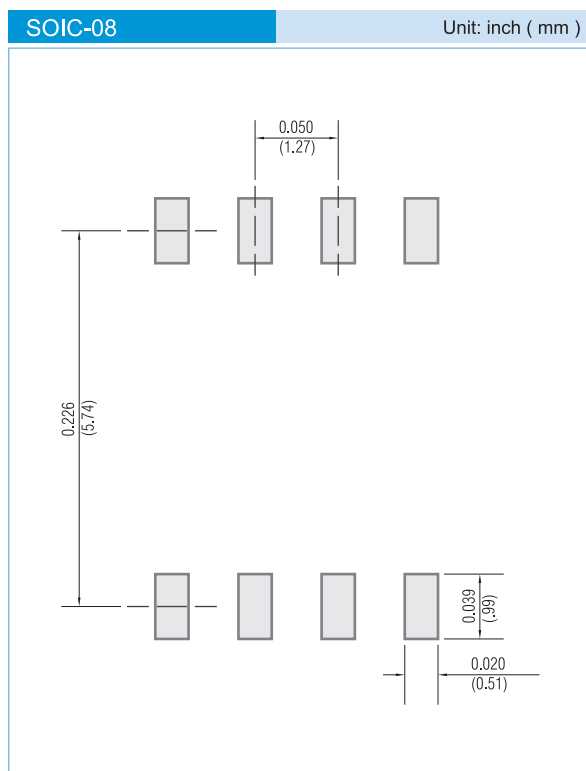


Fig. 11 - Source-Drain Diode Forward Voltage

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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
T/R - 3K per 13" plastic Reel

LEGAL STATEMENT

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