LMX2581 Wideband Frequency Synthesizer with Integrated VCO

Check for Samples: LMX2581

FEATURES

General Features

- **50 – 3760 MHz Operating Frequency**
- **Low Voltage Logic Compatibility**
- **Digital Lock Detect**
- **32 Pin QFN Package**

High Performance PLL

- **-229 dBc/Hz Normalized PLL Phase Noise**
- **-120.8 dBc/Hz Normalized PLL 1/f Noise**
- **200 MHz Maximum Phase Detector Frequency**
- **Programmable Charge Pump Current**

Broadband Multi-Core VCO

- **Tuning Range: 1880 - 3760 MHz**
- **-137 dBc/Hz Phase Noise @ 1 MHz for a 2.5 GHz Carrier**
- **Programmable Output Power**
- **Programmable Option to Use an External VCO**

Low Noise VCO Divider

- **Programmable to divide by 1 (bypass), 2, 4, 6, 8, ... , 38**
- **-155 dBc/Hz Noise Floor**

TARGET APPLICATIONS

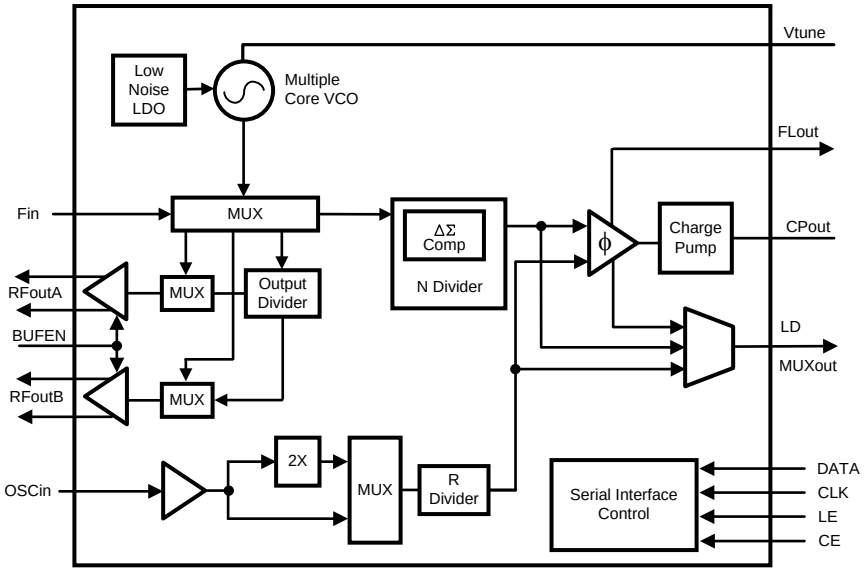
- **Wireless Infrastructure (UMTS, LTE, WiMax, Multi-Standard Base Stations)**
- **Broadband Wireless**
- **Wireless Meter Reading**
- **Test and Measurement**
- **Clock Generation**

DESCRIPTION

The LMX2581 is an ultra low noise wideband frequency synthesizer which integrates a delta-sigma fractional N PLL, a VCO with fully integrated tank circuit, and an optional frequency divider.

The LMX2581 integrates several low-noise, high precision LDOs to provide superior supply noise immunity and more consistent performance. When combined with a high quality reference oscillator, the LMX2581 generates a very stable, ultra low noise signal. The internal VCO can be bypassed so that an external VCO can be used.

FUNCTIONAL BLOCK DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

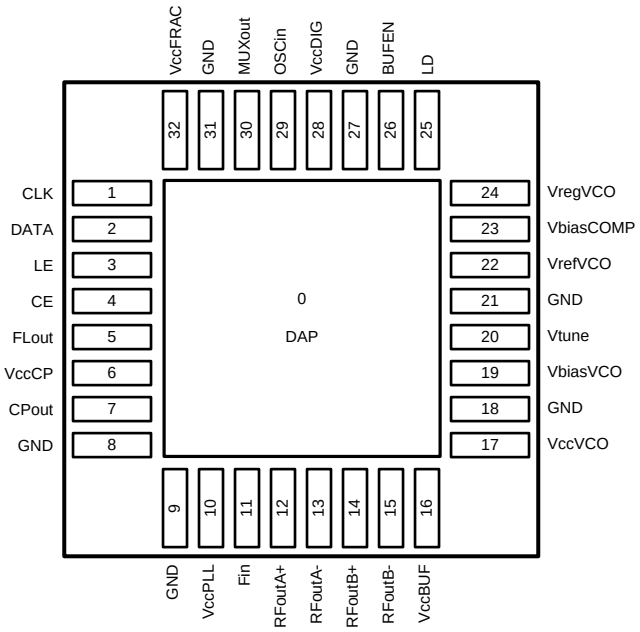


Table 1. Pin Descriptions

Pin #	Pin Name	Type	Description
0	DAP	GND	The DAP should be grounded
1	CLK	Input	MICROWIRE Clock Input. High Impedance CMOS input
2	DATA	Input	MICROWIRE Data. High Impedance CMOS input
3	LE	Input	MICROWIRE Latch Enable. High Impedance CMOS input
4	CE	Input	Chip Enable Pin
5	FLout	Output	Fastlock Output that can be high Z or ground.
6	VccCP	Supply	Charge Pump Supply
7	CPout	Output	Charge Pump Output
8	GND	GND	Ground for the Charge Pump.
9	GND	GND	Ground for the N and R divider.
10	VccPLL	Supply	Supply for the PLL
11	Fin	Input	High frequency input pin for an external VCO. Leave Open or Ground if not used.
12	RFoutA+	Output	Differential divided output.
13	RFoutA-	Output	Differential divided output.
14	RFoutB+	Output	Differential divided output.
15	RFoutB-	Output	Differential divided output.
16	VccBUF	Supply	Supply for the Output Buffer
17	VccVCO	Supply	Supply for the VCO
18	GND	GND	Ground Pin for the VCO. This can be attached to the regular ground. Ensure a solid trace connects this pin to the bypass capacitors on pins 19, 23, and 24.
19	VbiasVCO		Bias circuitry for the VCO. Place a 2.2 µF capacitor to GND (Preferably close to Pin 18).
20	Vtune	Input	VCO tuning Voltage input
21	GND	GND	VCO ground.

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Table 1. Pin Descriptions (continued)

Pin #	Pin Name	Type	Description
22	VrefVCO		VCO capacitance. Place a capacitor to GND (Preferably close to Pin 18). This value should be between 5% and 10% of the capacitance at pin 24. Recommended value is 1 uF.
23	VbiasCOMP		VCO bias voltage temperature compensation circuit. Place a 10 uF capacitor to GND (Preferably close to Pin 18). If it is possible, put two 10 uF capacitors as this may improve the VCO phase noise slightly.
24	VregVCO		VCO regulator output. Place a 10 uF capacitor to GND (Preferably close to Pin 18). If it is possible, put two 10 uF capacitors as this may improve the VCO phase noise slightly.
25	LD	Output	Lock detect output
26	BUFEN	Input	Enable pin for the RF output buffer
27	GND	GND	Digital Ground.
28	VccDIG	Supply	Digital Supply
29	OSCin	Input	Reference input clock
30	MUXout	Output	Multiplexed output that can select lock detect, N divider, or R dividert.
31	GND	GND	Ground for the fractional circuitry.
32	VccFRAC	Vcc	Supply for the fractional circuitry.

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Absolute Maximum Ratings(1) (2)

Parameter	Symbol	Ratings	Units
Power Supply Voltage	Vcc	-0.3 to 3.6	V
Input Voltage to Pins other than Vcc Pins	V_{IN}	-0.3 to (Vcc + 0.3)	V
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 sec.)	T_L	+260	°C
Voltage on OSCin (Pin29)	V_{OSCin}	≤1.8 with Vcc Applied ≤1 with Vcc=0	Vpp

(1) "Absolute Maximum Ratings" indicate limits beyond which permanent or latent damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics.

(2) This device has an ESD rating of ≥2500 V Human Body Model (HBM), ≥ 1250 V Charged Device Model (CDM), and ≥ 250 V Machine model (MM). It should only be assembled in ESD free workstations.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	Vcc	3.15	3.3	3.45	V
Ambient Temperature	T_A	-40		85	°C

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Electrical Characteristics

(3.15 V ≤ Vcc ≤ 3.45 V, -40°C ≤ T_A ≤ 85 °C; except as specified. Typical values are at Vcc = 3.3 V, 25 °C.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Current Consumption							
I_{CC}	Entire Chip Supply Current	One Output Enabled OUTx_PWR = 15			178		mA
I_{CC}Core	Supply Current Except for Output Buffers	VCO Divider Bypassed			134		mA
I_{CC}RFout	Additive Current for Output Buffer	OUTx_PWR = 15			44		mA
I_{CC}VCO_DIV	Additive VCO Divider Current	VCO Divider > 1			20		mA
I_{CC}PD	Power Down Current	Device Powered Down (CE Pin = LOW)			7		mA
OSCin Reference Input							
f_{OSCin}	OSCin Frequency Range	Doubler Enabled		5		250	MHz
		Doubler Disabled		5		900	
v_{OSCin}	OSCin Input Voltage	AC Coupled		0.4		1.7	Vpp
$Spur_{Foscin}$	Oscin Spur				-81		dBc
PLL							
f_{PD}	Phase Detector Frequency	Fractional Mode				200	MHz
K_{PD}	Charge Pump Gain	Gain = 1X			110		µA
		Gain = 2X			220		
		...			...		
		Gain = 31X			3410		
$PN_{PLL_1/f}$	Normalized PLL 1/f Noise	Gain > 8X			- 120.8		dBc /Hz
PN_{PLL_Flat}	Normalized PLL Noise Floor	Gain > 8X			- 229		dBc /Hz
f_{RFin}	External VCO Input Pin Frequency	Internal VCOs Bypassed (OUTA_PD=OUTB_PD=1)		0.5		2.2	GHz
p_{RFin}	External VCO Input Pin Power	Internal VCOs Bypassed (OUTA_PD=OUTB_PD=1)		0		+8	dBm
$Spur_{Fpd}$	Phase Detector Spurs	Fpd = 25 MHz			-85		dBc
		Fpd = 100 MHz			-71		
VCO (1)							
f_{VCO}		Before the VCO Divider	All VCO Cores Combined	1880		3760	
K_{VCO}	VCO Gain	Vtune = 1.3 Volts (2)	Core 1		12 - 24		MHz/ V
			Core 2		15 - 30		
			Core 3		20 - 37		
			Core 4		21 - 37		
ΔT_{CL}	Allowable Temperature Drift (3)	VCO not being recalibrated	Fvco ≥2.5 GHz	-125		+125	°C
			Fvco < 2.5 GHz	- 100		+125	

(1) All four VCO cores cover the range as reported in the specifications and the typical tuning ranges for each core are also reported. However, at some of the frequencies that are at the boundary of two cores, it might not be always possible to ensure which core the LMX2581 would use to achieve this frequency.
(2) The lower number for the VCO gain applies to the lower end of the tuning range for that VCO core and the upper number for the VCO gain applies to the upper range for that VCO core.
(3) Continuous tuning range over temperature refers to programming the device at an initial temperature and allowing this temperature to drift WITHOUT reprogramming the device. This drift could be up or down in temperature and the spec does not apply to temperatures that go outside the recommended operating temperatures of the device.

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Electrical Characteristics (continued)

(3.15 V ≤ Vcc ≤ 3.45 V, -40°C ≤ T_A ≤ 85 °C; except as specified. Typical values are at Vcc = 3.3 V, 25 °C.)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{VCOCal}	VCO Calibration Time (4)	f_{OSCin} = 100 MHz f_{PD} = 100 MHz Full Band Change 1880 — 3760 MHz	No Pre-programming		140		us
			With Pre-programming		10		
PN_{VCO}	VCO Phase Noise (OUTx_PWR =15)	f_{VCO} = 1.9 GHz Core 1	10 kHz Offset		-84.8		dBc /Hz
			100 kHz Offset		-113.7		
			1 MHz Offset		-136.7		
			10 MHz Offset		-154.2		
			40 MHz Offset		-156.7		
		f_{VCO} = 2.2 GHz Core 2	10 kHz Offset		-84.6		dBc /Hz
			100 kHz Offset		-114.1		
			1 MHz Offset		-137.5		
			10 MHz Offset		-154.5		
			40 MHz Offset		-155.2		
		f_{VCO} = 2.7 GHz Core 3	10 kHz Offset		-81.7		dBc /Hz
			100 kHz Offset		-111.1		
			1 MHz Offset		-135.5		
			10 MHz Offset		-152.9		
			40 MHz Offset		-154.6		
		f_{VCO} = 3.3 GHz	10 kHz Offset		-77.9		dBc /Hz
			100 kHz Offset		-108.0		
			1 MHz Offset		-132.4		
			10 MHz Offset		-151.5		
			40 MHz Offset		-153.6		
Outputs							
$p_{RFoutA+/-}$ $p_{RFoutB+/-}$	Output Power Level (5)	OUTx_PWR=15 Inductor Pull-Up Fout=2.7 GHz			5		dBm
$H2_{RFoutX+/-}$	Output Power Level (6)	OUTx_PWR = 15 Fout = 2.7 GHz			-25		dBc
Digital Interface (DATA, CLK, LE, CE, MUXout,BUFEN, LD)							
V_{IH}	High-Level Input Voltage			1.4		Vcc	V
V_{IL}	Low Level Input Voltage					0.4	V
I_{IH}	High-Level Input Current	V_{IH} = 1.75 V		-5		5	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V		-5		5	µA
V_{OH}	High-Level Output Voltage	I_{OH} = -500 µA		2			V
V_{OL}	Low-Level Output Voltage	I_{OL} = -500 µA			0	0.4	V
MICROWIRE Timing							
t_{ES}	Clock to Enable Low Time	See Serial Data Input Timing		35			ns

(4) When the VCO is programmed to a frequency, it goes through a digital calibration where it searches for the correct frequency band until it reaches the final frequency band. After this frequency calibration is done, the VCO will typically be far less than 1 MHz within the final target frequency. This final frequency error is corrected analog lock time, which is totally loop filter dependent, but it can be made <2 us for a wide enough loop filter (perhaps at the expense of fractional spurs). The number reported in the electrical specifications is for this digital VCO calibration time only. The lock time can be greatly reduced if the user can preprogram the device with an initial starting point for which VCO core and what frequency band in the core to start the VCO frequency calibration at. Even if it is the wrong core and the wrong band, it can greatly reduce the lock time provided that this frequency close (<20 MHz) of the final settling frequency.
(5) The output power is dependent of the setup and is also programmable. Consult the Applications section for more information.
(6) The harmonics vary as a function of frequency, output termination, board layout, and output power setting. Reported number is for an OUTx_PWR of 15.

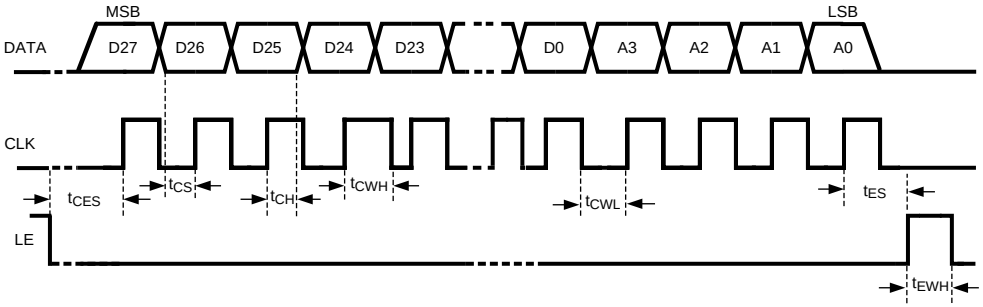
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Electrical Characteristics (continued)

(3.15 V ≤ Vcc ≤ 3.45 V, -40°C ≤ T_A ≤ 85 °C; except as specified. Typical values are at Vcc = 3.3 V, 25 °C.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CS}	Data to Clock Set Up Time	See Serial Data Input Timing	10			ns
t_{CH}	Data to Clock Hold Time	See Serial Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High	See Serial Data Input Timing	25			ns
t_{CWL}	Clock Pulse Width Low	See Serial Data Input Timing	25			ns
t_{CES}	Enable to Clock Set Up Time	See Serial Data Input Timing	10			ns
t_{EWH}	Enable Pulse Width High	See Serial Data Input Timing	10			ns

SERIAL DATA INPUT TIMING



There are several other considerations for programming:

- The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter.
- A slew rate of at least 30 V/us is recommended for the CLK, DATA, and LE signals
- If the CLK and DATA lines are toggled while the in VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

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Functional Description

The LMX2581 is a low power, high performance frequency synthesizer system which includes a PLL (Phased Locked Loop), VCO (Voltage Controlled Oscillator), VCO Divider, and Programmable Output Buffer.

OSCin INPUT and OSCin DOUBLER

The OSCin pin is driven with a single-ended signal which is used to as a frequency reference. Before the OSCin frequency reaches the phase detector, it can be doubled with the OSCin doubler and/or divided with the PLL R divider.

Because the OSCin signal is used as a clock for the VCO calibration, the OSC_FREQ field needs to be programmed correctly and a proper signal needs to be applied at the OSCin pin at the time of programming the R0 register order for the VCO calibration to properly work. Higher slew rates tend to yield the best fractional spurs and phase noise, so a square wave signal is best for OSCin. If using a sine wave, higher frequencies tend to yield better phase noise and fractional spurs due to their higher slew rates. The OSCin pin his high impedance, so for optimal performance, it is recommended to use either a shunt resistor or resistive pad to make such that the impedances looking towards our device and from the looking away from our device (as seen by the OSCin pin) are both close to 50 ohms

R DIVIDER

The R divider divides the OSCin frequency down to the phase detector frequency. With this device, it is possible to use both the doubler and the R divider at the same time.

PLL N DIVIDER AND FRACTIONAL CIRCUITRY

The N divider includes fractional compensation and can achieve any fractional denominator (PLL_DEN) from 1 to 4,194,303. The integer portion, PLL_N, is the whole part of the N divider value and the fractional portion, PLL_NUM / PLL_DEN, is the remaining fraction. PLL_N, PLL_NUM, and PLL_DEN are software programmable. So in general, the total N divider value, N, is determined by: N = PLL_N + PLL_NUM / PLL_DEN The order of the delta sigma modulator is programmable from integer mode to third order. There are also several dithering modes that are also programmable. In order to make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

PLL PHASE DETECTOR AND CHARGE PUMP

The phase detector compares the outputs of the R and N dividers and generates a correction current corresponding to the phase error. This charge pump current is software programmable to many different levels. The phase detector frequency, f_{PD}, can be calculated as follows: $f_{PD} = f_{OSCin} \times OSC_2X / R$. The charge pump outputs a correction current the loop filter, which is implemented with external components.

EXTERNAL LOOP FILTER

The LMX2581 requires an external loop filter. The design of this filter is application specific and can be done by software provided on the Texas Instruments website. For the LMX2581, it is recommended for the best possible VCO noise to ensure a capacitor of at least 3.3 nF next to the VCO. Not doing so will degrade the VCO phase noise at offsets in the 100k-1MHz region, although the device will still function properly.

LOW NOISE, FULLY INTEGRATED VCO

The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies and divider values as follows: $f_{VCO} = f_{PD} \times N = f_{OSCin} \times OSC_2X \times N / R$. The VCO is fully integrated, including the tank inductors.

In order to the reduce the VCO tuning gain and therefore improve the VCO phase noise performance, the internal VCO is actually four VCO cores working in conjunction. These cores starting from lowest frequency to highest frequency are VCO 1, VCO 2, VCO 3, and VCO 4. Each VCO core has 256 different frequency bands. This creates the need for frequency calibration in order to determine the correct VCO core and correct frequency band in that VCO core. The frequency calibration routine is activated any time that the R0 register is programmed with the NO_FCAL bit equal to zero. In order for this frequency calibration to work properly, the OSC_FREQ field needs to be set to the correct setting. The are also programmable settings that allow the user to suggest a particular VCO core for the device to choose.

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PROGRAMMABLE VCO DIVIDER

The VCO divider can be programmed to even values from 2 to 38 as well as bypassed by either one or both of the RFout outputs. When the zero delay mode is not enabled, the VCO divider is not in the feedback path between the VCO and the PLL and therefore has no impact on the PLL loop dynamics. After this programmable divider is changed, it may be beneficial to reprogram the R0 register to recallibrate the VCO . The frequency at the RFout pin is related to the VCO frequency and divider value, VCO_DIV, as follows: $f_{RFout} = f_{VCO}$ / VCO_DIV When this divider is enabled, there will be some far-out phase noise contribution to the VCO noise. .

When changing to a VCO_DIV value of 4, either from a state of VCO_DIV=2 or OUTx_MUX = 0, it is necessary to program VCO_DIV first to a value of 6, then to a value of 4. This holds for no other VCO_DIV value and is not necessary if the VCO frequency (but not VCO_DIV) is changing

0–DELAY MODE

In the event that the VCO divider is not used, there is a deterministic phase relationship between the OSCin and RFout pins. However, when the VCO divider is used, it creates an ambiguous phase relationship when 0–Delay mode is not enabled. When 0–Delay mode is enabled, it includes the VCO divider in the feedback path to make the phase relationship between OSCin and Fout deterministic.

When this mode is used, special care needs to be taken because it does interfere with the VCO calibration if not done correctly. The correct way to use 0–Delay mode is as follows

Calibration with Zero Delay

1. Program the 0_DLY bit = 1
2. Program the NO_FCAL bit = 1
3. Program the R0 register with the RF_N value multiplied by the VCO_DIV value.
4. Set the NO_FCAL bit = 0
5. Program the R0 register again with RF_N value not being multiplied by the VCO_DIV value.

DETERMINING THE OUTPUT FREQUENCY

Based on the oscillator input frequency (f_{OSC}), PLL R divider value (PLL_R), PLL N Divider Value (PLL_N), Fractional Numerator (PLL_NUM), Fractional Denominator (PLL_DEN), and VCO divider value (VCO_DIV), the output frequency of the LMX2581 (f_{OUT}) can be determined as follows:

$f_{OUT} = f_{OSC}$ x OSC_2X / PLL_R x (PLL_N + PLL_NUM / PLL_DEN) / VCO_DIV

PROGRAMMABLE RF OUTPUT BUFFERS

The output states of the RFoutA and RFoutB pins are controlled by the BUFEN pin as well as the BUFEN_DIS programming bit. If the pin is powered up, then output power can be programmed to various levels with the OUTx_PWR fields.

OUTA_PD OUTB_PD	BUFEN_DIS	BUFEN Pin	Output State
1	X	X	Powered Down
0	0	X	Powered Up
	1	Low	Powered Down
		High	Powered Up

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POWERDOWN MODES

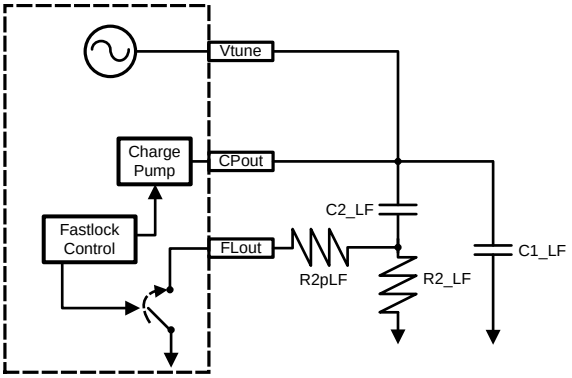
The LMX2581 can be powered down either partially or fully. The partial powerdown powers down the PLL, VCO, and output buffer, but keeps the LDOs running. The full powerdown powers down everything, although register settings are still retained. The type of powerdown is governed by the PWDN_MODE field and the CE pin in accordance to the following table.

PWDN_MODE	CE Pin	Device State
0	X	Powered Up
1	X	Full Powerdown
3	X	Partial Powerdown
4	Low	Full Powerdown
		Powered Up
5	Low	Partial Powerdown
	Up	Powered Up
7	Low	Full Powerdown
	High	Partial Powerdown
2,6	X	Invalid State

When coming out of a full powerdown state, it is necessary to do the initial power on programming sequence described in later sections. If coming out of a partial powerdown state, it is necessary to do the sequence for switching frequencies after initialization, that is described in later sections.

FASTLOCK

The LMX2581 includes the Fastlock™ feature that can be used to improve the lock times. When the frequency is changed, a timeout counter is used to engage the fastlock for a programmable amount of time. During the time that the device is in Fastlock, the FLout pin changes from high impedance to low, thus switching in the external resistor R2pLF in parallel with R2_LF.



Parameter	Normal Operation	Fastlock
Charge Pump Gain	CPG	FL_CPG
FLout Pin	High Impedance	Grounded

Once the loop filter values and charge pump gain are known for normal operation, they can be determined for fastlock operation as well. In normal operation, one can not use the highest charge pump gain and still use fastlock because there will be no larger current to switch in. The resistor and the charge pump current are changed simultaneously so that the phase margin remains the same while the loop bandwidth is by a factor of K as shown in the following table:

Parameter	Symbol	Calculation
Charge Pump Gain in Fastlock	FL_CPG	Typically use the highest value.
Loop Bandwidth Multiplier	K	K=sqrt(FL_CPG/CPG)
External Resistor	R2pLF	R2 / (K-1)

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Lock Detect

The LMX2581 offers two forms of lock detect, Vtune and Digital Lock Detect, which could be used separately or in conjunction. Digital Lock Detect gives a reliable indication of lock/unlock if programmed correctly with the one exception of when the PLL is locked to a valid OSCin signal and then the OSCin signal is abruptly removed. In this case, digital lock detect can sometimes still indicate a locked state, but Vtune Lock detect will correctly indicate an unlocked state. Therefore, for the most reliable lock detect, it is recommended to use these in conjunction, because they cover the deficits of each other.

Vtune Lock Detect

This style of lock detect only works with the internal VCO. Whenever the tuning voltage goes below the threshold of about 0.5 volts or above the threshold of about 2.2 volts, the internal VCO will become unlocked and the Vtune lock detect will indicate that the device is unlocked. For this reason, when the Vtune lock detect says the PLL is unlocked, one can be certain that it is unlocked.

Digital Lock Detect

This lock detect works by comparing the phase error as presented to the phase detector. If the phase error plus the delay as specified by the PFD_DLY bit outside the tolerance as specified by DLD_TOL, then this comparison would be considered to be an error, otherwise passing. At higher phase detector frequencies, it may be necessary to adjust the DLD_ERR_CNT and DLD_PASS_CNT. The DLD_ERR_CNT specifies how may errors are necessary to cause the circuit to consider the PLL to be unlocked. The DLD_PASS_CNT multiplied by 8 specifies how many passing comparisons are necessary to cause the PLL to be considered to be locked and also resets the count for the errors. The DLD_ERR_CNT and DLD_PASS_CNT values can be decreased to make the circuit more sensitive, but if lock detect is made too sensitive chattering can occur and these values should be increased.

PART ID AND REGISTER READBACK

The LMX2581 allows any of its registers to be read back. This could be useful for

- Register Readback
  - By reading back the register values, it can be confirmed that the correct information was written. In addition to this, Register R6 has special diagnostic information that could potentially be useful for debugging problem.
- Part ID Readback
  - By reading back the part ID, this information can be used by whatever device is programming the LMX2581 to identify this device and know what programming information to send. In addition to this, the BUFEN and CE pins can be used to create 4 unique part ID values. Although these pins can impact the device, they can be overridden in software. It is not necessary to have the device programmed in order to do part ID readback.

The procedure for doing this readback is as follows:

1. Hold the LE pin high
2. Send 32 clocks to the CLK pin and monitor the output at the LD pin to read back the bit stream of 32 bits
3. Depending on the settings for the ID(R0[31]) and RDADDR (R6[8:5]), information a different bit stream will be returned as shown in the following table. .

ID	RDADDR	BUFEN Pin	CE Pin	Read Back Code
0	6	X	X	Register Readback (Register R6)
1	0	0	0	0x 00000500
	0	0	1	0x 00000510
	1	1	0	0x 00000520
	1	1	1	0x 00000530

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General Programming Information

The LMX2581 is programmed using several 32-bit registers. A 32-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 bits, ADDR[3:0] form the address field, which is used to decode the internal register address. The remaining 28 bits form the data field DATA[27:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank.

Recommended Initial Power on Programming Sequence

When the device is first powered up, the device needs to be initialized and the ordering of this programming is very important. The following is the sequence. After this sequence is complete, the device should be running and locked to the proper frequency.

1. Apply power to the device and ensure the Vcc pins are at the proper levels.
2. Ensure that a valid reference is applied to the OSCin pin
3. Program register R5 with RESET=1
4. Program registers R15,R13,R10,R9,R8,R7,R6,R5,R4,R3,R2,R1,R0
5. Wait 20 ms
6. Program the R0 register again OR do the recommended sequence for changing frequencies.

Recommended Sequence for Changing Frequencies

After the device has gone through the initial power on programming sequence, it is not necessary to do this again. The recommended sequence for changing frequencies is as follows:

1. (optional) If the OUTx_MUX State is changing, program Register R5
2. (optional) If the VCO_DIV state is changing, program Register R3. See section on VCO_DIV if programming a to a value of 4.
3. (optional) If the MSB of the fractional numerator or charge pump gain is changing, program register R1
4. (Required) Program register R0

Although not necessary, it is also acceptable to program the R0 register a second time after this programming sequence.

Triggering Registers

The action of programming certain registers may trigger special actions as shown in the table below.

Reg	Conditions	Actions Triggered	Why this is done
R5	RESET = 1	All Registers are reset to power on default values. This takes less than 1 us. The reset bit is self-clearing.	The registers are reset by the power on reset circuitry when power is initially applied. The RESET bit allows the user the option to perform the same functionality of the power on reset through software.
R0	NO_FCAL = 0	—Starts the Frequency Calibration —Engages Fastlock (If FL_TOC>0)	This activates the frequency calibration, which chooses the correct VCO core and also the correct frequency band within that core. This is necessary whenever the frequency is changed. If it is desired that the R0 register be programmed without activating this calibration, then the NO_FCAL bit can be set to zero. If the fastlock timeout counter is programmed to a nonzero value, then this action also engages fastlock.
R0	NO_FCAL = 1	—Engages Fastlock (If FL_TOC>0)	This engages fastlock, which can be used to decrease the lock time in some circumstances.

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Table 2. Register Map

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[27:0]																												ADDRESS[3:0]			
R15	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	VCO_CAP_MAN	VCO_CAPCODE[7:0]								1	1	1	1
R13	DLD_ERR_CNT[3:0]				DLD_PASS_CNT[9:0]										DLD_TOL [2:0]			1	0	0	0	0	0	1	0	0	0	0	1	1	0	1
R10	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0
R9	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1
R8	0	0	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	1	1	1	0	0	0
R7	0	FL_SELECT [4:0]					FL_PINMODE [2:0]			FL_INV	MUXOUT_SELECT [4:0]					MUX_INV	MUXOUT_PINMODE [2:0]			LD_SELECT [4:0]					LD_INV	LD_PINMODE[2:0]			0	1	1	1
R6	0	RD_DIAGNOSTICS[19:0]																				1	0	RDADDR[3:0]				uWIRE_LOCK	0	1	1	0
R5	0	0	0	0	0	0	0	OUT_LDEN	OSC_FREQ[2:0]			BUFEN_DIS	0	0	0	VCO_SEL_MODE [1:0]		OUTB_MUX [1:0]		OUTA_MUX [1:0]		0_DLY	MODE [1:0]		PWDN_MODE [2:0]			RESET	0	1	0	1
R4	PFD_DLY [2:0]			FL_FRCE	FL_TOC[11:0]												FL_CPG[4:0]					0	CPG_BLEED[5:0]						0	1	0	0
R3	0	0	1	0	0	0	0	0	0	VCO_DIV[4:0]			OUTB_PWR[5:0]							OUTA_PWR[5:0]							OUTB_PD	OUTA_PD	0	0	1	1
R2	0	0	OSC_2X	0	CPP	1	PLL_DEN[21:0]																						0	0	1	0
R1	CPG[4:0]					VCO_SEL [1:0]	PLL_NUM[21:12]											FRAC_ORDER [2:0]			PLL_R[7:0]								0	0	0	1
R0	ID	FRAC_DITHER [1:0]		NO_FCAL	PLL_N[11:0]												PLL_NUM[11:0]												0	0	0	0

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Programming Field Descriptions

REGISTER R15

The programming of register R15 is not necessary and only needs to be done in situations where the programming fields in this register need to be changed. This is typically for diagnostic purposes or improving the digital VCO calibration time.

VCO_CAP_MAN — Manual VCO Band Select

This bit determines if the value of VCO_CAPCODE is just used as a starting point for the initial frequency calibration or if the VCO is forced to this value. If this is forced, it is only for diagnostic purposes.

VCO_CAP_MAN	Impact of VCO_CAPCODE	Application
0	Determines initial starting point for VCO calibration.	Setting the VCO_CAPCODE field can improve the digital calibration time.
1	Forces the band for the VCO all the time.	For diagnostic purposes only.

VCO_CAPCODE[7:0] — Capacitor Value for VCO Band Selection

This field selects the capacitor value that is initially used for the VCO tank when the VCO calibration is run or that is forced when VCO_CAP_MAN is set to one. The lower values correspond to less capacitance, which corresponds to a higher VCO Frequency for that given VCO Core. If not using this feature, the default value for this field is 128.

VCO_CAPCODE	VCO Tank Capacitance	VCO Frequency
0	Minimum	Highest
...	...	
255	Maximum	Lowest

REGISTER R13

Register R13 gives access to bits that are used for the digital lock detect circuitry.

DLD_ERR_CNT[3:0] - Digital Lock Detect Error Count

This is the amount of phase detector comparisons that may exceed the tolerance as specified in DLD_TOL before digital lockindicates an unlocked state. The recommended default is 4 for phase detector frequencies of 80 MHz or below, but larger values may be necessary for higher phase detector frequencies.

DLD_PASS_CNT[9:0] - Digital Lock Detect Success Count

This value multiplied by 8 is the amount of amount of phase detector comparisons within the tolerance specified by DLD_TOL and adjusted by DLD_ERR_CNT that are necessary that are necessary to cause the digital lock to indicate a locked state. The recommended default value is 32 for phase detector frequencies of 80 MHz or below, but larger values may be necessary for higher phase detector frequencies.

DLD_TOL[2:0] — Digital Lock Detect

This is the tolerance that is used to compare with each phase error to decide if it is a success or a fail. Larger settings are generally recommended, but they are limited by several factors such as PFD_DLY, modulator order, and especially the phase detector frequency.

DLD_TOL	Phase Error Tolerance (ns)	Typical Phase Detector Frequency
0	1	Fpd > 130 MHz
1	1.7	80 MHz > Fpd >= 130 MHz
2	3	60 MHz > Fpd >= 80 MHz
3	6	45 MHz > Fpd >= 60 MHz
4	10	30 MHz >Fpd >= 45 MHz
5	18	Fpd <= 30 MHz
6–7	Reserved	n/a

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REGISTERS R10, R9, and R8

These registers have no functions that are disclosed to the user. However, it is still important to program them to the values specified in the register map because they are necessary for proper operation.

REGISTER R7

This register has fields that control status pins, which would be LD, MUXout, and FLout

FL_PINMODE[2:0], MUXOUT_PINMODE[2:0], and LD_PINMODE[2:0] — Output Format for Status Pins

These fields control the state of the output pin

FL_PINMODE MUXOUT_PINMODE LD_PINMODE	Output Type
0	TRI-STATE (Default for LD_PINMODE)
1	Push-Pull (Default for MUXOUT_PINMODE)
2	Open Drain
3	High Drive Push-Pull (Can drive 5 mA for an LED)
4	High Drive Open Drain
5	High Drive Open Source
6,7	Reserved

FL_INV, MUX_INV, LD_INV - Inversion for Status Pins

The logic for the LD and MUXOUT pins can be inverted with these bits.

FL_INV MUX_INV LD_INV	Pin Status
0	Normal Operation
1	Inverted

FL_SELECT[4:0], MUXOUT_SELECT[4:0], LD_SELECT[4:0] — State for Status Pins

This field controls the output state of the MUXout, LD, and FLout pins. Note that during fastlock, the FL_SELECT field is ignored.

FL_SELECT MUXOUT_SELECT LD_SELECT	Output
0	Vcc
1	Lock Detect (Based on Phase Measurement)
2	Lock Detect (Based on tuning voltage)
3	Lock Detect (Based on Phase Measurement AND tuning voltage)
4	Readback (Default for MUXOUT_SELECT)
5	PLL_N divided by 2
6	PLL_N divided by 4
7	PLL_R divided by 2
8	PLL_R divided by 4
9	Analog Lock Detect
10	OSCin Detect
11	Fin Detect
12	Calibration Running

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FL_SELECT MUXOUT_SELECT LD_SELECT	Output
13	Tuning Voltage out of Range
14	VCO calibration fails in the low frequency direction.
15	VCO Calibration fails in the high frequency direction.
16-31	Reserved

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REGISTER R6

RD_DIAGNOSTICS[19:0] — Readback Diagnostics

This field is contains several pieces of information that can be read back for debug and diagnostic purposes.

RD_DIAGNOISTICS[19:0]																
R6 [30:29]		R6 [28]	R6 [27]	R6 [26]	R6 [25:22]	R6 [21]	R6 [20]	R6 [19]	R6 [18]	R6 [17]	R6 [16]	R6 [15]	R6 [14]	R6 [13]	R6 [12]	R6 [11]
19	18	17	16	15	[14:11]	10	9	8	7	6	5	4	3	2	1	0
VCO_SELECT		FIN_DETECT	OSCIN_DETECT	VCO_DETECT	Reserved	CAL_RUNNING	VCO_RAIL_HIGH	VCO_RAIL_LOW	Reserved	VCO_TUNE_HIGH	VCO_TUNE_VALID	FLOUT_ON	DLD	LD_PINSTATE	CE_PINSTATE	BUFEN_PINSTATE

field Name	Meaning if Value is One
VCO_ SELECT	This is the VCO that the device chose to use. 0 = VCO 1, 1 = VCO 2, 2 = VCO 3, 3 = VCO 4
FIN_DETECT	Indicates transitions at the Fin pin have been detected. This could either be the VCO signal or self-oscillation of the Fin pin in the even that no signal is present. This bit needs to be manually reset by programing register R5 with R5[30] = 1, and then again with bit R5[30]=0
OSCIN_DETECT	Indicates transitions at the OSCin pin have been detected. This could either be a signal at the OSCin pin or self-oscillation at the OSCin pin in the event no signal is present . This bit needs to be manually reset by programming R5 with R5[29] = 1 and then again with R5[29] = 0.
CAL_RUNNING	Indicates that some calibration in the part is currently running.
VCO_RAIL_HIGH	Indicates that the VCO frequency calibration failed because the VCO would need to be a higher frequency than it could achieve.
VCO_RAIL_LOW	Indicates that the VCO frequency calibration failed because the VCO would need to be a lower frequency than it could achieve.
VCO_TUNE_HIGH	Indicates that the VCO tuning voltage is higher than 2.4 volts and outside the allowable range.
VCO_TUNE_VALID	Indicates that the VCO tuning voltage is inside then allowable range.
FLOUT_ON	Indicates that the FLout pin is low.
DLD	Indicates that the digital lock detect phase measurement indicates a locked state. This does not include any consideration of the VCO tuning voltage.
LD_PINSTATE	This is the state of the LD Pin.
CE_PINSTATE	This is the state of the CE pin.
BUFEN_PINSTATE	This is the state of the BUFEN pin.

RDADDR[3:0] — Readback Address

When the ID bit is set to zero, this designates which register is read back from. When the ID bit is set to one, the unique part ID information is read back.

ID	RDADDR	Information Read Back
1	Don't Care	Part ID
0	0	Register R0
	1	Register R1
	...	...
	15 (default)	Register R15

uWIRE_LOCK - Microwire lock

uWIRE_LOCK	Microwire
0	Normal Operation
1	Locked out – All Programming except to the uWIRE_LOCK bit is ignored

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REGISTER R5

OUT_LDEN — Mute Outputs Based on Lock Detect

When this bit is enabled, the RFoutA and RFoutB pins are disabled if the PLL digital lock detect circuitry indicates that the PLL is in the unlocked state.

OUT_LDEN	PLL Digital Lock Detect Status	RFoutA / RFoutB Pins
0	Don't Care	Normal Operation
1	Locked	Normal Operation
1	Unlocked	Powered Down

OSC_FREQ[2:0] — OSCin Frequency for VCO Calibration

This bit should be set to in accordance to the OSCin frequency BEFORE the doubler. It is critical for running internal calibrations for this device.

OSC_FREQ	OSCin Frequency
0	f_{OSCin} < 128 MHz
1	128 ≤ f_{OSCin} < 256 MHz
2	256 ≤ f_{OSCin} < 512 MHz
3	512 ≤ f_{OSCin}
>=4	Reserved

BUFEN_DIS - Disable for the BUFEN Pin

This pin allows the BUFEN pin to be disabled. This is useful if one does not want to pull this pin high or use it for the readback ID.

BUFEN_DIS	BUFEN Pin
0	Impacts Output buffers
1	Ignored.

VCO_SEL_MODE — Method of Selecting Internal VCO Core

This field allows the user to choose how the VCO selected by the VCO_SEL field is treated. Note setting 0 should not be used if switching from a frequency above 3 GHz to a frequency below 2.2 GHz.

VCO_SEL_MODE	VCO Selection
0	VCO core is automatically selected based on the last one that was used. If none was used before, it chooses the lowest frequency VCO core.
1	VCO selection starts at the value as specified by the VCO_SEL field. However, if this is invalid, it will choose another VCO.
2	VCO is forced to the selection as defined by the VCO_SEL field, regardless of whether it is valid or not. Note that this mode is not ensured and is only included for diagnostic purposes.
3	Reserved

OUTB_MUX — Mux for RFoutB

This bit determines whether RFoutB is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTB_MUX	RFoutB Frequency
0	f_{VCO}
1	f_{VCO} / VCO_DIV
2	f_{Fin}
3	Reserved

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OUTA_MUX — Mux for RFoutA

This bit determines whether RFoutA is the VCO frequency, the VCO frequency divided by VCO_DIV, or the fin frequency.

OUTA_MUX	RFoutB Frequency
0	f_{VCO}
1	f_{VCO} / VCO_DIV
2	f_{Fin}
3	Reserved

0_DLY - Zero Delay Mode

When this mode is enabled, the VCO divider is put in the feedback path of the PLL so that the delay from input to output of the device will be deterministic.

0_DLY	Phase Detector Input
0	Direct VCO or Fin signal.
1	Channel Divider output.

MODE[1:0] — Operating Mode

This field determines what mode the device is run in

MODE	Operational Mode	PLL	VCO	Fin Pin
0	Full Chip Mode	Powered Up	Powered Up	Powered Down
1	PLL Only Mode	Powered Up	Powered Down	Powered Down
2,3	Reserved	Reserved	Reserved	Reserved

PWDN_MODE - Powerdown Mode

This field power the device up and down. Aside from the traditional power up and power down, there is the partial powerdown that powers down the PLL and VCO, but keeps the LDOs powered up to allow the device to power up faster.

PWDN_MODE	CE Pin	Device Status
0	X	Powered Up
1	X	Powered Down
2	X	Reserved
3	X	Partial Powerdown
4	Low	Powered Down
	High	Powered Up
5	X	Reserved
6	Low	Partial Powerdown
	High	Powered Up
7	Low	Powered Down
		Partial Powerdown

RESET - Register Reset

When this bit is enabled, the action of programming register R5 resets all registers to their default power on reset status, otherwise the fields in register 5 can be programmed without resetting all the registers.

RESET	Action of Programming Register R5
0	Registers and state machines are operational.
1	Registers and state machines are reset, then this reset is automatically released.

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REGISTER R4

PFD_DLY[2:0] — Phase Detector Delay

This word controls the minimum on time for the charge pump. The minimum setting often yields the best phase detector spurs and integer mode PLL phase noise. Higher settings can be useful in reducing the delta sigma noise of the modulator when dithering is enabled, but are not generally recommended if the phase detector frequency exceeds 130 MHz. If unsure, default this word to zero.

PFD_DLY	Pulse Width	When Recommended
0	370 ps	Default Use with a 2nd order modulator , when dithering is disabled, or when the phase detector frequency is >130 MHz.
1	760 ps	Consider these settings for a 3rd order modulator when dithering is used.
2	1130 ps	
3	1460 ps	
4	1770 ps	
5	2070 ps	
6	2350 ps	
7	2600 ps	

FL_FRCE — Force Fastlock Conditions

This bit forces the fastlock conditions on provided that the FL_TOC field is greater than zero.

FL_FRCE	Fastlock Timeout Counter	Fastlock
0	0	Disabled
	> 0	Fastlock engaged as long as timeout counter is counting down
1	0	Invalid State
	> 0	Always Engaged

FL_TOC[11:0] — Fastlock Timeout Counter

This field controls the timeout counter used for fastlock.

FL_TOC	Fastlock Timeout Counter	Comments
0	Disabled	Fastlock Disabled
1	2 x Reference Cycles	Fastlock engaged as long as timeout counter is counting down
2	2 x 2 x Reference cycles	
...		
4095	2 x 4095 x Reference cycles	

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FL_CPG[4:0] — Fastlock Charge Pump Gain

This bit determines the charge pump current that is active during fastlock.

FL_CPG	Fastlock Current
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

CPG_BLEED[5:0]

The CPG bleed field is for advanced users who want to get the lowest possible integer boundary spur. The impact of this bit is on the order of 2 dB. For users who do not care about this, the recommendation is to default this field to zero.

User Type	FRAC_ORDER	CPG	CPG Bleed Recommendation
Basic User	X	X	0
Advanced User	< 2	X	0
	X	< 4X	0
	>1	4X ≤ CPG < 12X	2
		12X ≤ CPG	4

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REGISTER R3

VCO_DIV[4:0] — VCO Divider Value

This field determines the value of the VCO divider. Note that the this divider can be bypassed with the OUTA_MUX and OUTB_MUX fields.

VCO_DIV	VCO Divider Value
0	2
1	4
2	6
3	8
4	10
...	...
18	38
20 - 31	Invalid State

OUTB_PWR[5:0] — RFoutB Output Power

This field controls the output power for the RFoutB output.

OUTB_PWR	RFoutB Power
0	Minimum
...	...
47	Maximum
48 – 63	Reserved

OUTA_PWR[5:0] — RFoutA Output Power

This field controls the output power for the RFoutA output.

OUTA_PWR	RFout Power
0	Minimum
...	...
47	Maximum
48 – 63	Reserved.

OUTB_PD — RFoutB Powerdown

This bit powers down the RFoutB output.

OUTB_PD	RFoutB
0	Normal Operation
1	Powered Down

OUTA_PD — RFoutA Powerdown

This bit powers down the RFoutA output.

OUTA_PD	RFoutA
0	Normal Operation
1	Powered Down

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REGISTER R2

OSC_2X — OSCin Doubler

This bit controls the doubler for the OSCin frequency.

OSC_2X	OSCin Doubler
0	Disabled
1	Enabled

CPP - Charge Pump Polarity

This bit sets the charge pump polarity. Note that the internal VCO has a negative tuning gain, so it should be set to negative gain with the internal VCO enabled.

CPP	Charge Pump Polarity
0	Positive
1	Negative (Default)

PLL_DEN[21:0] — PLL Fractional Denominator

These fields control the denominator for the PLL fraction. Note that 0 is only permissible in integer mode.

PLL_DEN	PLL_DEN[21:0]																					
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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REGISTER R1

CPG[4:0] — PLL Charge Pump Gain

This bit determines the charge pump current that used during steady state operation

CPG	Charge Pump Current
0	TRI-STATE
1	1X
2	2X
..	...
31	31X

Note that if the CPG setting is 400 µA or lower, then the CPG_BLEED field needs to be set to 0.

VCO_SEL[1:0] - VCO Selection

These fields allow the user to specify which VCO the frequency calibration starts at. If uncertain, program this bit to 0 to start at the lowest frequency VCO core. A programming setting of 3 (VCO 4) should not be used if switching to a frequency below 2.2 GHz.

VCO_SEL	VCO Selection
0	VCO 1 (Lowest Frequency)
1	VCO 2
2	VCO 3
3	VCO 4 (Highest Frequency)

FRAC_ORDER[2:0] — PLL Delta Sigma Modulator Order

This field sets the order for the fractional engine

FRAC_ORDER	Modulator Order
0	Integer Mode
1	1st Order Modulator
2	2nd Order Modulator
3	3rd Order Modulator
4-7	Reserved

PLL_R[7:0] — PLL R divider

This field sets the value that divides the OSCin frequency.

PLL_R	PLL_R Divider Value
0	256
1	1 (bypass)
...	...
255	255

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REGISTER R0

Register R0 controls the frequency of the device. Also, unless disabled by setting NO_FCAL = 1, the action of writing to the R0 register triggers a frequency calibration for the internal VCO.

ID - Part ID Readback

When this bit is set, the part ID is readback from the device. Consult the Functional Description for more details.

ID	Readback Mode
0	Register
1	Part ID

FRAC_DITHER[1:0] — PLL Fractional Dithering

This bit sets the dithering mode. When the fractional numerator is zero, it is recommended, although not required, to set the FRAC_DITHER mode to disabled for the best possible spurs. Doing this shuts down the fractional circuitry and eliminates fractional spurs for these frequencies. This is the reason why the FRAC_DITHER word is in the R0 register, so that it can be set correctly for every frequency if this setting changes.

FRAC_DITHER	Dithering Mode
0	Weak
1	Medium
2	Strong
3	Disabled

NO_FCAL — Disable Frequency Calibration

Normally, when the R0 register is written to, a frequency calibration for the internal VCO is triggered. However, this feature can be disabled. If the frequency is changed, then this frequency calibration is necessary for the internal VCO.

NO_FCAL	VCO Frequency Calibration
0	Done upon write to R0 Register
1	Not done on write to R0 Register

PLL_N - PLL Feedback Divider Value

This is the feedback divider value for the PLL. There are some restrictions on this depending on the modulator order.

PLL_N	PLL_N[11:0]											
<7	Invalid state											
7	Possible only in integer mode or with a 1st order modulator											
8-9	Possible in integer mode, 1st order modulator, or 2nd order modulator											
10-13	Possible only in integer mode, 1st order modulator, 2nd order modulator, or 3rd order modulator											
14	0	0	0	0	0	0	0	0	1	1	1	0
...	...	...	...	...	...	...	...	...	...	...	...	...
4095	1	1	1	1	1	1	1	1	1	1	1	1

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PLL_NUM[21:12] and PLL_NUM[11:0] — PLL Fractional Numerator

These fields control the numerator for the PLL fraction.

PLL_NUM	PLL_NUM[21:12]										PLL_NUM[11:0]											
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4095	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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APPLICATIONS INFORMATION

VCO Digital Calibration

The VCO has four cores, VCO 1, VCO 2, VCO 3, and VCO 4. Each of these 4 cores has 256 different frequency bands. Band 255 is the lowest frequency for a given core and Band 0 is the highest frequency. When the frequency is changed, the digital VCO goes through the following VCO calibration:

1. Depending on the status of the VCO_SEL field, the starting VCO core is selected.
2. The algorithm starts counting at the default band in this core as determined by the VCO_CAPCODE value.
3. Based on the what the actual VCO output is compared to the target VCO output the VCO increments or decrements the CAPCODE.
4. Repeat step 3 until either the VCO is locked or the VCO is at VCO_CAPCODE = 0 or 255
5. If not locked, then choose the next appropriate VCO if possible and return to step 3. If not possible, the calibration is done.

A good starting point is to set VCO_SEL =2 for VCO 3 and set VCO_SEL_MODE = 1 to start at the selected core. If there is the potential of switching the VCO from a frequency above 3 GHz directly to a frequency below 2.2 GHz, VCO_SEL_MODE can not be set to 0. In this case, VCO_SEL_MODE can still be set to 1 to select a starting core, but the starting core specified by VCO_SEL can not be VCO 4.

The digital calibration time can be dramatically improved by giving the VCO guidance of which VCO core and which VCO_CAPCODE to start with. Even if the wrong VCO core is chosen, which could happen near the boundary of two cores, this calibration time is improved. For situations where the frequency change is small, the device can be programmed to automatically start at the last VCO core used. For applications where the frequency change is relatively small, the best VCO calibration time can often be achieved by setting the VCO_SEL_MODE to choose the last VCO core that was used.

Optimizing the RFoutA and RFoutB Pins

Choosing the Proper Pull-Up Component

The first decision is to whether to use a resistor or inductor for a pull up.

- The resistor pull-up involves placing a 50 Ω resistor to the power supply on each side, which makes the output impedance easy to match to and close to 50 Ω. However, it is higherr current for the same output power, and the maximum possible output power is more limited. For this method, the OUTx_PWR setting should be kept about 30 or less (for a 3.3 volt supply) to avoid saturation.
- The inductor pull-up involves placing an inductor to the power supply. This inductor should look like high impedance at the frequency of interest. This method offers higher output power for the same current and higher maximum output power. The output power is about 3 dB higher for the same OUTx_PWR setting than the resistor pull-up. Because the output impedance will be very high and poorly matched, it is recommended to either keep traces short or AC couple this into a pad for better impedance matching.

If an output is partially used or unused, then treat this as follows:

- If the output is unused, then power it down in software and no external components are necessary.
- If only one side of the differential output is used, include the pull-up component and terminate the unused side such that the impedance as seen by this pin looks similar to the impedance as seen by the used side.

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Choosing the Best Setting for the RFoutA_PWR and RFoutB_PWR Fields

The following table shows the impact of the RFoutA_PWR and RFoutB_PWR on the output. Note that THIS IS THE RELATIVE OUTPUT POWER, NOT THE ACTUAL VALUE OF THE OUTPUT POWER. All settings are normalized to the case of RFoutX_PWR = 15, which typically yields the optimal noise floor. The relative currents are pretty much consistent regardless of the pull-up component used. Note that for the resistive pull-up, setting OUTx_PWR to greater than 30 does not improve the output power, but it draws more current. So settings for OUTx_PWR for the resistive load are not recommended to go much above 30. These numbers are typical for a 3.3 volt supply.

OUTx_PWR	RELATIVE Current (mA)	RELATIVE Output Power for Resistive Pull-Up (dBm)	RELATIVE Output Power for Inductor Pull-Up (dBm)
0	−16	− 9.0	− 9.0
5	− 11	− 4.6	− 4.6
10	− 5	−2.0	−2.0
15	0	0	0
20	+ 5	+ 1.4	+ 1.5
25	+10	+ 2.1	+ 2.8
30	+15	+ 2.4	+ 3.9
35	+20	+ 2.2	+ 4.8
40	+25	+ 1.9	+ 5.4
45	+30	+ 1.4	+5.9

Using External VCO Mode

The LMX2581 allows the user to use an external VCO by using the Fin pin and selecting the external VCO mode for the MODE field. Because this is software selectable, the user can have a setup that switches between the external and internal VCO. Because the Fin pin is close to the RFoutA and RFoutB pins, some care needs to be taken to minimize board crosstalk when both an external VCO and an output buffer is used. If only one output buffer is required, it is recommended to use the RFoutB output because it is physically farther from the Fin pin and therefore will have less board related crosstalk. When using external VCO, it may be necessary to change the phase detector polarity (CPP).

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Optimization of Spurs

The behaviors of the LMX2581 spurs vary with the application and the particular spur of interest. To get the best possible spurs, it sometimes involves actual bench measurements and even trial and error. That being said, there are resources available for better understanding of these spurs and to make the process of optimizing spurs more systematic. Application note 1879, the clock design tool simulation for the LMX2581, and the following table give good background on the LMX2581 fractional spurs and the following sections also give some part-specific tips on how to optimize spurs.

Spur Type	Offset	Ways to Reduce
Phase Detector Spur	Fpd	1. Reduce Phase Detector Frequency 2. Decrease PFD_DLY 3. Decrease CPG_BLEED
Integer Boundary Spur	Fpd/Fden*min{Fnum,Fden/Fnum}	1. Reduce Phase Detector Frequency 2. At OSCin Pin, ensure good slew rate, signal integrity, and that this pin sees about 50 ohms looking outwards.
Primary Fractional Spur	Fpd/Fden	1. Decrease Loop Bandwidth 2. Change Modulator Order
Sub-Fractional Spur	Fpd/Fden/k, k=2,3, or 6	1. Use Dithering 2. Use Larger Equivalent Fractions 3. Reduce Modulator Order 4. Eliminate factors of 2 or 3 in denominator (see AN-1879)

Phase Detector Spur

The phase detector spur occurs at an offset from the carrier equal to the phase detector frequency, Fpd. They have a general increasing tendency as the phase detector frequency increases, although this trend stops around 100 MHz. To minimize this spur, considering using a smaller value for PFD_DLY, smaller value for CPG_BLEED, and a lower phase detector frequency. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, one might see some benefit to using a narrower loop bandwidth or adding poles to the loop filter, but otherwise these spurs are not impacted much by these things.

Fractional Spur - Integer Boundary Spur

This spur occurs at an offset equal to the difference between the VCO frequency and the closest integer channel for the VCO. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, then the integer boundary spur would be at 3 MHz offset. If this spur is outside the loop bandwidth, which it usually is, the largest factor influencing this spur is the phase detector frequency. Lowering the phase detector frequency will reduce this spur significantly. If the phase detector frequency is reduced, charge pump gain should be changed to compensate for this, or the loop filter should be re-designed if this is not possible. If it is closer to the loop bandwidth, a lower loop bandwidth may also improve this spur. This spur can change between the different VCO cores, with VCO 3 having the best performance for this spur. The signal and termination at the OSCin pin may also have a small impact on this spur. Fractional settings such as FRAC_DITHER, FRAC_ORDER, and larger equivalent fractions (i.e. 1000000/4000000 instead of 1/4) may impact this spur by a few dB, but the impact is typically not very much.

Fractional Spur - Primary Fractional Spurs

These spurs occur at multiples of Fpd/Fden and are not the integer boundary spur. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, the primary fractional spurs would be at 1,2,4,5,6,...MHz. These are impacted by the loop filter and modulator order

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Fractional Spur - Sub-Fractional Spurs

These spurs appear at a fraction of Fpd/Fden and depend on modulator order. With the first order modulator, there are no sub-fractional spurs. The second order modulator can produce 1/2 sub-fractional spurs if the denominator is even. A third order modulator can produce sub-fractional spurs at 1/2,1/3, or 1/6 of the offset, depending if it is divisible by 2 or 3. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, we would expect no sub-fractional spurs for a first order modulator, sub-fractional spurs at multiples of 1.5 MHz for a 2nd or 3rd order modulator.

Aside from strategically choosing the fractional denominator and using a lower order modulator, another tactic to eliminate these spurs is to use dithering and express the fraction in larger equivalent terms (i.e. 1000000/4000000 instead of 1/4). However, dithering can also add phase noise, so if dithering is used, this needs to be managed with the various levels of it has and the PFD_DLY word to get the best possible performance.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMX2581SQ/NOPB	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		X2581	Samples
LMX2581SQE/NOPB	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		X2581	Samples
LMX2581SQX/NOPB	ACTIVE	WQFN	RTV	32	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR		X2581	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

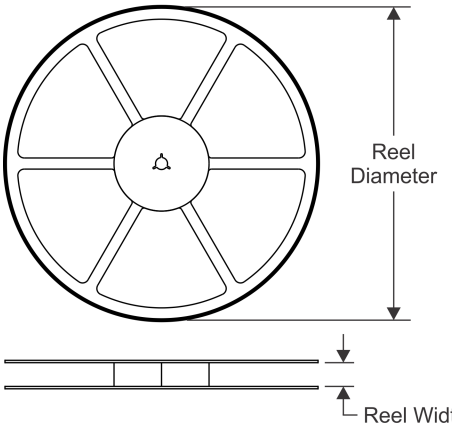
(4) Only one of markings shown within the brackets will appear on the physical device.

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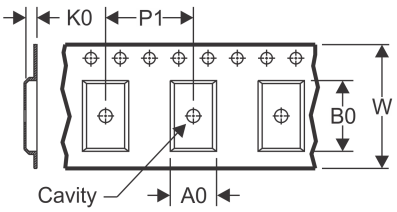
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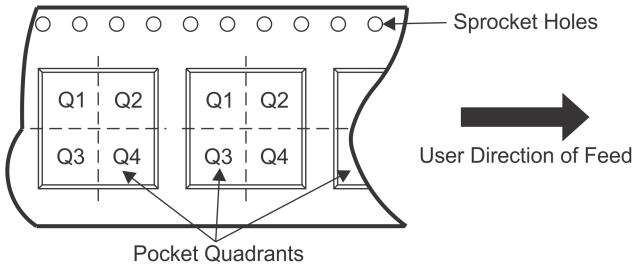


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

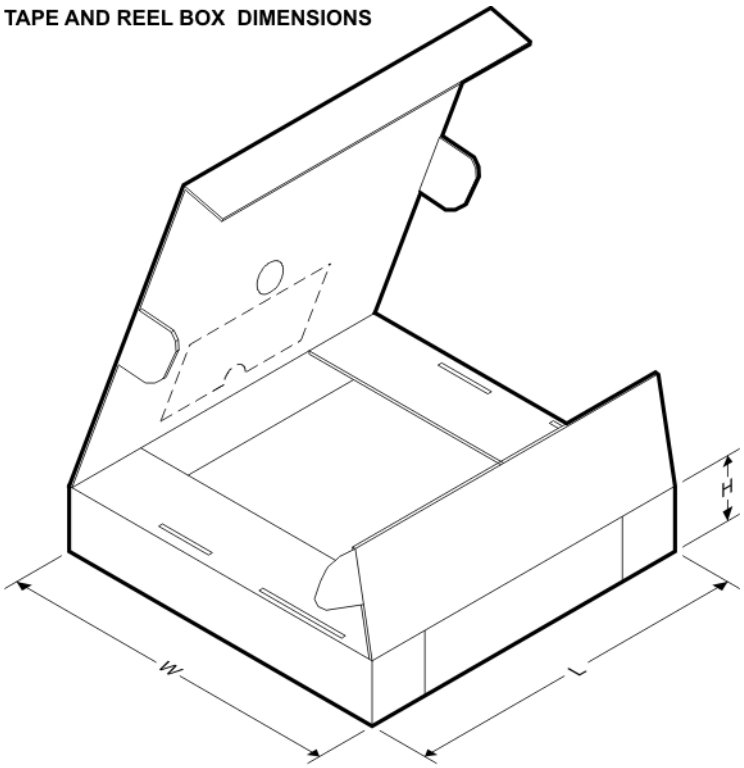
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMX2581SQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMX2581SQE/NOPB	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
LMX2581SQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

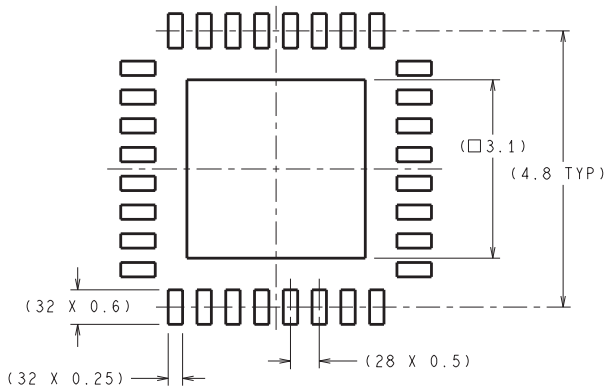
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMX2581SQ/NOPB	WQFN	RTV	32	1000	213.0	191.0	55.0
LMX2581SQE/NOPB	WQFN	RTV	32	250	213.0	191.0	55.0
LMX2581SQX/NOPB	WQFN	RTV	32	4500	367.0	367.0	35.0

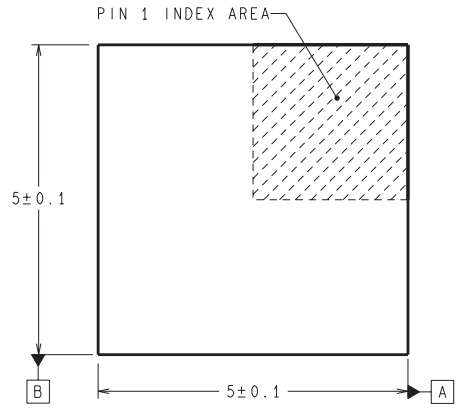
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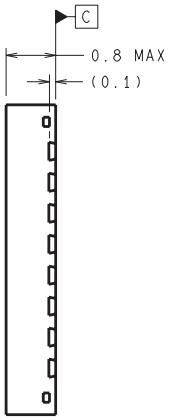


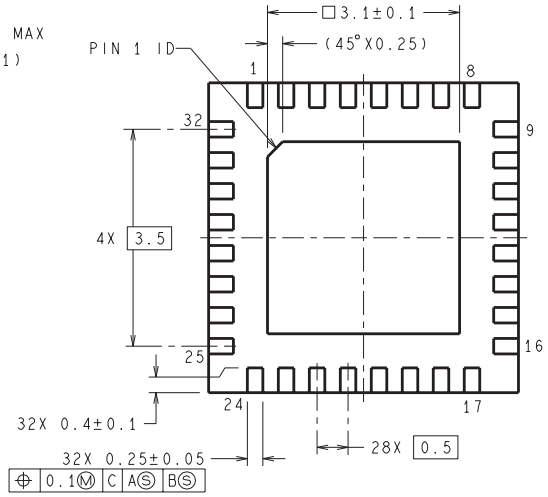
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