DS2125
Ultra3 LVD/SE SCSI 15-Line Terminator

www.maxim-ic.com

GENERAL DESCRIPTION

The DS2125 Ultra3 LVD/SE SCSI terminator is both a low-voltage differential (LVD) and single-ended (SE) terminator. The multimode operation enables the designer to implement LVD in current products while allowing the end user SE backward compatibility with legacy devices. If the device is connected in an LVD-only bus, the DS2125 uses LVD termination. If any SE devices are connected to the bus, the DS2125 uses SE termination, which is accomplished automatically inside the part by sensing the voltage on the SCSI bus DIFFSENS line.

For the LVD termination, the DS2125 integrates two current sources with 15 precision resistor strings. For the SE termination, one regulator and 15 precision 110Ω resistors are used. Two DS2125 terminators are needed for a wide SCSI bus.

APPLICATIONS

Raid Systems
SCSI Host Bus Adapter (HBA) Cards
Servers
SCSI Cables
Network Attached Storage (NAS)
Storage Area Networks (SANs)

ORDERING INFORMATION

PART*	PIN-PACKAGE	TOP MARK**
DS2125	48 LQFP	DS2125
DS2125+	48 LQFP	DS2125
DS2125/T&R	48 LQFP/Tape and Reel	DS2125
DS2125+T&R	48 LQFP/Tape and Reel	DS2125

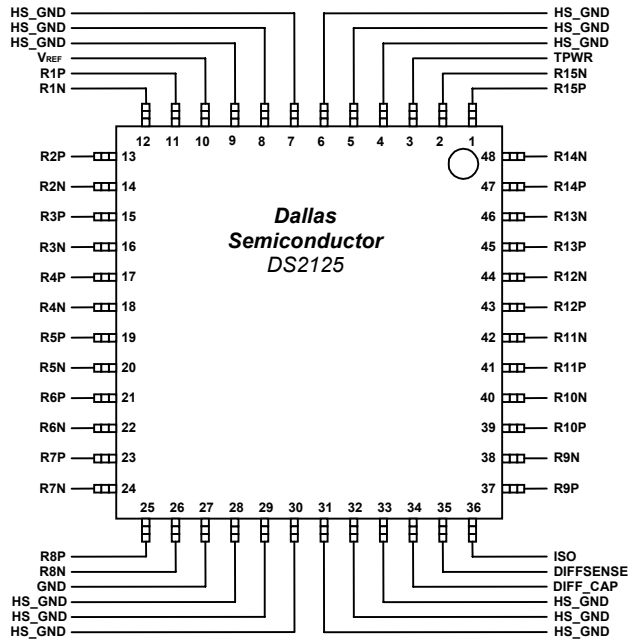
**All devices rated over the commercial operating temperature range, 0°C to +70°C.*
***The top mark includes a "+" for lead-free packages.*
+Denotes lead-free/RoHS-compliant package.

FEATURES

- **Fully Compliant with Ultra3 SCSI**
- **Provides Multimode Low-Voltage Differential/Single-Ended (LVD/SE) Termination for 15 Signal Line Pairs**
- **Auto-Selection of LVD or SE Termination**
- **5% Tolerance on SE and LVD Termination Resistance**
- **Low 3pF Power-Down Capacitance**
- **On-Board Thermal-Shutdown Circuitry**
- **SCSI Bus Hot-Plug Compatible**
- **Fully Supports Actively Negated SE SCSI Signals**

PIN CONFIGURATION

TOP VIEW



LQFP (1.4mm)

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

REV: 012306

ABSOLUTE MAXIMUM RATINGS

V_{REF}, ISO, GND, DIFFSENSE, DIFF_CAP, TPWR, RxP, RxN (x = 1 . . . 15)……-0.3V, +6.0V
V_{REF} Continuous Output Current……±200mA
Continuous Power Dissipation (T_A = +70°C), 48-Pin LQFP……...2W
Operating Temperature Range……0°C to +70°C
Junction Temperature……...+150°C
Storage Temperature Range……...-65°C to +160°C
Lead Temperature (soldering, 10s)……+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(TPWR = 3.3V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TPWR Operating Supply Range	V_{TPWR}	LVD	2.7		5.5	V
		SE	4.0		5.5	
TPWR SUPPLY CURRENT						
TPWR Supply Current (All Lines Open)	I_{TPWR_LVD}	LVD SCSI mode		20	32	mA
	I_{TPWR_SE}	SE SCSI mode		1.6	10	mA
	I_{TPWR_ISO}	ISO mode (terminators disabled)		250	750	µA
LVD TERMINATION (Applies to each line pair, 1 to 15 in LVD mode)						
Differential-Mode Termination Resistance	R_{DM}		100		110	Ω
Common-Mode Termination Resistance	R_{CM}	R_P and R_N shorted together	110		165	Ω
Differential-Mode Bias	V_{DM}	All lines open	100		125	mV
Common-Mode Bias	V_{CM}	R_P and R_N shorted together	1.15	1.25	1.35	V
SE TERMINATION (Applies to SE terminators, 1 to 15 in SE mode)						
Single-Ended Mode Termination Resistance	R_{SE}	$R_{SE} = (V_{Lx} - 0.2) / I_{Lx}$, where V_{Lx} = voltage at terminator pin with pin unloaded and I_{Lx} = current for each terminator pin with the pin forced to 0.2V (Note 2)	104.5	110	115.5	Ω
Termination Current (Note 2)	I_{SE}	Signal level at 0.2V, all lines low	-21.0	-24	-25.4	mA
		Signal level at 0.5V	-18.0		-22.4	
SE Voltage Reference	V_{REF}	(Note 2)	2.7	2.85	3.0	V
Pin Leakage		With ISO high			400	nA
Single-Ended GND Resistance	R_{GND}	Measured at R_P pins, I = 10mA		20	60	Ω
TERMINATOR PIN CAPACITANCE						
Terminator Pin Capacitance	C_{IN}	With ISO high (Note 1)			3	pF
V_{REF} REGULATOR						
1.25V Regulator Output Voltage	V_{REF_LVD}		1.15	1.25	1.35	V
1.25V Regulator Short-Circuit Source Current	I_{SOURCE}	V_{REF} = 0V	-375	-700	-1000	mA
1.25V Regulator Short-Circuit Sink Current	I_{SINK}	V_{REF} = 3.3V	170	300	700	mA
1.25V Regulator Line Regulation		V_{REF} unloaded; vary TPWR from 2.7V to 5.5V		1.0	2.5	%
2.85V Regulator		(Note 2)	2.7	2.85	3.0	V
2.85V Regulator Short-Circuit Source Current		V_{REF} = 0V (Note 2)	-375	-700	-1000	mA
2.85V Regulator Short-Circuit Sink Current		V_{REF} = 3.3V (Note 2)	170	300	700	mA

ELECTRICAL CHARACTERISTICS (continued)

(TPWR = 3.3V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{REF} REGULATOR						
2.85V Regulator Line Regulation		V_{REF} unloaded; vary TPWR from 4.0V to 5.5V		1.0	2.5	%
DIFFSENS OUTPUT						
DIFFSENS Driver Output Voltage	V_{DSO}	-5mA ≤ $I_{DFFSENS}$ ≤ 50µA	1.2		1.4	V
DIFFSENS Driver Source Current	I_{DSH}	$V_{DIFFSENS}$ = 0V	-15		-5	mA
DIFFSENS Driver Sink Current	I_{DSL}	$V_{DIFFSENS}$ = 3.3V	100		200	µA
DIFFSENS Leakage (Note 3)	$I_{LEAK, LOW}$	With ISO high, $\|V_{DIFFSENS}\|$ = 0.3V	-3		+1	µA
	$I_{LEAK, HIGH}$	With ISO high, $\|V_{DIFFSENS} - V_{TPWR}\|$ = 0.3V	1		3	
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		For increasing temperature (Note 1)		150		°C
Thermal-Shutdown Hysteresis		(Note 1)		10		°C
MODE CHANGE DELAY/FILTER						
Mode Change Delay	t_{DELAY}		0.66	1.25	2.00	ms
LOGICAL SIGNALS (ISO)						
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input High Voltage	V_{IH}		2		TPWR + 0.3	V
Input Current	I_{IL}	V_{CC} = 3.3V	-30	-10		µA
DIFF_CAP						
Input Current	I_L	V_{IL} = -0.3V	-1		+1	µA
DIFF_CAP SE Operating Range	V_{SEOR}		-0.3		+0.5	V
DIFF_CAP LVD Operating Range	V_{LVDOR}		0.7		1.9	V
DIFF_CAP HVD Operating Range	V_{HVDOR}		2.4		V_{TPWR} + 0.3	V

Note 1: Guaranteed by design.

Note 2: TPWR = 4.0V.

Note 3: Room temperature only.

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2, 11–26, 37–48	RxP, RxN	Signal Termination. Connect to SCSI bus signal lines.
3	TPWR	Termination Power. Connect to the SCSI TERMPWR line and decouple with a 2.2µF capacitor.
4–9, 28–33	HS_GND	Heat-Sink Ground. Internally connected to the mounting pad. This should be grounded.
10	V_{REF}	Reference Voltage. 2.85V reference in SE mode and 1.25V reference in LVD mode; must be decoupled with a 4.7µF capacitor.
27	GND	Ground. Signal ground, 0V.
34	DIFF_CAP	DIFFSENSE Capacitor. Connect a 0.1µF capacitor for the DIFFSENSE filter. Input to detect the type of device (differential or single-ended) on the SCSI bus.
35	DIFFSENSE	DIFFSENSE. Output to drive the SCSI bus DIFFSENS line.
36	ISO	Isolation. When pulled high, the DS2125 isolates its bus pins (RxN, RxP) from the SCSI bus.

Figure 1. Block Diagram

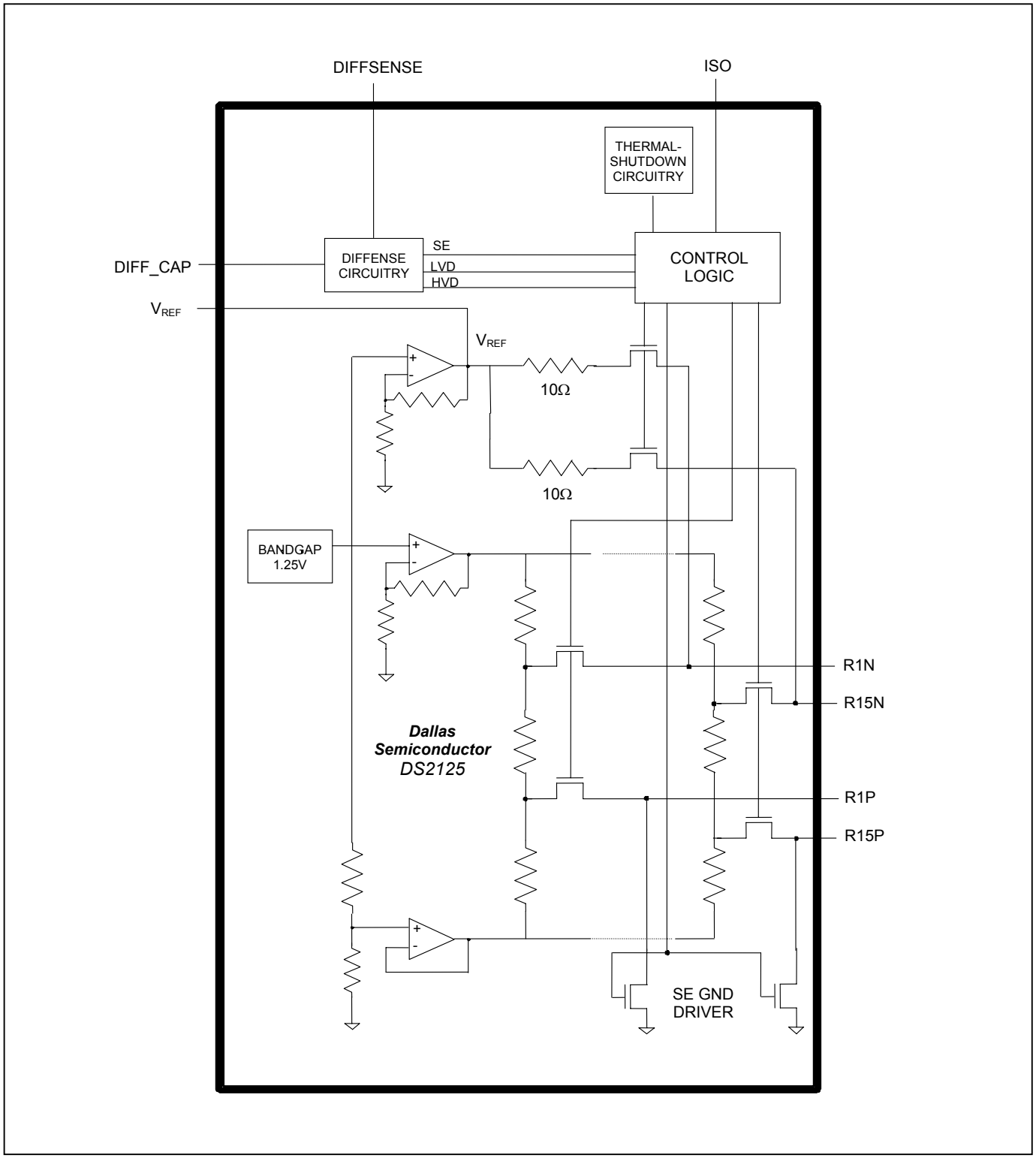
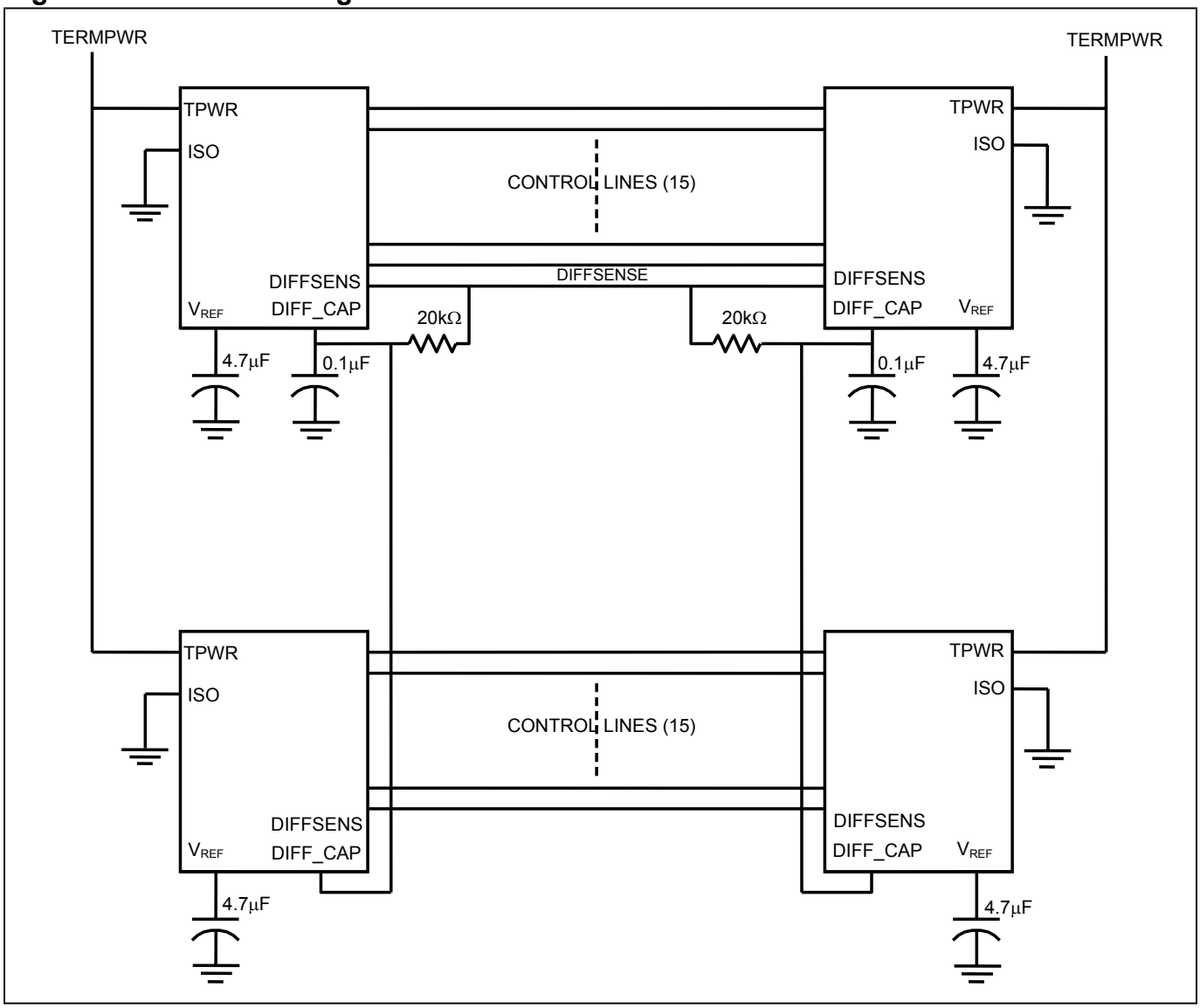


Figure 2. SCSI Bus Configuration



Note: The following terms are used throughout this data sheet:
DIFFSENS: Refers to the SCSI bus signal.
DIFFSENSE: Refers to the DS2125 pin name and internal circuitry capable of driving the DIFFSENS line.
DIFF_CAP: Refers to the DS2125 pin name and internal circuitry relating to monitoring the DIFFSENS line.

DETAILED DESCRIPTION

The DS2125 combines LVD and SE termination with DIFFSENSE sourcing and detection. A bandgap reference is fed into two amplifiers, which creates a 1.25V reference voltage and a 2.85V reference voltage. The control logic determines which of these references are applied to the termination resistors. If the SCSI bus is in LVD mode, the 1.25V reference is used. If the SCSI bus is in SE mode, the 2.85V reference is used. That same control logic switches in/out parallel resistors to change the total termination resistance accordingly. Finally, in SE mode the R_p pins are switched to ground.

The DIFFSENSE circuitry decodes trinary logic. There is one of three voltages on the SCSI control line called DIFFSENS. Two comparators and a NAND gate determine if the voltage is below 0.6V, above 2.15V, or in between, which indicates the mode of the bus as SE, HVD, or LVD, respectively.

The DS2125's DIFF_CAP pin monitors the DIFFSENS line to determine the device's proper operating mode. The DIFFSENSE pin can also drive the SCSI DIFFSENS line to determine the SCSI bus-operating mode. The DS2125 switches to the termination mode that is appropriate for the bus based on the value of the DIFFSENS voltage. These modes are LVD mode, SE mode, and HVD isolation mode.

LVD MODE

A precision laser-trimmed resistor string with two amplifiers provides LVD termination. This configuration yields 105Ω differential and 150Ω common-mode impedance. A 112mV fail-safe bias is maintained when no drivers are connected to the SCSI bus.

SE MODE

When the external driver for a given signal line turns off, the active terminator pulls that signal line to 2.85V (quiescent state). The terminating resistors maintain their 110Ω value.

HVD ISOLATION MODE

The DS2125 identifies that there is an HVD device on the SCSI bus and isolates the termination pins from the bus.

When ISO is pulled high, the termination pins are isolated from the SCSI bus, and V_{REF} remains active. During thermal shutdown, the termination pins are isolated from the SCSI bus, and V_{REF} becomes high impedance. The DIFFSENSE driver is shut down during either of these two events. An internal pulldown resistor assures that the DS2125 is terminating the bus if the ISO pin is left floating.

To ensure proper operation, the TPWR pin should be connected to the SCSI bus TERMPWR line. As with all analog circuitry, the TERMPWR and V_{DD} lines should be bypassed locally. A 2.2µF capacitor and a 0.01µF high-frequency capacitor are recommended between TPWR and ground, and placed as close as possible to the DS2125. The DS2125 should be placed as close as possible to the SCSI connector to minimize signal and power trace length, thereby resulting in less input capacitance and reflections, which can degrade the bus signals.

To maintain the specified regulation, a 4.7µF capacitor is required between the V_{REF} pin and ground of each DS2125. A high-frequency capacitor (0.1µF ceramic recommended) can also be placed on the V_{REF} pin in applications that use fast rise/fall-time drivers. Figure 2 shows a typical SCSI bus configuration.

REFERENCE DOCUMENTS

TITLE	T10 PROJECT DOCUMENT	T10 COMMITTEE FTP LINK	ANSI DOCUMENT NO.
SCSI Parallel Interface 2 (SPI-2)	Project: 1142-M, 1998	ftp://ftp.t10.org/t10/drafts/spi2/spi2r20b.pdf	X3.302:1998
SCSI Parallel Interface 3 (SPI-3)	Project: 1302-D, 1999	ftp://ftp.t10.org/t10/drafts/spi3/spi3r14.pdf	NCITS.336:2000
SCSI Parallel Interface 4 (SPI-4)	Project: 1365-D, 200x	ftp://ftp.t10.org/t10/drafts/spi4/spi4r10.pdf	INCITS.362:2002

SUPPLIERS

SUPPLIER	PHONE	WEBSITE
American National Standards Institute (ANSI)	212-642-4900	www.ansi.org/
Global Engineering Documents	800-854-7179	http://global.ihs.com/

CHIP INFORMATION

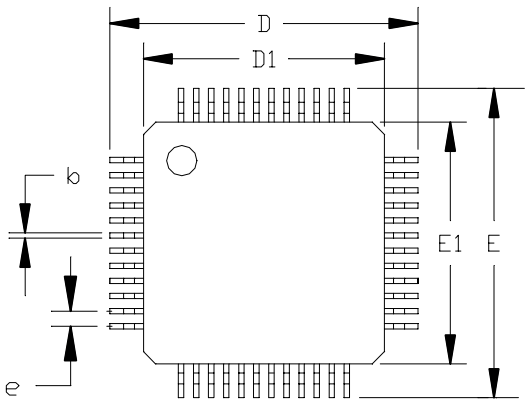
TRANSISTOR COUNT: 8382 MOS and 87 BiPOLAR
PROCESS: BiCMOS
SUBSTRATE CONNECTED TO GROUND

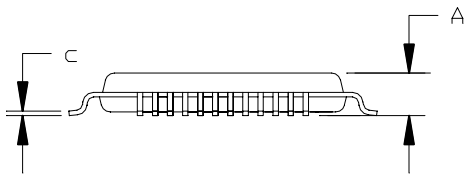
THERMAL INFORMATION

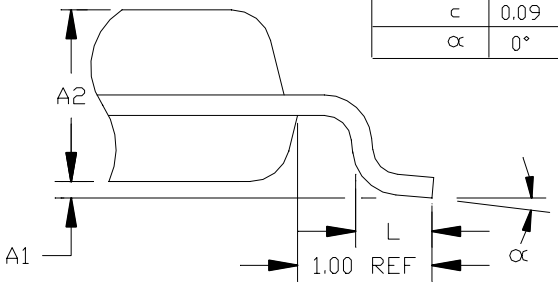
Theta-JA: 65°C/W

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)







JEDEC VARIATION		
	BE	
	48 LEAD	
	MIN.	MAX.
A	---	1.60
A_1	0.05	0.15
A_2	1.35	1.45
D	8.90	9.10
D_1	7.00 BSC.	
E	8.90	9.10
E_1	7.00 BSC.	
e	0.5 BSC.	
L	0.45	0.75
b	0.17	0.27
c	0.09	0.20
α	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

Maxim/Dallas Semiconductor cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim/Dallas Semiconductor product. No circuit patent licenses are implied. Maxim/Dallas Semiconductor reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

© 2006 Maxim Integrated Products • Printed USA

The Maxim logo is a registered trademark of Maxim Integrated Products, Inc. The Dallas logo is a registered trademark of Dallas Semiconductor.