NB2762A

Low Power, Reduced EMI Clock Synthesizer

The NB2762A is a versatile spread spectrum frequency modulator designed specifically for a wide range of clock frequencies. The NB2762A reduces ElectroMagnetic Interference (EMI) at the clock source, allowing system wide reduction of EMI of all clock dependent signals. The NB2762A allows significant system cost savings by reducing the number of circuit board layers, ferrite beads and shielding that are traditionally required to pass EMI regulations.

The NB2762A uses the most efficient and optimized modulation profile approved by the FCC and is implemented by using a proprietary all digital method.

The NB2762A modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation'.

The NB2762A is targeted towards all portable devices with very low power requirements like MP3 players and digital still cameras.

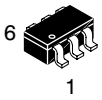
Features

- Generates an EMI Optimized Clocking Signal at the Output
- Integrated Loop Filter Components
- Operates with a 3.3 V / 2.5 V Supply
- Operating Current less than 3.0 mA
- Low Power CMOS Design
- Input Frequency Range: 6.0 MHz to 12 MHz for 2.5 V
  Input Frequency Range: 6.0 MHz to 13 MHz for 3.3 V
- Generates a 1X Low EMI Spread Spectrum clock of the Input Frequency
- Frequency Deviation −1.25% (TYP) @ 10 MHz
- Available in TSOP−6 Package (TSOT−23−6)
- Pb−Free Package is Available

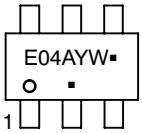
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM*



TSOP−6
(TSOT−23−6)
SN SUFFIX
CASE 318G



E04 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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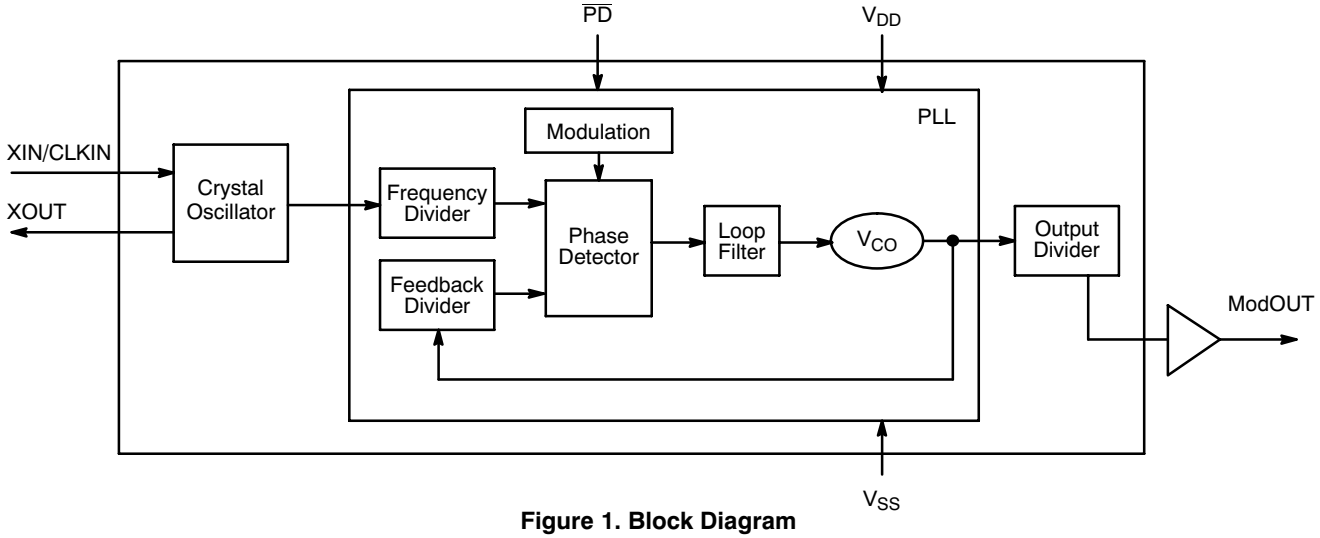


Figure 1. Block Diagram

Table 1. KEY SPECIFICATIONS

Description	Specification
Supply Voltages	V_{DD} = 3.3 V / 2.5 V
Frequency Range For 2.5 V Supply For 3.3 V Supply	6 MHz < CLKIN < 12 MHz 6 MHz < CLKIN < 13 MHz
Cycle−to−Cycle Jitter	200 ps (maximum)
Output Duty Cycle	45/55% (worst case)
Modulation Rate Equation	F_{IN}/256
Frequency Deviation	−1.25% (TYP) @ 10 MHz

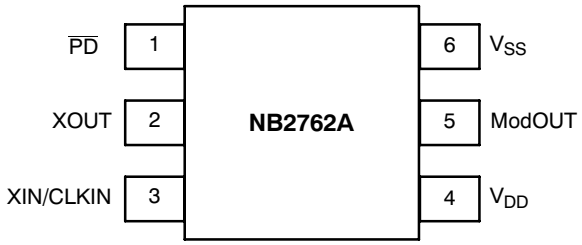


Figure 2. Pin Configuration

Table 2. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	$\overline{PD}$	I	Powerdown control pin. Pull low to enable powerdown mode. Connect to V_{DD} if not used.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	XIN/CLKIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock.
4	V_{DD}	P	Power supply for the entire chip.
5	ModOUT	O	Spread spectrum clock output.
6	V_{SS}	P	Ground connection.

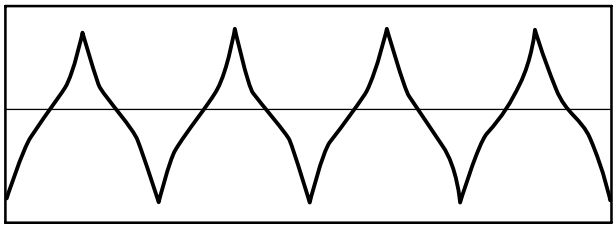


Figure 3. Modulation Profile

Table 3. MAXIMUM RATINGS

Symbol	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	0.5 to +7.0	V
T_{STG}	Storage Temperature	−65 to +125	°C
T_A	Operating Temperature	0 to 70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per MIL−STD−883, Method 3015)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY (Test Conditions: All parameters are measured at room temperature 25°C)

Symbol	Description	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage	GND − 0.3		0.8	V
V_{IH}	Input HIGH Voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input LOW Current			−35	μA
I_{IH}	Input HIGH Current			35	μA
I_{XOL}	XOUT Output LOW Current (@ 0.5 V, V_{DD} = 2.5 V)		3.0		mA
I_{XOH}	XOUT Output HIGH Current (@ 1.8 V, V_{DD} = 2.5 V)		3.0		mA
V_{OL}	Output LOW Voltage (V_{DD} = 2.5 V, I_{OL} = 8.0 mA)			0.6	V
V_{OH}	Output HIGH Voltage (V_{DD} = 2.5 V, I_{OH} = 8.0 mA)	1.8			V
I_{DD}	Static Supply Current (Note 1)			10	μA
I_{CC}	Dynamic Supply Current (2.5 V, 10 MHz, and No Load)		2.0		mA
V_{DD}	Operating Voltage	2.375	2.5	2.625	V
t_{ON}	Powerup Time (first locked cycle after powerup) (Note 2)			5.0	mS
Z_{OUT}	Clock Output Impedance		50		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. $\overline{PD}$ pin is pulled low.
2. V_{DD} and XIN/CLKIN input are stable, $\overline{PD}$ pin is made high from low.

Table 5. AC ELECTRICAL CHARACTERISTICS FOR 2.5 V SUPPLY

Symbol	Description	Min	Typ	Max	Unit
CLKIN	Input Frequency	6.0		12	MHz
ModOUT	Output Frequency	6.0		12	MHz
f_d	Frequency Deviation Input Frequency = 6.0 MHz Input Frequency = 12 MHz			±1.75 ±0.95	%
t_{LH} (Note 3)	Output Rise Time (measured at 0.7 V to 1.7 V)	0.7	1.1	1.4	ns
t_{HL} (Note 3)	Output Fall Time (measured at 1.7 V to 0.7 V)	0.5	0.8	1.0	ns
t_{JC}	Jitter (Cycle−to−Cycle)			200	ps
t_D	Output Duty Cycle	45	50	55	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. t_{LH} and t_{HL} are measured at capacitive load of 15 pF.

Table 6. DC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY (Test Conditions: All parameters are measured at room temperature 25°C)

Symbol	Description	Min	Typ	Max	Unit
V_{IL}	Input LOW Voltage	GND − 0.3		0.8	V
V_{IH}	Input HIGH Voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input LOW Current			−35	μA
I_{IH}	Input HIGH Current			35	μA
I_{XOL}	XOUT Output LOW Current (@ 0.4 V, V_{DD} = 3.3 V)		3.0		mA
I_{XOH}	XOUT Output HIGH Current (@ 2.5 V, V_{DD} = 3.3 V)		3.0		mA
V_{OL}	Output LOW Voltage (V_{DD} = 3.3 V, I_{OL} = 8.0 mA)			0.4	V
V_{OH}	Output HIGH Voltage (V_{DD} = 3.3 V, I_{OH} = 8.0 mA)	2.5			V
I_{DD}	Static Supply Current (Note 4)			10	μA
I_{CC}	Dynamic Supply Current (3.3 V, 10 MHz, and No Load)		3.0		mA
V_{DD}	Operating Voltage	2.7	3.3	3.6	V
t_{ON}	Powerup Time (first locked cycle after powerup) (Note 5)			5.0	mS
Z_{OUT}	Clock Output Impedance		45		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. $\overline{PD}$ pin is pulled low.
5. V_{DD} and XIN/CLKIN input are stable, $\overline{PD}$ pin is made high from low.

Table 7. AC ELECTRICAL CHARACTERISTICS FOR 3.3 V SUPPLY

Symbol	Description	Min	Typ	Max	Unit
CLKIN	Input Frequency	6.0		13	MHz
ModOUT	Output Frequency	6.0		13	MHz
f_d	Frequency Deviation Input Frequency = 6.0 MHz Input Frequency = 13 MHz			±1.75 ±0.89	%
t_{LH} (Note 6)	Output Rise Time (measured at 0.8 V to 2.0 V)	0.5	1.0	1.4	ns
t_{HL} (Note 6)	Output Fall Time (measured at 2.0 V to 0.8 V)	0.4	0.9	1.2	ns
t_{JC}	Jitter (Cycle−to−Cycle)			200	ps
t_D	Output Duty Cycle	45	50	55	%

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. t_{LH} and t_{HL} are measured at capacitive load of 15 pF.

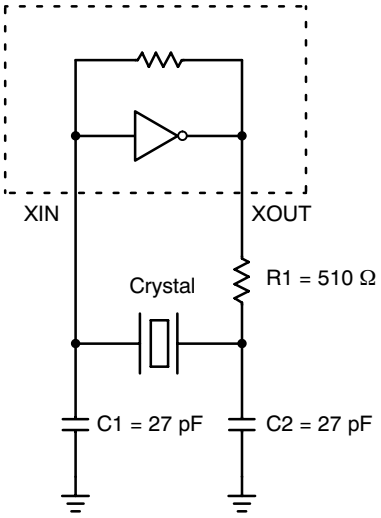


Figure 4. Typical Crystal Oscillator Circuit

Table 8. TYPICAL CRYSTAL SPECIFICATIONS

Fundamental AT Cut Parallel Resonant Crystal	
Nominal Frequency	8.0 MHz
Frequency Tolerance	±50 ppm or better at 25°C
Operating Temperature Range	−25°C to +85°C
Storage Temperature	−40°C to +85°C
Load Capacitance	18 pF
Shunt Capacitance	7 pF Maximum
ESR	25 Ω

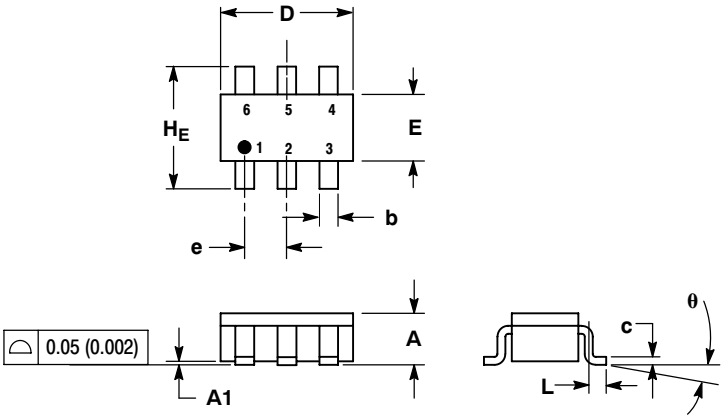
ORDERING INFORMATION

Device	Marking	Temperature Range	Package	Shipping†	Availability
NB2762ASNR2	E04	0°C – 70°C	TSOP−6 (TSOT−23−6)	2500 Tape & Reel	*Now*
NB2762ASNR2G	E04	0°C – 70°C	TSOP−6 (TSOT−23−6) (Pb−Free)	2500 Tape & Reel	*Contact Sales Representative*

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

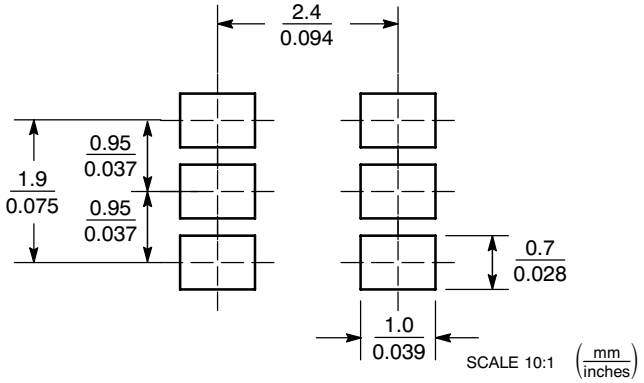
TSOP−6
CASE 318G−02
ISSUE S



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

This product utilizes US Patent #6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, Dated 11−11−2003.

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