PRELIMINARY

MX27C4111

4M-BIT [512K x8/256K x16] CMOS EPROM WITH PAGE MODE

FEATURES

- With Page Mode function, 8-word/16-byte page
- 512K x 8 or 256K x 16 organization
- +12.5V programming voltage
- Fast access time: 90/100/120/150 ns
- Page mode access time 50/60/75 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 60mA
- Standby current: 100uA
- Package type:
  - 40 pin plastic DIP
  - 40 pin SOP

GENERAL DESCRIPTION

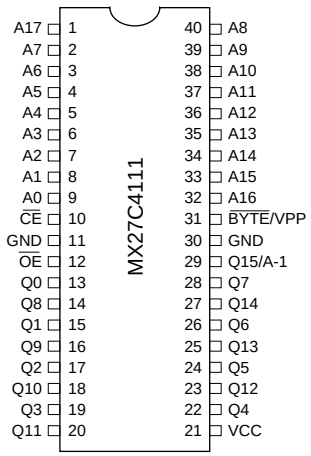
The MX27C4111 is a 4M-bit, One Time Programmable Read Only Memory with page mode. It is organized as 512K x 8 or 256K x 16, operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27C4111 supports a intelligent fast programming algorithm which can result in programming time of less than two minutes.

MX27C4111 provides Page Read Access Mode which can greatly reduce the read access time. Normal read access time and Page Mode read access time is as fast as 90/50ns. It is designed to be compatible with all microprocessors and similar applications in which high perofmrance, large bit storage and simple interfacing are important design considerations.

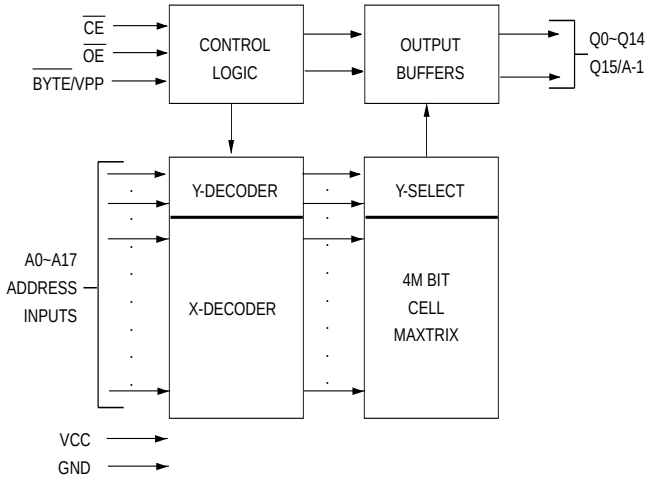
This EPROM is packaged in industry standard 40 pin dual-in-line packages and 40 pin SOP packages.

PIN CONFIGURATIONS

PDIP/SOP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q14	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection/Program Supply Voltage
Q15/A-1	Q15(Word mode)/LSB addr. (Byte mode)
VCC	Power Supply Pin (+5V)
GND	Ground Pin

TRUTH TABLE OF $\overline{BYTE}$ FUNCTION

$\overline{BYTE}$ MODE($\overline{BYTE}$ = GND)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q7	SUPPLY CURRENT
H	X	X	Non selected	High Z	Standby(ICC2)
L	H	X	Non selected	High Z	Operating(ICC1)
L	L	A-1 input	Selected	DOUT	Operating(ICC1)

WORD MODE($\overline{BYTE}$ = VCC)

$\overline{CE}$	$\overline{OE}$	Q15/A-1	MODE	Q0-Q14	SUPPLY CURRENT
H	X	High Z	Non selected	High Z	Standby(ICC2)
L	H	High Z	Non selected	High Z	Operating(ICC1)
L	L	DOUT	Selected	DOUT	Operating(ICC1)

NOTE : X = H or L

FUNCTIONAL DESCRIPTION

THE PROGRAMMING OF THE MX27C4111

When the MX27C4111 is delivered, or it is erased, the chip has all 4M bits in the "ONE" or HIGH state. "ZEROs" are loaded into the MX27C4111 through the procedure of programming.

For programming, the data to be programmed is applied with 16 bits in parallel to the data pins.

VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP. When programming an MXIC EPROM, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{OE}$ = VIH (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the $\overline{CE}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27C4111's in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27C4111 may be common. A TTL low-level program pulse applied to an MX27C4111 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V will program the MX27C4111. A high-level $\overline{CE}$ input inhibits the other MX27C4111s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ at VIL, $\overline{CE}$ at VIH, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25℃ ± 5℃ ambient temperature range that is required when programming the MX27C4111.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27C4111, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q15) defined as the parity bit.

READ MODE

The MX27C4111 provides page mode with 8 words/16 bytes per page. In order to get the benefit of fast page read, the user should keep chip enable($\overline{CE}$) low and toggle address A0~A2 in word mode or A-1~A2 in byte mode. Page Read access time(tPA) is equal to the delay from address stable to data output. It is twice as fast as normal tACC and is highly recommended.

WORD-WIDE MODE

With $\overline{BYTE}$/VPP at VCC ± 0.2V outputs Q0-7 present data Q0-7 and outputs Q8-15 present data Q8-15, after $\overline{CE}$ and $\overline{OE}$ are appropriately enabled.

BYTE-WIDE MODE

With $\overline{BYTE}$/VPP at GND ± 0.2V, outputs Q8-15 are tri-stated. If Q15/A-1 = VIH, outputs Q0-7 present data bits Q8-15. If Q15/A-1 = VIL, outputs Q0-7 present data bits Q0-7.

STANDBY MODE

The MX27C4111 has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX27C4111 also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

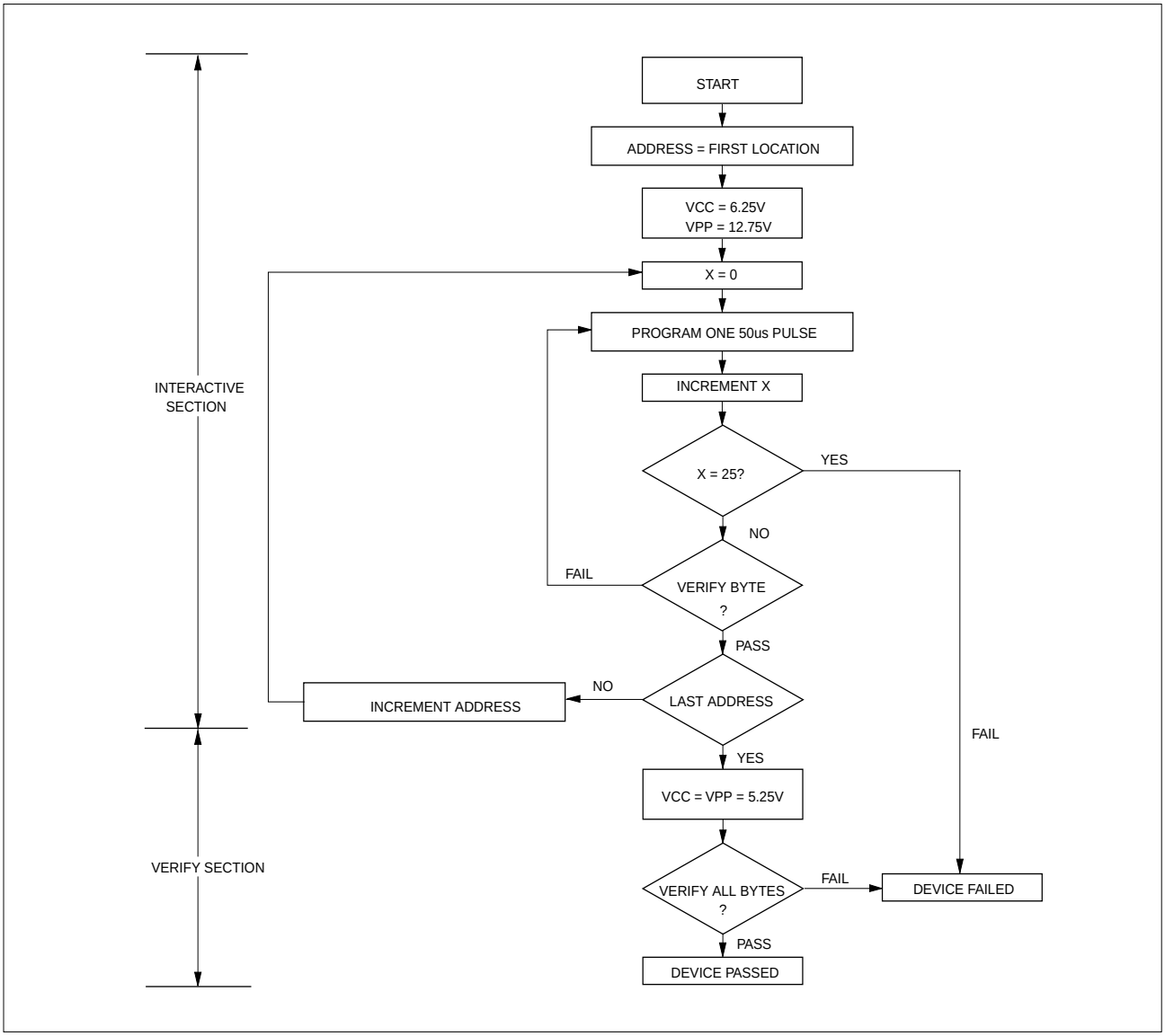
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

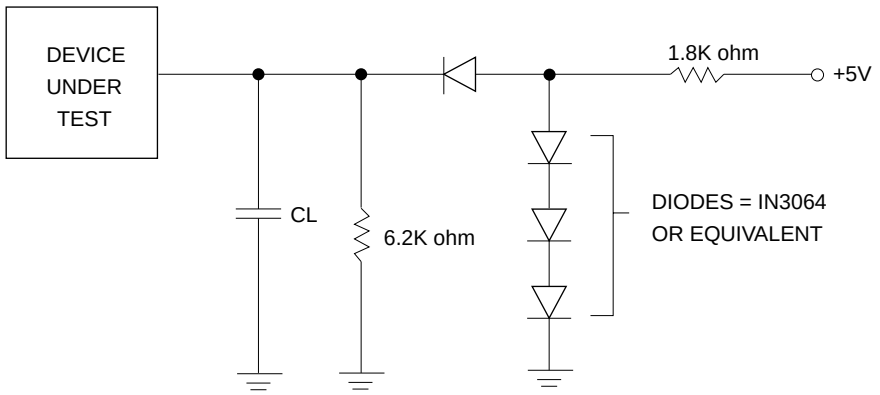
MODE	$\overline{CE}$	$\overline{OE}$	A9	A0	Q15/A-1	$\overline{BYTE}$/VPP(5)	Q8-14	Q0-7
Read (Word)	VIL	VIL	X	X	Q15 Out	VCC	Q8-14 Out	Q0-7 Out
Read (Upper Byte)	VIL	VIL	X	X	VIH	GND	High Z	Q8-15 Out
Read (Lower Byte)	VIL	VIL	X	X	VIL	GND	High Z	Q0-7 Out
Output Disable	VIL	VIH	X	X	High Z	X	High Z	High Z
Standby	VIH	X	X	X	High Z	X	High Z	High Z
Program	VIL	VIH	X	X	Q15 In	VPP	Q8-14 In	Q0-7 In
Program Verify	VIH	VIL	X	X	Q5 Out	VPP	Q8-14 Out	Q0-7 Out
Program Inhibit	VIH	VIH	X	X	High Z	VPP	High Z	High Z
Manufacturer Code(3)	VIL	VIL	VH	VIL	0B	VCC	00H	C2H
Device Code(3)	VIL	VIL	VH	VIH	1B	VCC	38H	00H

NOTES:
1. VH = 12.0V ± 0.5V
2. X = Either VIH or VIL
3. A1 - A8, A10 - A17 = VIL (For auto select)
4. See DC Programming Characteristics for VPP voltages.
5. $\overline{BYTE}$/VPP is intended for operation under DC Voltage conditions only.
6. Manufacture code = 00C2H
   Device code = B800H

FIGURE 1. FAST PROGRAMMING FLOW CHART

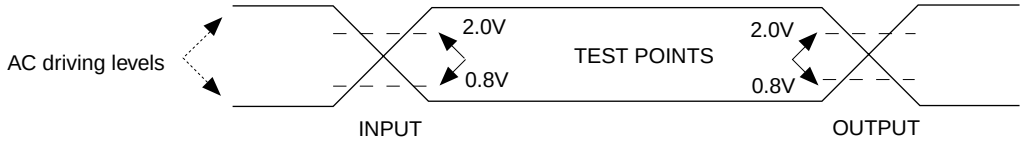


SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V.
Input pulse rise and fall times are < 20ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC Operating Condition for Read Operation

		MX27C4111			
		-90	-10	-12	-15
Operating Temperature	Commercial	0℃ to 70℃	0℃ to 70℃	0℃ to 70℃	0℃ to 70℃
Vcc POwer Supply		5V ± 5%	5V ± 10%	5V ± 10%	5V ± 10%

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
ICC3	VCC Power-Down Current		100	uA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		1.5	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		60	mA	$\overline{CE}$ = VIL, f=5MHz, Iout = 0mA
IPP	VPP Supply Current Read		10	uA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS

		27C4111-90		27C4111-10		27C4111-12		27C4111-15			
Symbol	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		100		120		150	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		90		100		120		150	ns	$\overline{OE}$ = VIL
tPA	Page Address to Output Delay		50		50		60		75	ns	$\overline{CE}$ = $\overline{OE}$ =VIL
tOE	Output Enable to Output Delay		45		45		50		65	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	30	0	35	0	50	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0	0	0		0		0		ns	
tBHA	$\overline{BYTE}$ Access Time		90		100		120		150	ns	
tOHB	$\overline{BYTE}$ Output Hold Time	0		0		0		0		ns	
tBHZ	$\overline{BYTE}$ Output Delay Time		70		70		70		70	ns	
tBLZ	$\overline{BYTE}$ Output Set Time	10		10		10		10		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

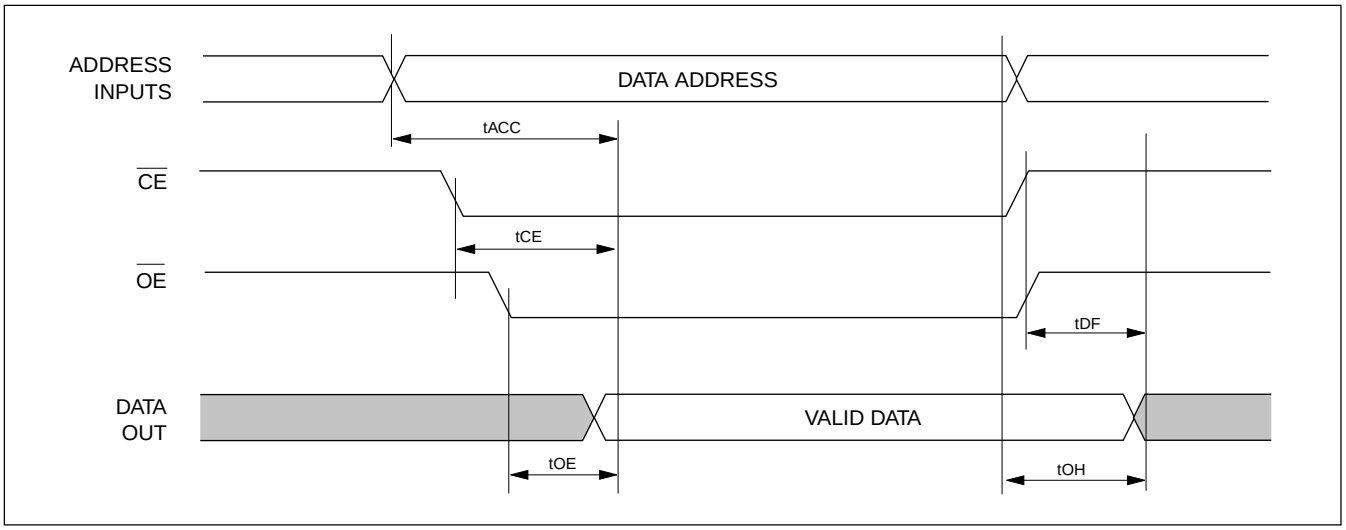
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.40mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

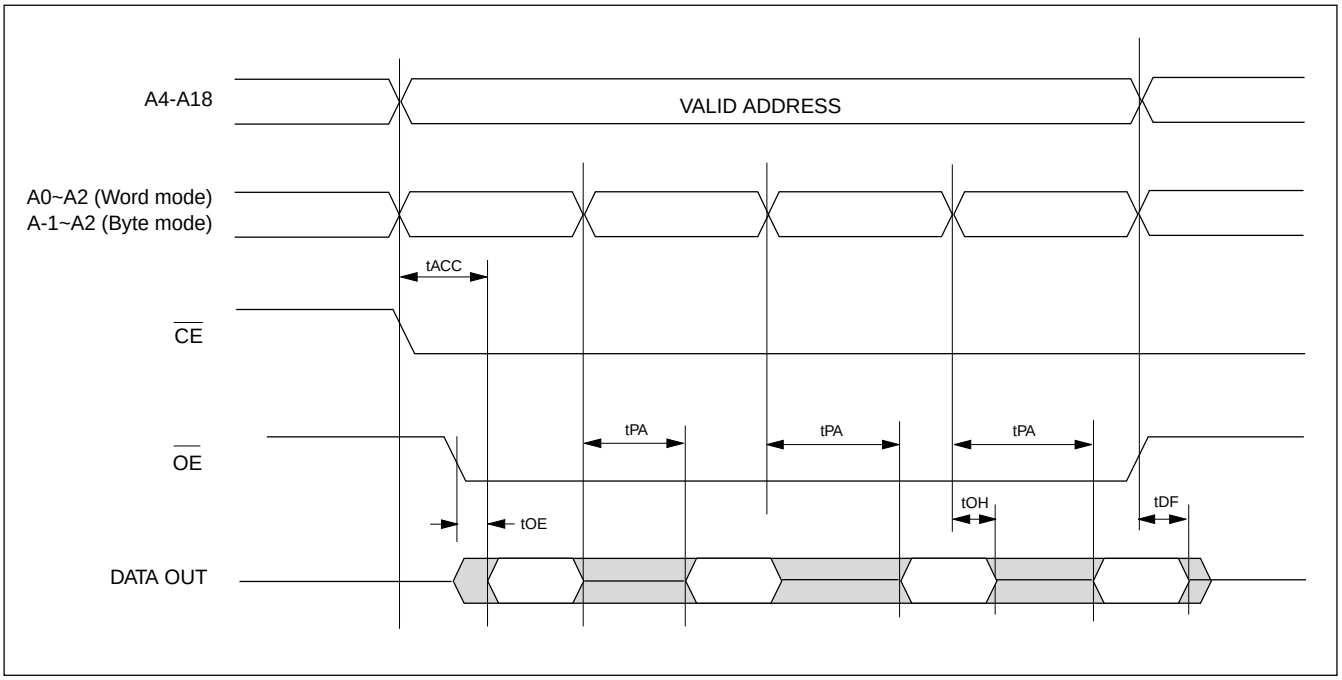
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
tAS	Address Setup Time	2.0		us	
tOES	$\overline{OE}$ Setup Time	2.0		us	
tDS	Data Setup Time	2.0		us	
tAH	Address Hold Time	0		us	
tDH	Data Hold Time	2.0		us	
tDFP	Chip Enable to Output Float Delay	0	130	ns	
tVPS	$\overline{BYTE}$/VPP Setup Time	2.0		us	
tPW	$\overline{CE}$ initial Program Pulse Width	95	105	us	
tVCS	VCC Setup Time	2.0		us	
tOE	Data valid from $\overline{OE}$		150	ns	

WAVEFORMS

NORMAL READ CYCLE(WORD MODE)

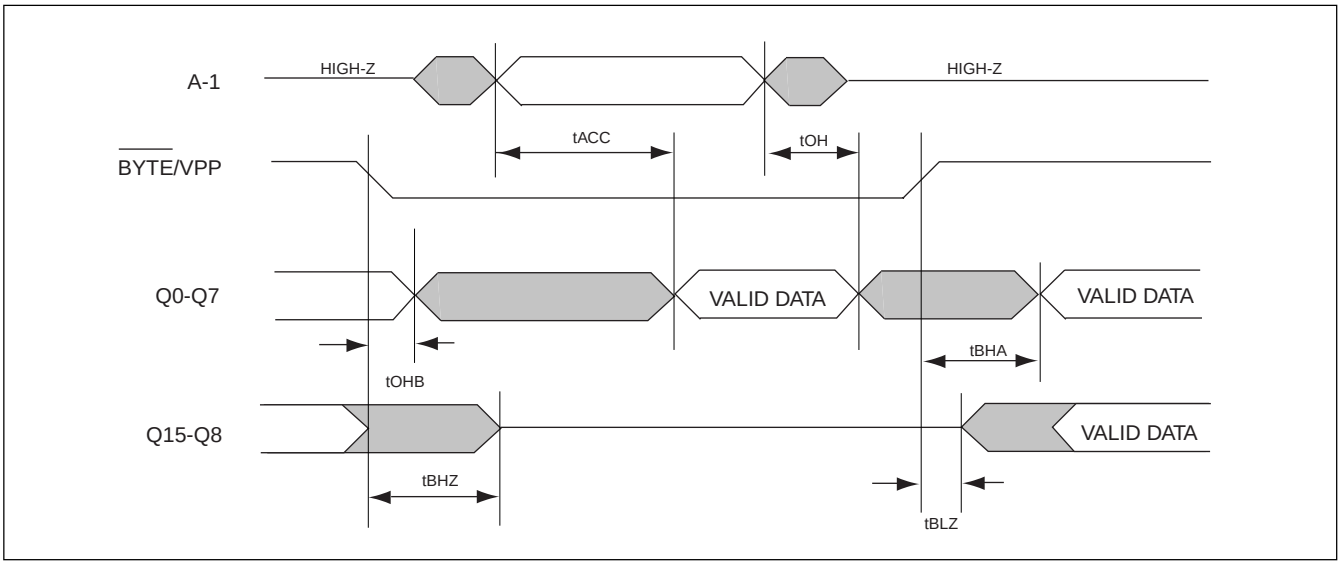


PAGE MODE READ CYCLE

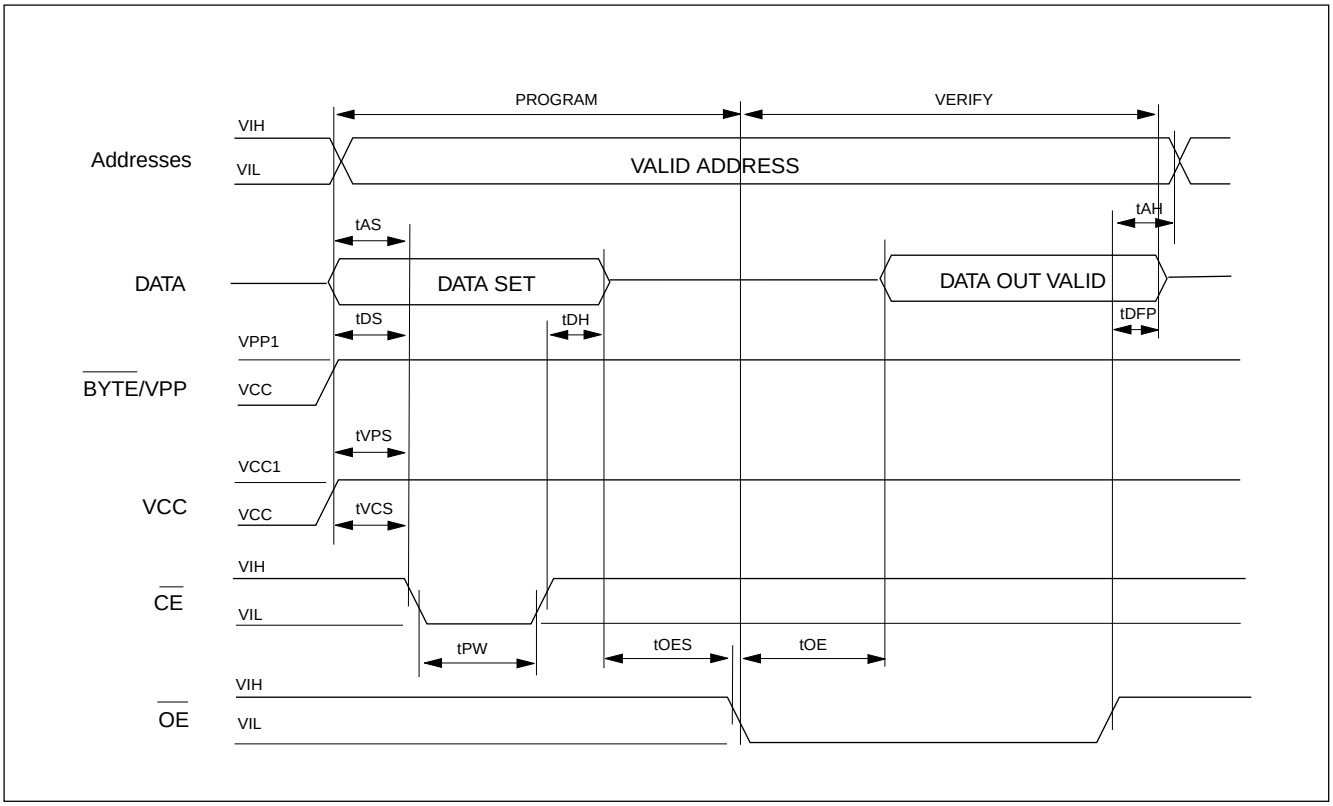


WAVEFORMS

NORMAL READ CYCLE(BYTE MODE)



FAST PROGRAMMING ALGORITHM WAVEFORMS



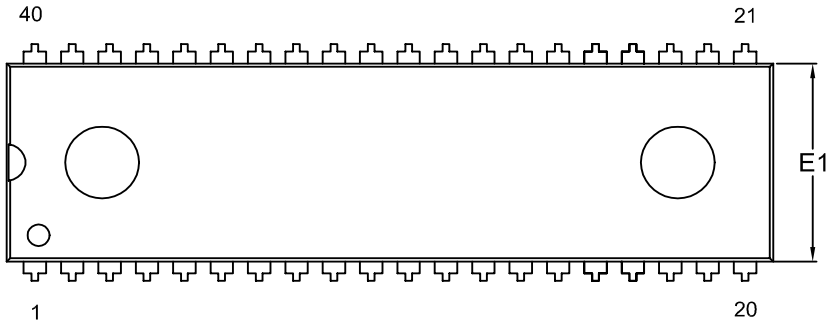
ORDERING INFORMATION

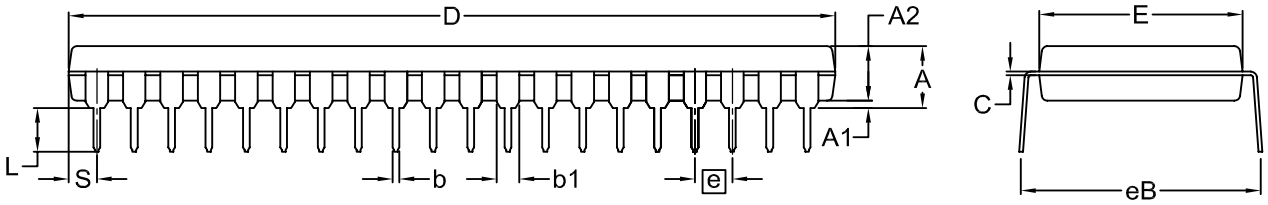
PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX27C4111MC-90	90	60	100	40 Pin SOP(ROM pin out)
MX27C4111MC-10	100	60	100	40 Pin SOP(ROM pin out)
MX27C4111MC-12	120	60	100	40 Pin SOP(ROM pin out)
MX27C4111MC-15	150	60	100	40 Pin SOP(ROM pin out)
MX27C4111PC-90	90	60	100	40 Pin PDIP(ROM pin out)
MX27C4111PC-10	100	60	100	40 Pin PDIP(ROM pin out)
MX27C4111PC-12	120	60	100	40 Pin PDIP(ROM pin out)
MX27C4111PC-15	150	60	100	40 Pin PDIP(ROM pin out)

PACKAGE INFORMATION

Title: **Package Outline for PDIP 40L(600MIL)**



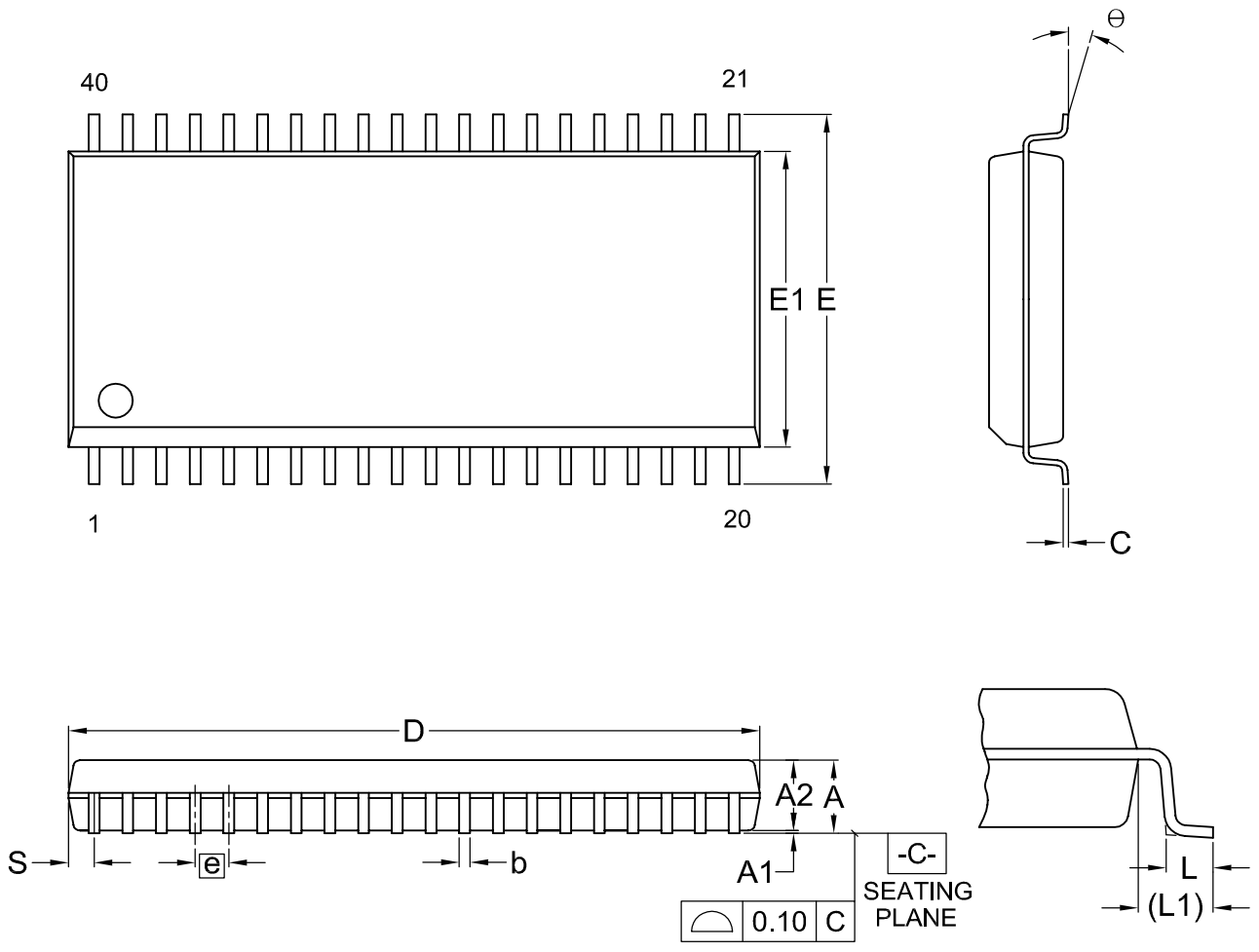


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	—	0.51	3.73	0.38	1.14	0.20	51.94	15.11	13.84		15.75	2.92	1.65
	Nom.	—	0.64	3.94	0.46	1.27	0.25	52.07	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.20	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.020	0.147	0.015	0.045	0.008	2.045	0.595	0.545		0.620	0.115	0.065
	Nom.	---	0.025	0.155	0.018	0.050	0.010	2.050	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.055	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.4	5				07-03-'02

Title: **Package Outline for SOP 40L (450MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	25.93	13.92	11.17		0.56	1.20	0.84	0
	Nom.	---	0.15	2.69	0.41	0.20	26.06	14.12	11.30	1.27	0.76	1.40	0.97	5
	Max.	3.00	0.20	2.80	0.51	0.25	26.19	14.32	11.43		0.96	1.60	1.10	8
Inch	Min.	---	0.004	0.102	0.014	0.006	1.021	0.548	0.440		0.022	0.047	0.033	0
	Nom.	---	0.006	0.106	0.016	0.008	1.026	0.556	0.445	0.050	0.030	0.055	0.038	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.031	0.564	0.450		0.038	0.063	0.043	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404.1	3	MO-099			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
2.0	1) Eliminate Interactive Programming Mode		6/14/1997
	2) 40-CDIP package quartz lens, change to square shape.		
2.1	IPP 100uA --> 10uA		8/07/1997
2.2	Add 100ns speed grade.		1/31/1998
2.3	Add 90ns speed grade.		4/07/1998
2.4	90ns speed grade VCC=5V±10% --> VCC=5V±5%		5/06/1998
2.5	Cancel ceramic DIP package type	P1,3,12,13	MAR/02/2000
2.6	Cancel "Ultraviolet Erasable" wording in General Description	P1	AUG/20/2001
	To modify Package Information	P12~13	
2.7	To modify Package Information	P12~13	NOV/19/2002

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