Half-Bridge N-Channel MOSFET Driver With Break-Before-Make

FEATURES

- 5-V Gate Drive
- Undervoltage Lockout
- Sub 1-Ω Gate Drivers
- Internal Bootstrap Diode
- Drive MOSFETs In 4.5- to 30-V Systems
- Switching Frequency: 250 kHz to 1 MHz
- Synchronous Enable/Disable Option

APPLICATIONS

- Multi-Phase DC/DC
- High Current Synchronous Buck Converters
- High Frequency Synchronous Buck Converters
- Asynchronous-to-Synchronous Adaptations
- Mobile Computer DC/DC Converters
- Desktop Computer DC/DC Converters

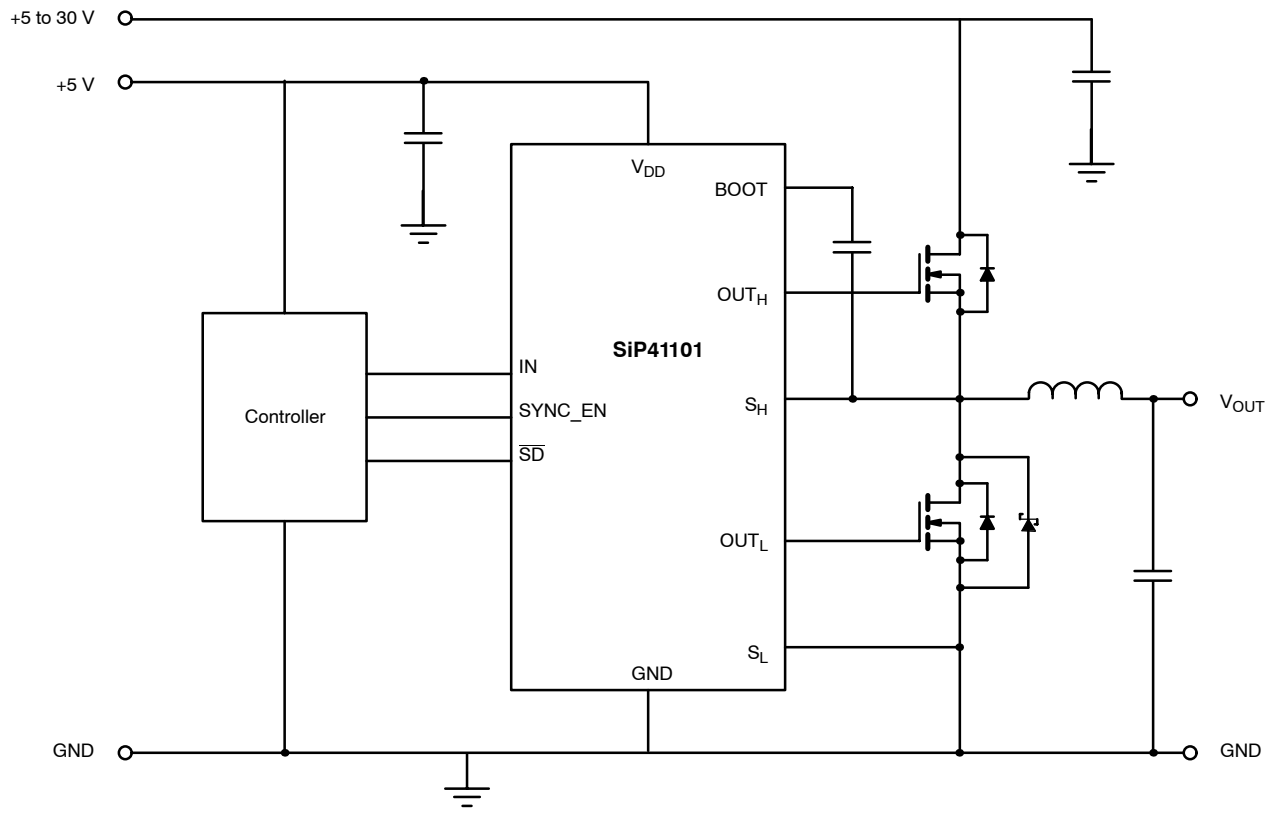
DESCRIPTION

The SiP41101 is a high speed half-bridge driver, with make-before-break, for use in high frequency, high current multiphase dc-to-dc power supplies for supply voltages as high as 30 V. It is designed to operate at frequencies up to 1 MHz. The high-side driver is bootstrapped to allow driving an n-channel high-side MOSFET. The bootstrap diode is internal. The output drivers provide currents up to 4 A, allowing use of low $r_{DS(on)}$ power MOSFETs.

The SiP41101 comes with internal break-before-make circuitry to prevent shoot-through current in the external MOSFETs. The $\overline{SD}$ control pin is provided to enable the drivers. A Synchronous Enable control pin is provided to disable the the low-side or synchronous MOSFET to maximize efficiency under low output current conditions.

The SiP41101 is available in a 16-pin TSSOP package for operation over the industrial temperature range of -40 to 85°C.

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD} . . . . . 7 V
V_{IN} . . . . . -0.3 V to V_{DD} + 0.3 V
V_{SH} . . . . . 30 V
V_{BOOT} . . . . . V_{SH} + 7 V
Storage Temperature . . . . . -40 to 150°C
Operating Junction Temperature . . . . . 125°C

Power Dissipation[a]
TSSOP-16 . . . . . 925 mW
Thermal Impedance (Θ_{JA})$_a$
TSSOP-16 . . . . . 135°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE (ALL VOLTAGES REFERENCED TO GND = 0 V)

V_{DD} . . . . . 4.5 V to 5.5 V
V_{BOOT} . . . . . 4.5 V to 30 V
C_{BOOT} . . . . . 100 nF to 1 µF
Operating Temperature Range . . . . . -40 to 85°C

SPECIFICATIONS[a]

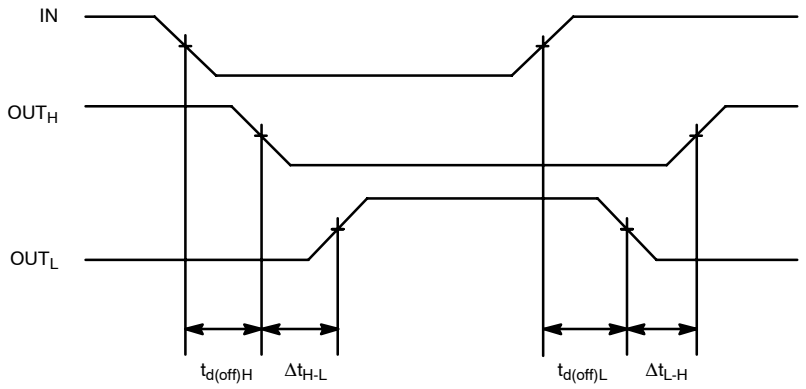
Parameter	Symbol	Test Conditions Unless Specified V_{DD} = 4.5 to 5.5 V, V_{BOOT} = 4.5 to 30 V, T_A = -40 to 85°C	Limits Min[a]	Typ[b]	Max[a]	Unit
Power Supplies						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	f_{IN} = 300 kHz, $\overline{SD}$ = H, Sync_en = H see Figure 1		25	40	mA
Quiescent Current	I_{DDQ}	IN = L, $\overline{SD}$ = H, Sync_en = H, No Load		1.4	2.5	µA
Reference Voltage						
Break-Before-Make	V_{BBM}	V_{DD} = 5.5 V		2.5		V
Logic Inputs — IN, Sync En, $\overline{SD}$						
Input High	V_{IH}		2.5			V
Input Low	V_{IL}				1.0	
Undervoltage Lockout						
V_{DD} Undervoltage	V_{UVL}	V_{DD} Rising	2.5	3.6	4.4	V
Undervoltage Hysteresis	V_{HYST}			400		mV
Bootstrap Diode						
Forward Voltage	V_F	I_F = 10 mA		0.65		V
MOSFET Drivers						
High-Side Drive Current[c]	$I_{PKH(source)}$	V_{BOOT} - V_{SH} = 4.5 V, V_{OUTH}-V_{SA}=2.25V		3.0		A
	$I_{PKH(sink)}$			3.0		
Low-Side Drive Current[c]	$I_{PKL(source)}$	V_{DD} = 4.5 V, V_{OUTL}=2.25V		4.1		
	$I_{PKL(sink)}$			4.1		
High-Side Driver Impedance	$R_{DH(source)}$	V_{DD} = 4.5 V, S_H = GND		0.75	1.3	Ω
	$R_{DH(sink)}$			0.75	1.3	
Low-Side Driver Impedance	$R_{DL(source)}$	V_{DD} = 4.5 V		0.55	1.1	
	$R_{DL(sink)}$			0.55	1.1	

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V_{DD} = 4.5 to 5.5 V, V_{BOOT} = 4.5 to 30 V, T_A = -40 to 85°C	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
MOSFET Drivers						
High-Side Rise Time[c]	t_{rH}	10% - 90%		15		ns
High-Side Fall Time[c]	t_{fH}	90% - 10%		15		
High-Side Propagation Delay[c]	$t_{d(off)H}$	50% - 50%		25		
	$\Delta tH\text{-}L$			5		
Low-Side Rise Time[c]	t_{rL}	10% - 90%		25		
Low-Side Fall Time[c]	t_{fL}	90% - 10%		15		
Low-Side Propagation Delay[c]	$t_{d(off)L}$	50% - 50%		10		
	$\Delta tL\text{-}H$			25		

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum (-40° to 85°C).
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design.

TIMING WAVEFORMS



TEST SETUP

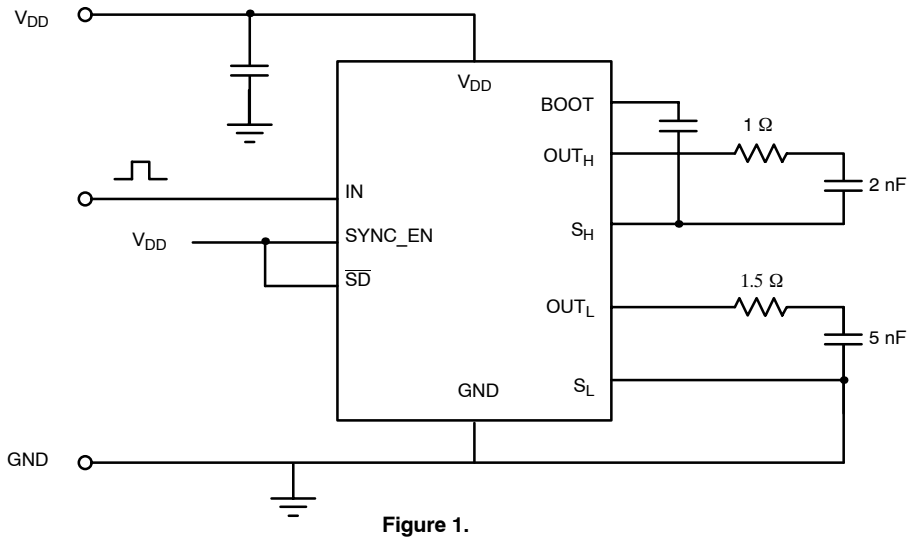
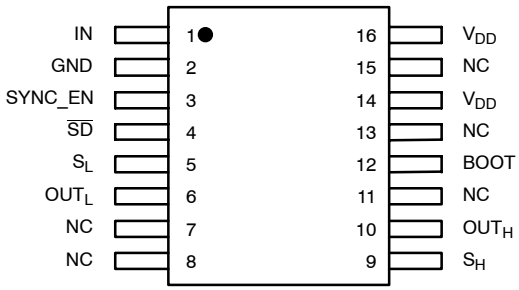


Figure 1.

PIN CONFIGURATION, ORDERING INFORMATION, AND TRUTH TABLE

SiP41101 (TSSOP-16)



Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Marking**
SiP41101DQ-T1	-40 to 85°C	41101

Eval Kit	Temperature Range
SiP41101DB	-40 to 85°C

TRUTH TABLE				
$\overline{SD}$	SYNC_EN	IN	OUT_H	OUT_L
H	H	L	L	H
H	H	H	H	L
H	L	L	L	L
H	L	H	H	L
L	X	X	L	L

PIN DESCRIPTION		
Pin	**Name**	**Function**
1	IN	Input signal to the MOSFET drivers
2	GND	Ground
3	SYNC_EN	Synchronous MOSFET enable
4	$\overline{SD}$	Shutdown
5	S_L	Connection to source of low-side MOSFET
6	OUT_L	Synchronous or low-side MOSFET gate drive
7, 8, 11, 13, 15	NC	No Connect
9	S_H	Connection to source of high-side MOSFET
10	OUT_H	Control or high-side MOSFET gate drive
12	BOOT	Connection for the bootstrap capacitor
14, 16	V_{DD}	+5-V supply

FUNCTIONAL BLOCK DIAGRAM

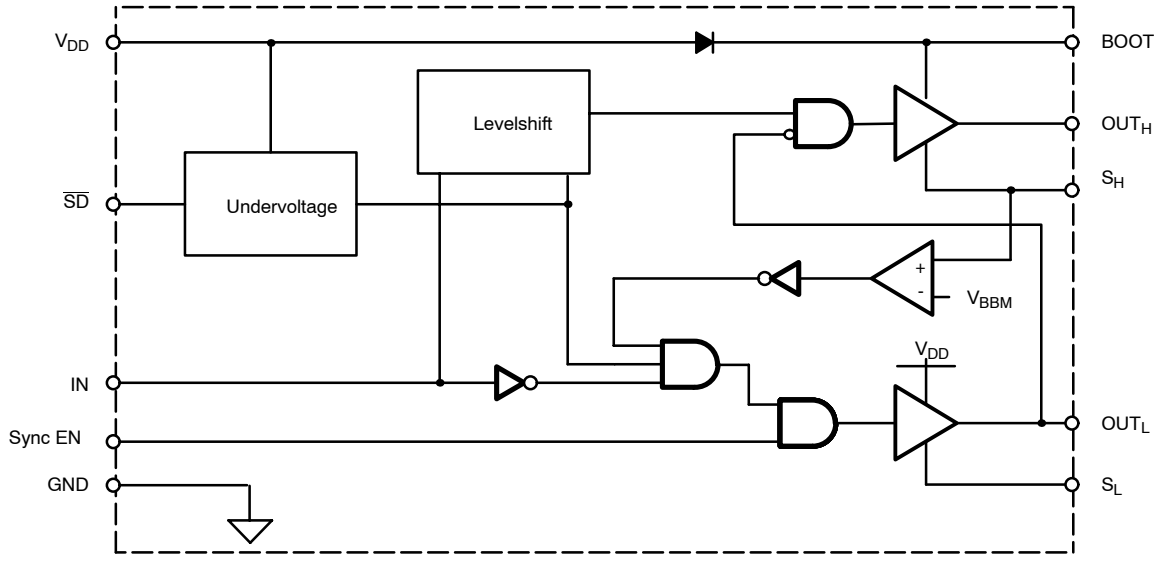


Figure 2.

DETAILED OPERATION

Break-Before-Make Function

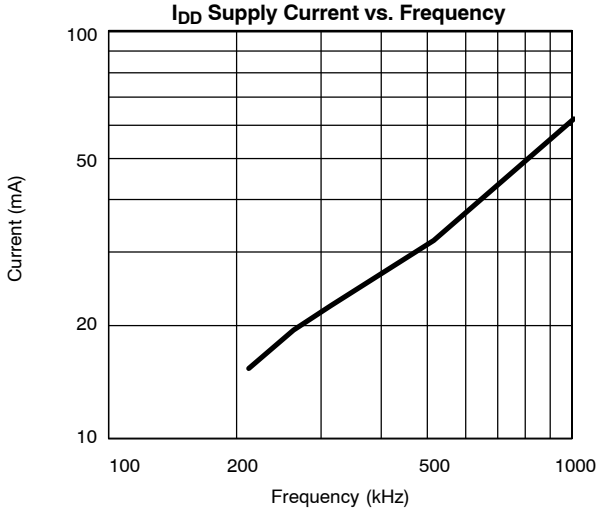
The SiP41101 has an internal break-before-make function to ensure that both high-side and low-side MOSFETs are not turned on at the same time. The high-side drive (OUT_H) will not turn on until the low-side gate drive voltage (measured at the OUT_L pin) is less than V_{BBM}, thus ensuring that the low-side MOSFET is turned off. The low-side drive (OUT_L) will not turn on until the voltage at the MOSFET half-bridge output (measured at the S_L pin) is less than V_{BBM}, thus ensuring that the high-side MOSFET is turned

Under Voltage Lockout Function

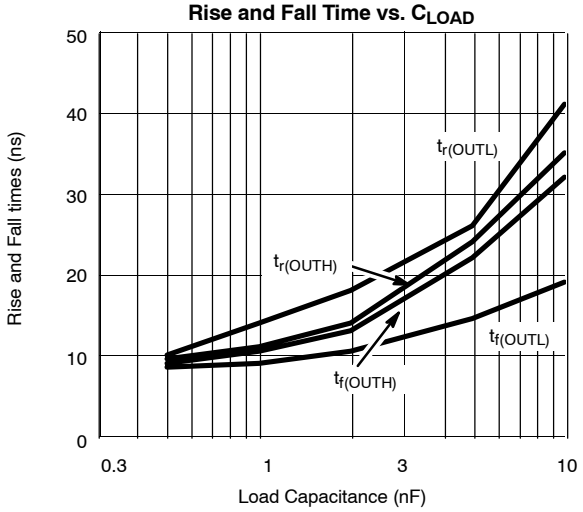
The SiP41101 has an internal under-voltage lockout feature to prevent driving the MOSFET gates when the supply voltage (at V_{DD}) is less than the under-voltage lockout specification (V_{UVL}). This prevents the output MOSFETs from being turned on without sufficient gate voltage to ensure they are fully on. There is hysteresis included in this feature to prevent lockout from cycling on and off.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

I_{DD} Supply Current vs. Frequency

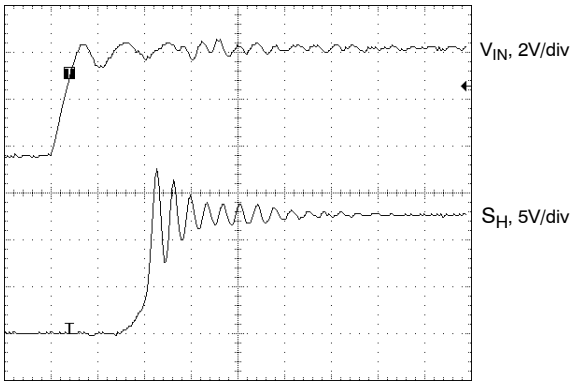


Rise and Fall Time vs. C_{LOAD}



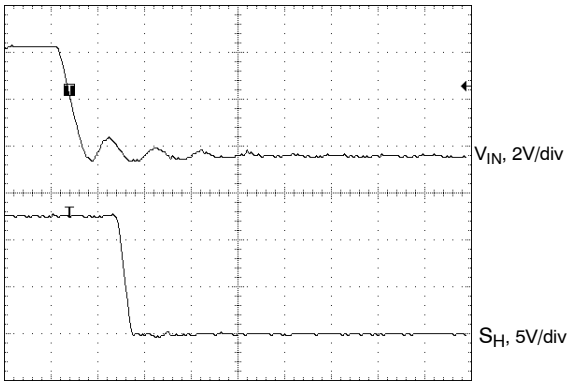
TYPICAL WAVEFORMS

V_{IN} Rising vs. S_H



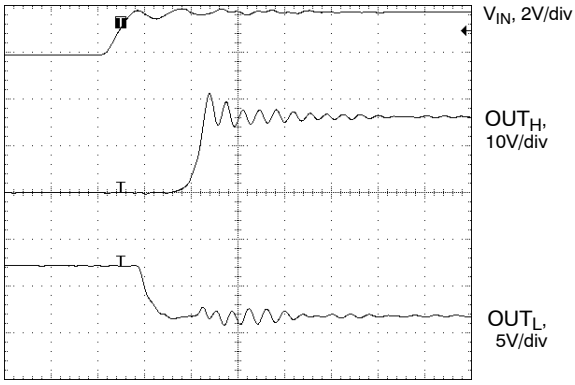
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V_{IN} Falling vs. S_H



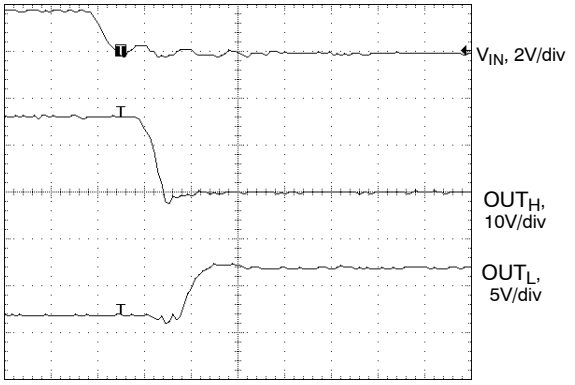
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V_{IN} Rising vs. OUT_H and OUT_L



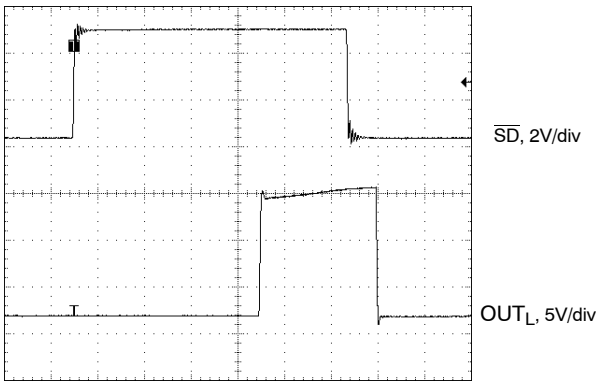
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V_{IN} Falling vs. OUT_H and OUT_L



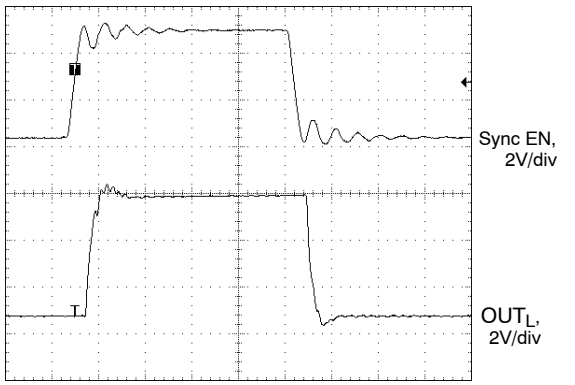
25ns/div

$\overline{SD}$ vs. OUT_L



400 ns/div

Sync EN vs. OUT_L



50ns/div