Ordering number : EN4520

CMOS LSI

SANYO No. 4520

LC7868E, 7869E

Digital Signal Processor for Compact Disc Players

Overview

The LC7868E and the LC7869E are CMOS LSIs for signal processing and servo control in compact disk players, laser disk players, and CD-V and CD-I products. Only the digital filtering blocks differ between the LC7868E and the LC7869E. These products perform signal processing such as demodulation of the EFM signal from the optical pickup, de-interleaving, error detection and correction, and digital filtering that can contribute to end product cost reduction. Furthermore, these products also process commands from the system microprocessor directed at the servo system. These products also support direct interface with the Sanyo LC78815 and LC78816 serial input D/A converters.

Functions

- HF signals that are input are sliced at an accurate level, converted to EFM signals, and undergo phase-comparison with VCO for PLL playback at an average of 4.3218 MHz.
- Through external connection of a 16.9344 MHz crystal oscillator, all required timing signals can be generated on-chip, including the standard clock.
- Frame phase difference signals made from the playback clock and the reference clock can control the speed of the disc motor.
- Performs detection, protection, and interleaving of frame synchronization signals, ensuring stable data reading.
- Demodulates EFM signals and performs conversion to 8-bit symbol data.
- Separates subcodes from EFM demodulation signals for output to an external microprocessor.
- After CRC checking, Q subcode signals are output to the microprocessor by the serial I/O interface (LSB-first output selectable).
- On-chip RAM performs buffering for EFM demodulation signals, as well as absorbing up to ±4 frames of jitter due to fluctuations in the speed of disc rotation.
- Performs unscrambling and deinterleaving for rearranging the EFM demodulation signals into the specified sequence.
- Performs detection and correction of error signals, as well as error flag processing (double C1 and double C2 error correction system).
- The LC7868/69 sets the C2 flags by referencing the C1 flags and the C2 check result, and uses the C2 flags for signal interpolation and muting. The interpolation circuit performs a fourfold interpolation. The system forces the data to zero when the C2 flags are set four times in a row.
- Performs functions such as track jump, focus start, disc motor start and stop, muting on and off, and track count when the appropriate command is input from the microprocessor (8-bit serial input).
- Features on-chip digital out.
- Can perform the desired track counting. High-speed access is possible.
- Uses zero cross-muting.
- Oversampling and digital filtering provide a D/A converter signal with improved output data continuity LC7868E (4fsDF), LC7869E (8fsDF).
- Supports all types of D/A conversion.
- Built-in digital deemphasis
- Features on-chip digital level meter and peak meter functions.
- Supports bilingual function.

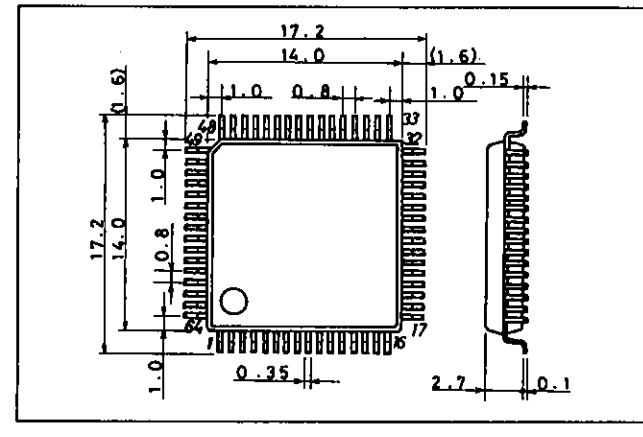
Features

- Compact and space-saving 64-pin QFP package
- Silicon-gate CMOS design (low power dissipation)
- Single 5 V power supply (suitable for portable sets)
- DEMO pin for improved operability in adjustment

Package Dimensions

unit: mm

3159-QFP64E



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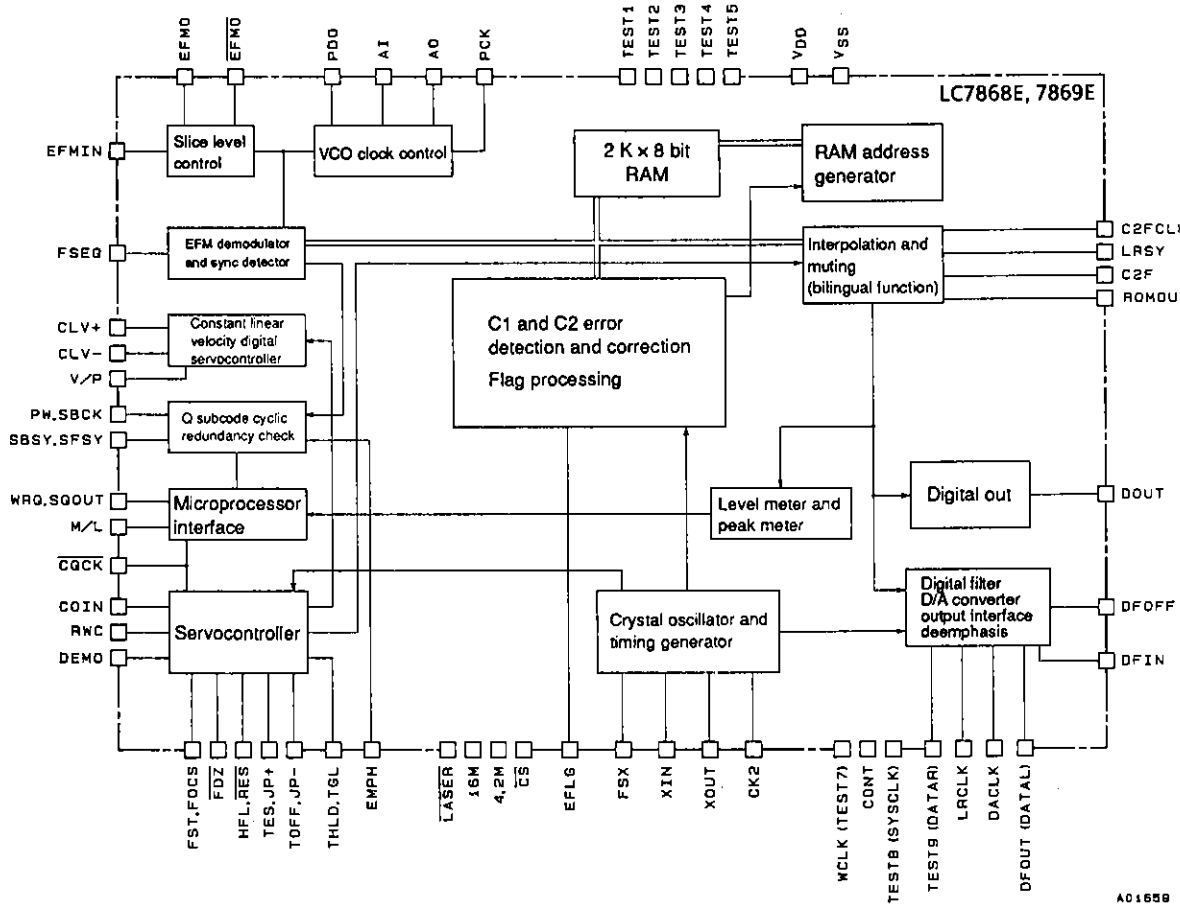
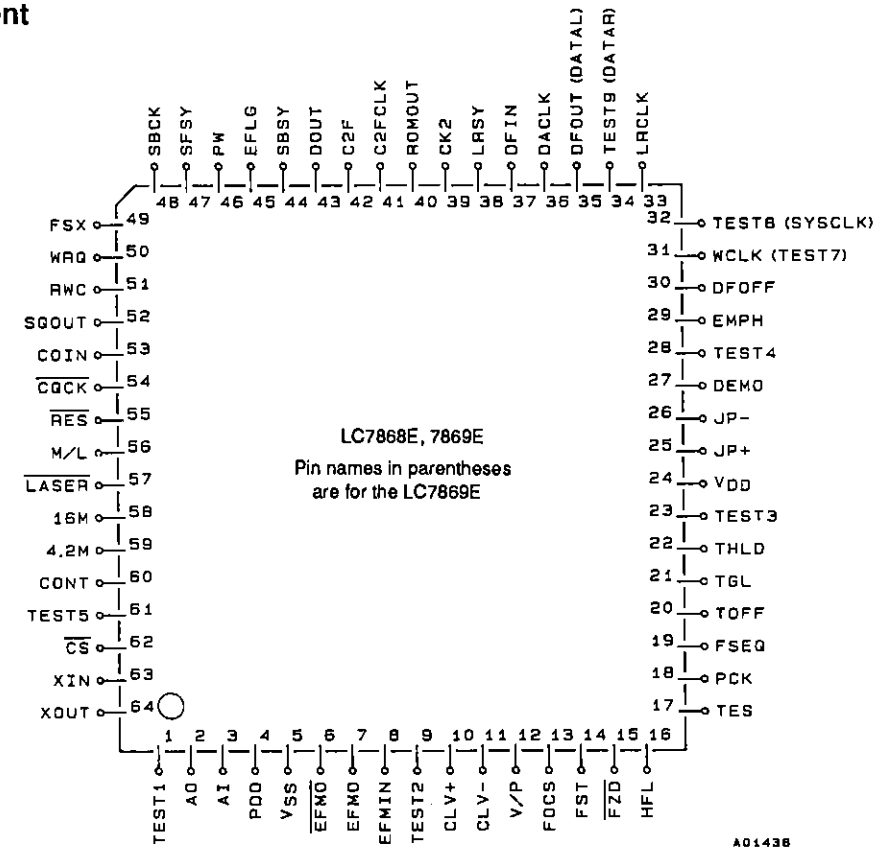
Equivalent Circuit

Block names in parentheses are for the LC7869E.



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to 7	V
Maximum input voltage	V_{IN} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Maximum output voltage	V_{OUT} max		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
Input high level voltage	V_{IH} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, DFOFF, M/L, $\overline{RES}$	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	2.2		V_{DD}	V
	V_{IH} (3)	EFMIN	0.6 V_{DD}		V_{DD}	V
	V_{IH} (4)	TES	0.8 V_{DD}		V_{DD}	V
Input low level voltage	V_{IL} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, DFOFF, M/L, $\overline{RES}$	V_{SS}		0.3 V_{DD}	V
	V_{IL} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	V_{SS}		0.8	V
	V_{IL} (3)	EFMIN	V_{SS}		0.4 V_{DD}	V
	V_{IL} (4)	TES	V_{SS}		0.2 V_{DD}	V
Data setup time	t set up	COIN, RWC: Figure 1	400			ns
Data hold time	t hold	RWC: Figure 1	400			ns
High level clock pulse width	$t_{WøH}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Low level clock pulse width	$t_{WøL}$	$\overline{CQCK}$, SBCK: Figures 1, 2 and 3	400			ns
Data read access time	t_{RAC}	Figures 2 and 3	0		400	ns
Command output time	t_{RWC}	RWC: Figure 1	1000			ns
Sub-Q read enable time	t_{SQE}	Figure 2, no RWC signal		11.2		ms
Subcode read cycle	t sc	Figure 3		136		µs
Subcode read enable	t se	Figure 3	400			ns
Crystal oscillator frequency	fX'tal	X_{IN}, X_{OUT}		16.9344		MHz
Operating frequency range	f op (1)	AI	2.0		20	MHz
	f op (2)	EFMIN: V_{IN} ≥ 1 Vpp			10	MHz

Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V, V_{DD} = 5 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current drain	I_{DD}			17	30	mA
Input high level current	I_{IH} (1)	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{DD}			5	µA
	I_{IH} (2)	TEST1 to 5, DEMO, $\overline{CS}$: V_{IN} = V_{DD} = 5.5 V	25		75	µA
Input low level current	I_{IL} (1)	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{SS}	–5			µA
Output high level voltage	V_{OH} (1)	AO, PDO, EFMO, $\overline{EFMO}$, CLV+, CLV–, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP–, EMPH, EFLG, FSX, V/P: I_{OH} = –1 mA	V_{DD} – 1			V
	V_{OH} (2)	DOUT: I_{OH} = –12 mA	V_{DD} – 0.5			V
	V_{OH} (3)	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, LRCLK, WRQ, C2F, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK, DFOUT (DATAL), TEST9 (DATAR), TEST8 (SYSCLK), WCLK (TEST7), DFIN: I_{OH} = –0.5 mA	V_{DD} – 1			V

Note: Pin names in parentheses are for the LC7869E.

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Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output low level voltage	V_{OL} (1)	AO, PDO, EFMO, $\overline{\text{EFMO}}$, CLV+, CLV−, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP+, JP−, EMPH, EFLG, FSX, V/P: I_{OL} = 1 mA			1	V
	V_{OL} (2)	DOUT: I_{OL} = 12 mA			0.5	V
	V_{OL} (3)	$\overline{\text{LASER}}$, SQOUT, 16M, 4.2M, CONT, LRCLK, WRQ, C2F, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK, DFOUT (DATAL), TEST9 (DATAR), TEST8 (SYSCLK), WCLK (TEST7), DFIN: I_{OL} = 2 mA			0.4	V
	V_{OL} (4)	FST: I_{OL} = 5 mA			0.75	V
Output off leakage current	I_{OFF} (1)	PDO, FST: $V_{OH} = V_{DD}$			5	µA
	I_{OFF} (2)	PDO, FST: $V_{OL} = V_{SS}$	−5			µA

Note: Pin names in parentheses are for the LC7869E.

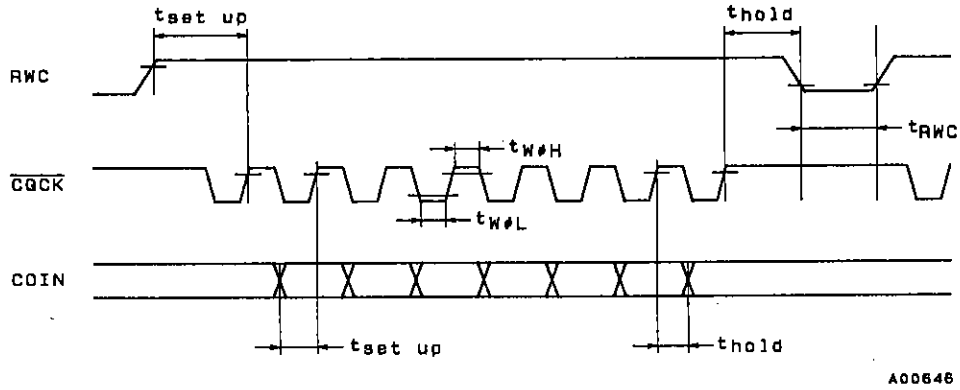

Figure 1 Command Input

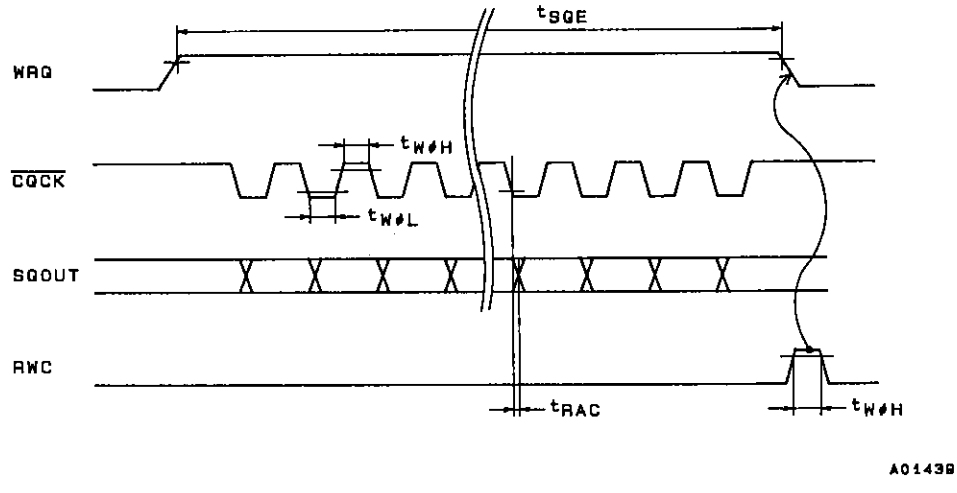

Figure 2 Subcode Q Output

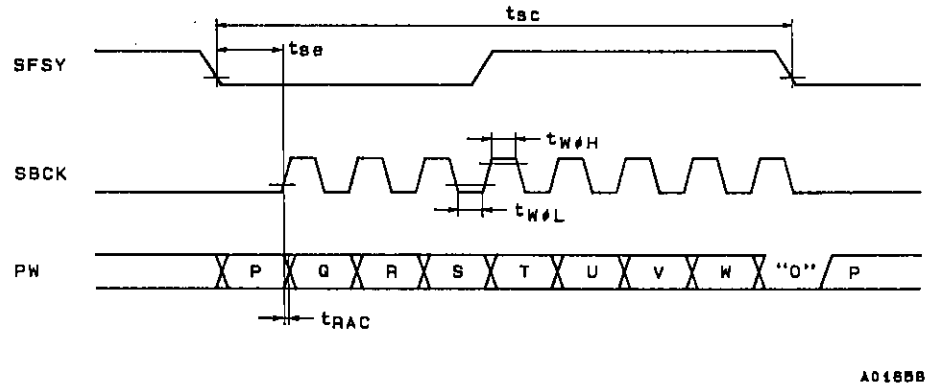

Figure 3 Subcode Output

Pin Description

No.	Name	I/O	Description
1	TEST1	I	LSI test input. Normally unconnected.
2	AO	O	Pin for input of the on-chip VCO output from the LA9210 (8.6436 MHz). Phase detector output (PDO) is phased output with the EFM signal, set so that frequency is raised by positive voltage.
3	AI	I	
4	PDO	O	
5	V_{SS}	—	GND
6	$\overline{EFMO}$	O	Inputs 1 to 2 V_{PP} HF signal to EFMIN. Complementary EFM signal output is made from EFMO and $\overline{EFMO}$ via the amplitude limiter. These are used for slice level control.
7	EFMO	O	
8	EFMIN	I	
9	TEST2	I	LSI test input. Normally unconnected.
10	CLV+	O	Disc motor control outputs.
11	CLV-	O	
12	V/P	O	Output is high with constant linear velocity rough servo, and low during phase control
13	FOCS	O	Focus servo is switched off when FOCS is high. Lens is lowered by FST and raised gradually when FOCS is high. Generation of $\overline{FZD}$ resets FOCS. Used for focus servo control.
14	FST	O	
15	$\overline{FZD}$	I	
16	HFL	I	Generates kick pulse, JP+, or JP- according to track jump command. Jumps the specified number of tracks (1, 2, 4, 16, 32, 64, or 128).
17	TES	I	
18	PCK	O	4.3218 MHz PCK monitor output.
19	FSEQ	O	High when SYNC (true frame sync) detected from the EFM signal matches SYNC from counter (interleaving frame sync). (Single-frame latch output.)
20	TOFF	O	Generates kick pulse, JP+, or JP- according to track jump command. Jumps the specified number of tracks (1, 2, 4, 16, 32, 64, or 128).
21	TGL	O	
22	THLD	O	
23	TEST3	I	LSI test input. Normally unconnected.
24	V_{DD}	—	+5 V
25	JP+	O	Generates kick pulse, JP+, or JP- according to track jump command. Jumps the specified number of tracks (1, 2, 4, 16, 32, 64, or 128).
26	JP-	O	
27	DEMO	I	Sound generation function for set adjustment.
28	TEST4	I	LSI test input. Normally unconnected.
29	EMPH	O	Deemphasis required when high.
30	DFOFF	I	Digital filter on/off switch: the filter is disabled when this pin is high.
31	WCLK (TEST7)	O	Signal outputs for the D/A converter, including latch, L/R switching, and sample and hold signals.
32	TEST8 (SYSCLK)	O	
33	LRCLK	O	
34	TEST9 (DATAR)	O	
35	DFOUT (DATAL)	O	
36	DACLK	O	
37	DFIN	O	LSI test input. Normally unconnected.

Note: Pin names in parentheses are for the LC7869E.

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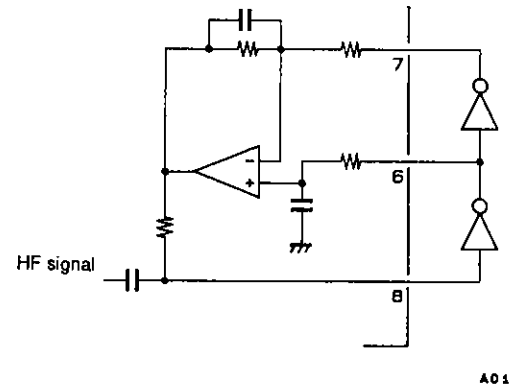
No.	Name	I/O	Description
38	LRSY	O	For output of CD-ROM interface signals.
39	CK2	O	
40	ROMOUT	O	
41	C2FCLK	O	
42	C2F	O	
43	DOUT	O	Digital OUT output
44	SBSY	O	Subcode block synchronization output
45	EFLG	O	C1 and C2 single and double error correction flag.
46	PW	O	SFSY is subcode frame synchronization signal. P, Q, R, S, T, U, V, and W subcodes are read out by sending clock eight times to SBCK.
47	SFSY	O	
48	SBCK	I	
49	FSX	O	7.35 kHz synchronization signal output
50	WRQ	O	WRQ goes high when Q subcode data passes the CRC check. Through external connection and sending of $\overline{CQCK}$, data is read from SQOUT. Set MSB-first/LSB-first to low when data in LSB-first format is desired. Command is generated by sending output synchronized with $\overline{CQCK}$ command data after setting microprocessor RWC to high.
51	RWC	I	
52	SQOUT	O	
53	COIN	I	
54	$\overline{CQCK}$	I	
55	$\overline{RES}$	I	Set to low at powerup.
56	M/L	I	Same as for pins 50 to 54.
57	$\overline{LASER}$	O	Permits control via serial control from the microprocessor.
58	16 M	O	16.9344 MHz output pin
59	4.2 M	O	4.2336 MHz output pin.
60	CONT	O	Permits control via serial control from the microprocessor.
61	TEST5	I	LSI test input. Normally unconnected.
62	$\overline{CS}$	I	Chip select pin. The LC7868/69 becomes active when this pin is low. (pull-down resistor built in)
63	X_{IN}	I	16.9344 MHz crystal oscillator connection pins.
64	X_{OUT}	O	

Note: Pin names in parentheses are for the LC7869E.

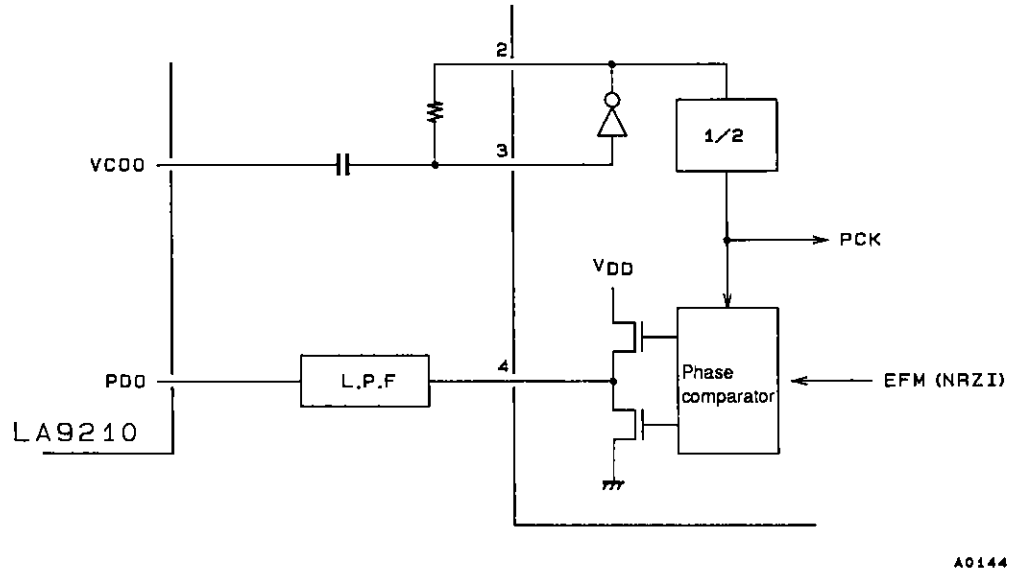
Functional Description

HF Signal Input Circuit (pin 8: EFMIN, pin 7: EFMO and pin 6: $\overline{EFMO}$)

An EFM signal (NRZ) sliced at the optimum level is obtained when the HF signal is input on EFMIN.



PLL Clock Regeneration Circuit (pin 4: PDO, pin 3: AI, and pin 2: AO)



A PLL comprising a VCO can be made with an LA9210. Output from the PDO pin goes positive when the VCO phase is lagging.

VCO Half-Frequency Clock (pin 18: PCK)

This pin monitors a signal generated by dividing the VCO frequency by two. This signal has an average frequency of 4.3218 MHz.

Frame Synchronization Detector Monitor (pin 19: FSEQ)

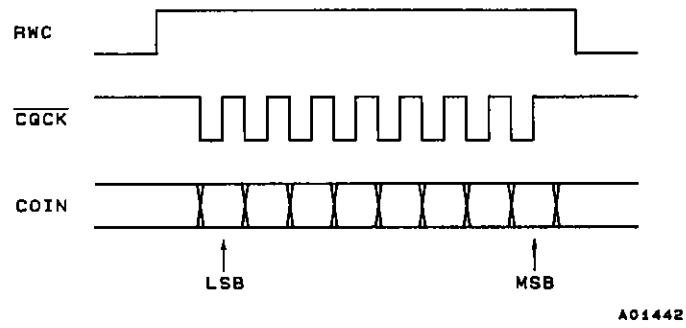
FSEQ is latched high for one frame when the frame sync (true synchronization signal) recovered from the EFM signal matches the sync timing generated by an internal counter.

Servo Command Function (pin 51: RWC, pin 53: COIN, pin 54: $\overline{\text{CQCK}}$ and pin 62: $\overline{\text{CS}}$)

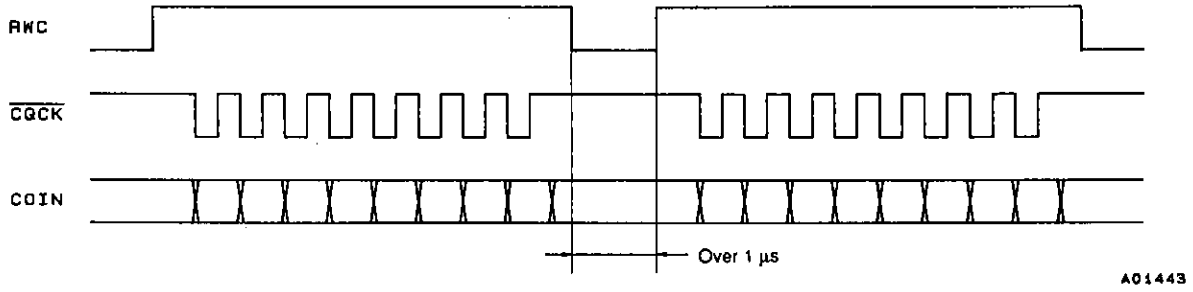
Commands can be input by setting RWC high and issuing the command synchronized to the $\overline{\text{CQCK}}$ clock from COIN.

Focus start Track jump Mute control Disc motor control Other control commands	1-byte commands
Track count	2-byte command

1. 1-byte Commands



2. 2-byte Commands

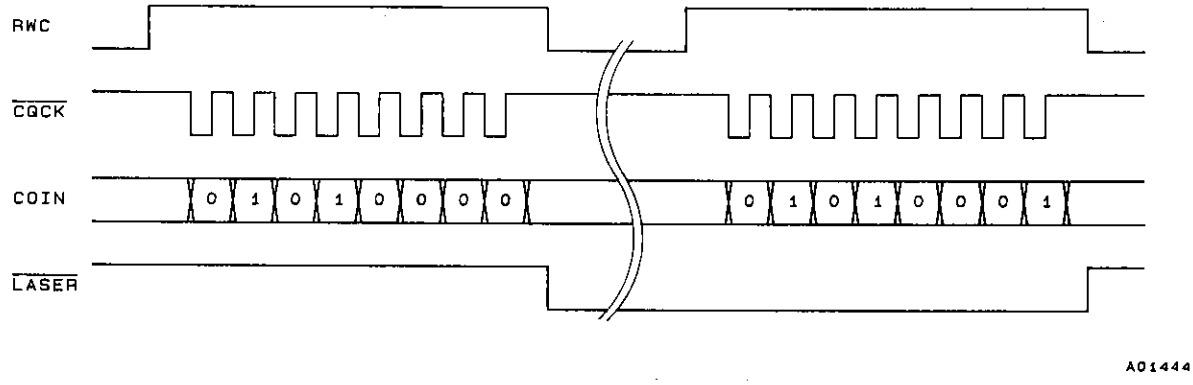


The commands are executed on the falling edge of RWC.

Focus Servocontroller (pin 13: FOCS, pin 14: FST, pin 15: $\overline{\text{FZD}}$ and pin 57: $\overline{\text{LASER}}$)

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 0	FOCUS START #1	
1 0 1 0 0 0 1 0	FOCUS START #2	
0 0 0 0 1 0 1 0	LASER ON	
1 0 0 0 1 0 1 0	LASER OFF	○
0 0 0 0 0 0 0 0	NOTHING	

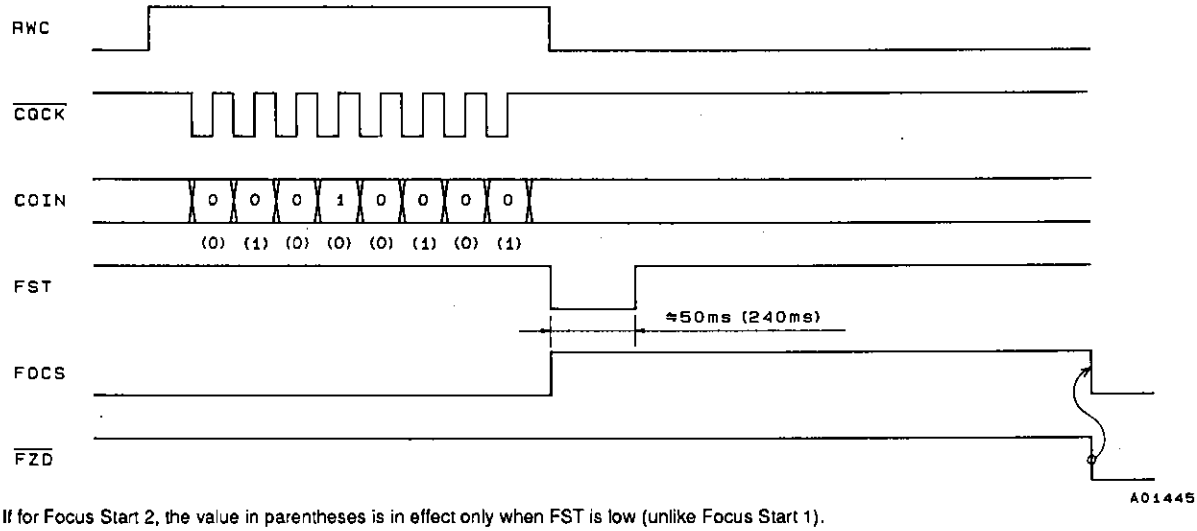
1. Laser Control



2. Focus Start

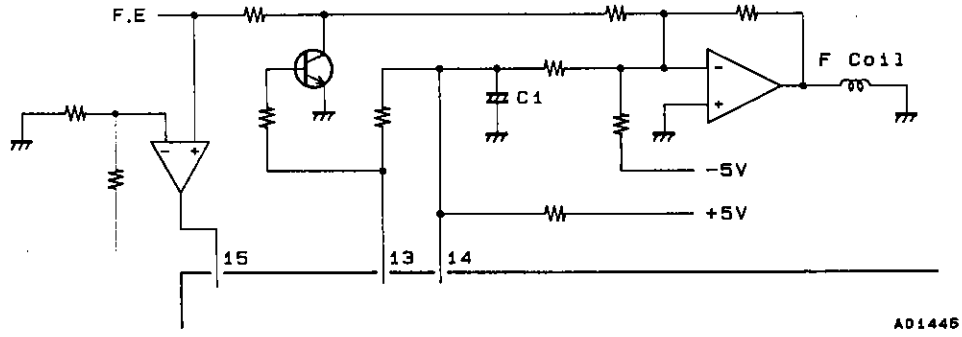
When a Focus Start command (either 1 or 2) is issued, the pickup lens is first lowered as C1 discharges through FST and then raised gradually as C1 is recharged by FOCS. $\overline{\text{FZD}}$ goes low when the focal point is reached, and FOCS is reset and the focus servocontroller turned on when this signal is received.

After issuing this command, the microprocessor checks the DRF signal from the LA9210 to verify that focus has been reached, and advances to the next step. If C1 recharges fully before focus has been reached, the Focus Start command should be reissued to repeat operation of the focus servocontroller.



Note: If for Focus Start 2, the value in parentheses is in effect only when FST is low (unlike Focus Start 1).

Notes: 1. The falling edge of $\overline{\text{FZD}}$ is not accepted when FST is low.
2. After a Focus Start command has been issued, the focus servocontroller is reinitialized when RWC goes high. For this reason, a new command should not be issued until the S-curve for the focus coil drive has been completed.
3. If focus cannot be reached (i.e., the $\overline{\text{FZD}}$ signal does not go low), the FOCS signal remains high and the lens remains raised. In this case, the Nothing command should be issued to reinitialize the servocontroller.
4. When the $\overline{\text{RES}}$ pin is set low, $\overline{\text{LASER}}$ is directly set high.
5. Focus start using the DEMO pin is in mode 1.

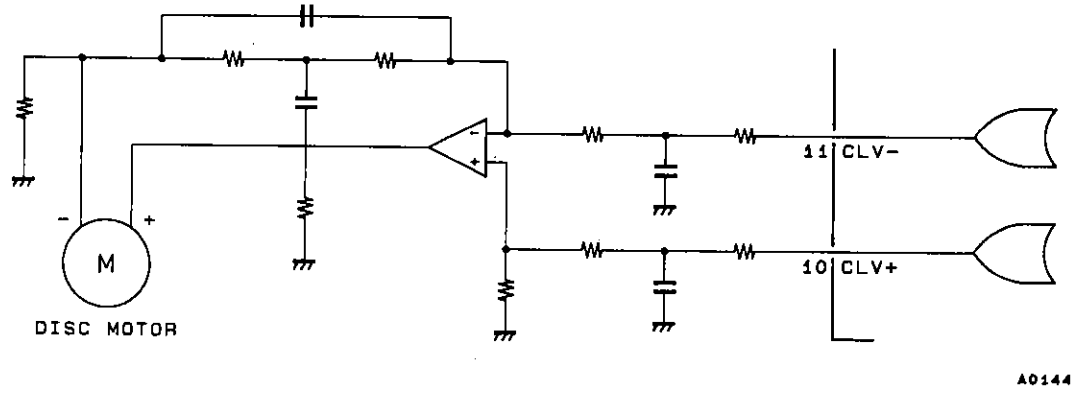


Constant Linear Velocity Servocontroller (pin 10: CLV⁺, pin 11: CLV⁻ and pin 12: V/P)

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 0 1 0 0	DISC MOTOR START (accelerate)	
0 0 0 0 0 1 0 1	DISC MOTOR CLV (CLV)	
0 0 0 0 0 1 1 0	DISC MOTOR BRAKE (decelerate)	
0 0 0 0 0 1 1 1	DISC MOTOR STOP (stop)	○

The disc motor accelerates when CLV⁺ is high and decelerates when CLV⁻ is high. These outputs are selected by the motor mode commands issued by the microprocessor (accelerate, decelerate, CLV, or stop). The CLV⁺ and CLV⁻ outputs for each mode are shown in the following table.

Mode	CLV+	CLV-
Accelerate	High	Low
Decelerate	Low	High
CLV	*	*
Stop	Low	Low



Note: * For constant linear velocity servo control commands, the TOFF pin is low only in the CLV mode; otherwise it is high. Control of the TOFF pin by command is effective only in the CLV mode.

1. CLV Mode

- In the CLV (constant linear velocity) mode, the LC78681E detects disc speed from the HF signal and switches the internal DSP mode to perform various types of control for maintaining the correct linear velocity. The pulse-width modulation cycle is 7.35 kHz, and the 1/64 duty cycle is 1.114 s. V/P outputs high during rough servo and low during phase control.

Internal mode	CLV+	CLV-	V/P
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PLCK locked)	PWM	PWM	Low

2. CLV Control Gain Switching

MSB LSB	Command	$\overline{RES}$ = low
1 0 1 0 1 0 0 0	DISC 8 set	
1 0 1 0 1 0 0 1	DISC 12 set	○

CLV control gain during rough switching for 8-cm discs can be set at 8.5 dB lower than for 12-cm discs.

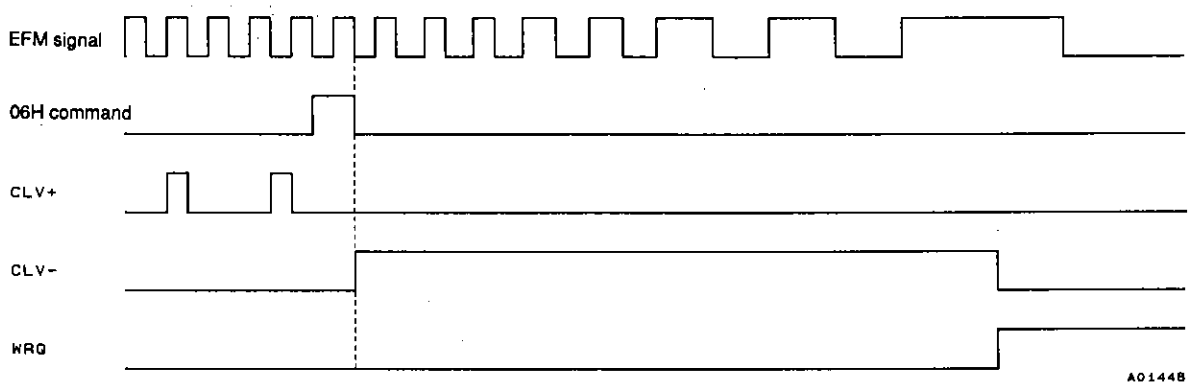
3. Internal Brake Mode

MSB LSB	Command	$\overline{RES}$ = low
1 1 0 0 0 1 0 1	Internal brake on	
1 1 0 0 0 1 0 0	Internal brake off	○
1 0 1 0 0 0 1 1	Internal brake control	

- The internal brake mode is enabled when an Internal Brake On command (C5H) is input. Executing a Brake command (06H) in this mode allows the deceleration of the disk to be monitored at the WRQ pin.

- In this mode, the EFM signal density per frame can be counted to determine the status of disc deceleration. When there are fewer than four EFM signals, CLV- falls to low, and the WRQ pin simultaneously goes high to indicate that brakes is completed. The microprocessor issues a Stop command when it senses that the WRQ pin is high, thereby completing the stopping of the disc.

- Note that if false deceleration state detections occur, changing the EFM signal count from 4 to 8 using the internal brake control command (A3H) may help in some cases.



Notes: 1. If focus is lost during execution of an internal brake command, it is necessary to first refocus and then input the internal brake command again.
2. Due to the possibility of state determination errors due to the EFM signal playback state (e.g., damaged disk or access in progress) we recommend that this product be used in conjunction with a microprocessor.

Track Jump Circuit
(pin 16: HFL, pin 17: TES, pin 20: TOFF, pin 21: TGL, pin 22: THLD, pin 25: JP^+ and pin 26: JP^-)

1. Internal Track Count

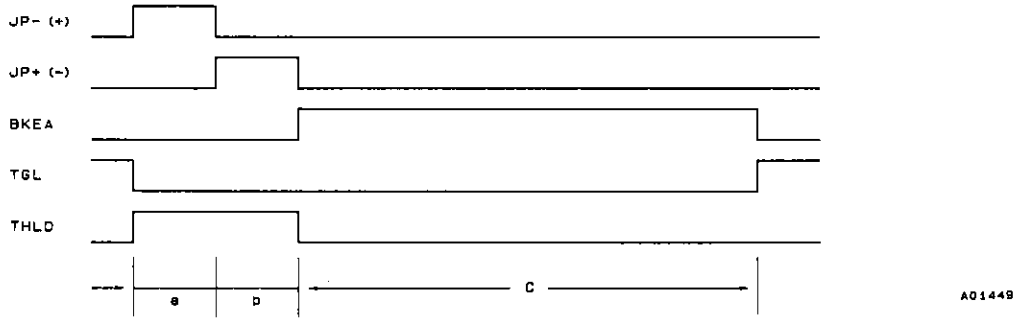
The LC7868/69 supports two internal track counting modes, as shown in the table below.

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 0 0 1 0	New track count (combination of TES and HFL)	○
0 0 1 0 0 0 1 1	Standard track count (direct count of the TES signal)	

The standard track count uses the TES signal without modification as the internal track count clock. In order to reduce counting errors due to noise on the rising and falling edges of the TES signal, the new track counter suppresses this noise through combination with the HFL signal, enabling an accurate track count. However, if the HFL signal is lost because of foreign matter or scratching on the disk, no track count pulse may be generated. For this reason, caution is required when using this mode.

2. Track Jump Commands

MSB							LSB	Command	$\overline{RES}$ = low
1	0	1	0	0	0	0	0	Standard track jump	○
1	0	1	0	0	0	0	1	New track jump	
0	0	0	1	0	0	0	1	1 TRACK JUMP IN #1	
0	0	0	1	0	0	1	0	1 TRACK JUMP IN #2	
0	0	1	1	0	0	0	1	1 TRACK JUMP IN #3	
0	0	0	1	0	0	0	0	2 TRACK JUMP IN	
0	0	0	1	0	0	1	1	4 TRACK JUMP IN	
0	0	0	1	0	1	0	0	16 TRACK JUMP IN	
0	0	1	1	0	0	0	0	32 TRACK JUMP IN	
0	0	0	1	0	1	0	1	64 TRACK JUMP IN	
0	0	0	1	0	1	1	1	128 TRACK JUMP IN	
0	0	0	1	1	0	0	1	1 TRACK JUMP OUT #1	
0	0	0	1	1	0	1	0	1 TRACK JUMP OUT #2	
0	0	1	1	1	0	0	1	1 TRACK JUMP OUT #3	
0	0	0	1	1	0	0	0	2 TRACK JUMP OUT	
0	0	0	1	1	0	1	1	4 TRACK JUMP OUT	
0	0	0	1	1	1	0	0	16 TRACK JUMP OUT	
0	0	1	1	1	0	0	0	32 TRACK JUMP OUT	
0	0	0	1	1	1	0	1	64 TRACK JUMP OUT	
0	0	0	1	1	1	1	1	128 TRACK JUMP OUT	
0	0	0	1	0	1	1	0	256 TRACK CHECK	
0	0	0	0	1	1	1	1	TOFF	
1	0	0	0	1	1	1	1	TON	○
1	0	0	0	1	1	0	0	TRACK JUMP BRAKE	



When a track jump command is issued to the servocontroller, an acceleration pulse is generated (a period), followed by a deceleration pulse (b period) and braking (c period), completing the specified jump. TES and HFL input during braking detects the direction of beam slippage, and the portion of the TE signal that compensates for slippage is cut off by TOFF, which, together with boosting of the servo gain by TGL, supplements the destination track for the jump.

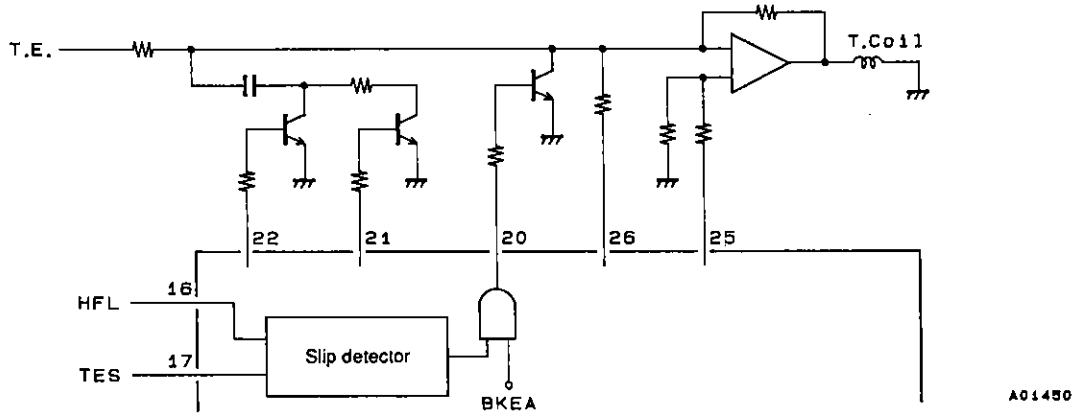
Note: Of the disc motor control outputs, the TOFF pin is low in the CLV mode, and high in the Start Stop, and Brake modes. TOFF can also be independently switched on or off by the microprocessor. However, disc motor control is enabled only in the CLV mode.

3. Track Jump Modes

The relationship between acceleration pulses, deceleration pulses, and brake periods is shown in the following table.

Command	Standard track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	24 ms	233 µs	233 µs	24 ms
1 TRACK JUMP IN (OUT) #2	0.5-track jump	233 µs	24 ms	0.5-track jump	a period	24 ms
1 TRACK JUMP IN (OUT) #3	0.5-track jump	233 µs	Does not occur	0.5-track jump	a period	Does not occur
2 TRACK JUMP IN (OUT)	There are no a, b, or c periods.			1-track jump	a period	Does not occur
4 TRACK JUMP IN (OUT)	2-track jump	466 µs	24 ms	2-track jump	a period	24 ms
16 TRACK JUMP IN (OUT)	9-track jump	7-track jump	24 ms	9-track jump	a period	24 ms
32 TRACK JUMP IN (OUT)	18-track jump	14-track jump	24 ms	18-track jump	14-track jump	24 ms
64 TRACK JUMP IN (OUT)	36-track jump	28-track jump	24 ms	36-track jump	28-track jump	24 ms
128 TRACK JUMP IN (OUT)	72-track jump	56-track jump	24 ms	72-track jump	56-track jump	24 ms
256 TRACK CHECK	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		24 ms	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		24 ms
TRACK JUMP BRAKE	There are no a or b periods.		24 ms	There are no a or b periods.		24 ms

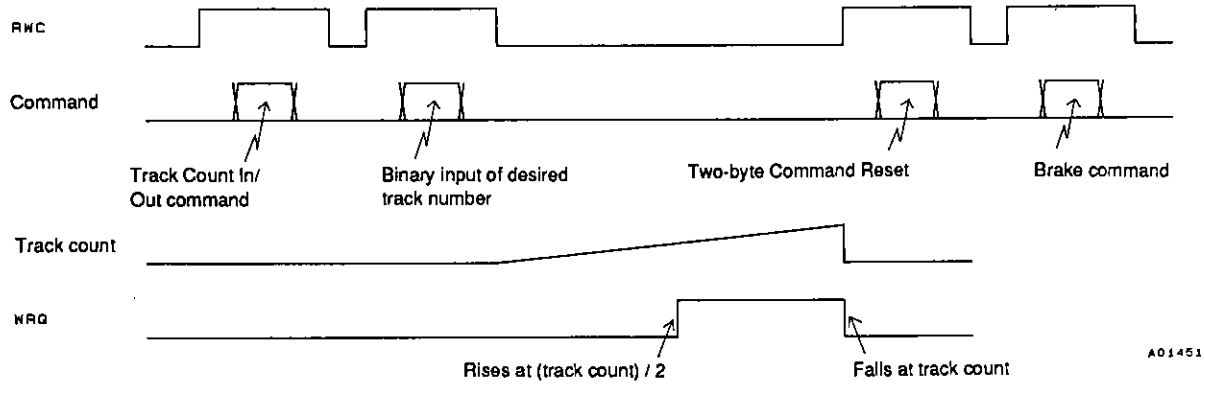
Notes: 1. The actuator drive signals are not generated for the 256-track Check. Instead issuance of a feed motor signal is required because the TES signal is in the track-count mode and the tracking servocontroller is off.
2. The servocontroller register is automatically reset after one a, b, and c track jump sequence.
3. When a new track jump command is issued while a previous command is still being processed, the new command is executed immediately.



4. Track Check Mode

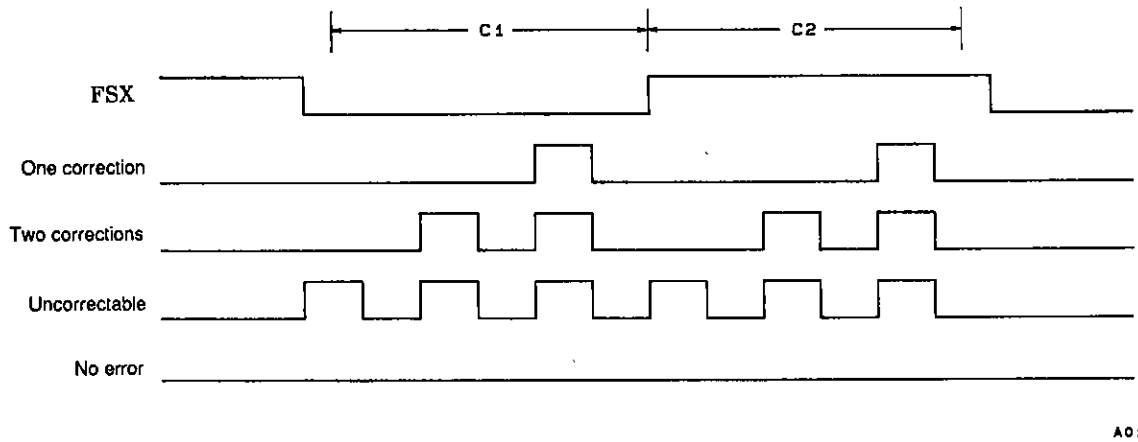
MSB LSB	Command	$\overline{RES}$ = low
1 1 1 1 0 0 0 0	Track Count In	
1 1 1 1 1 0 0 0	Track Count Out	
1 1 1 1 1 1 1 1	2-byte COMMAND RESET	○

A Track Count In or Track Count Out command followed by a binary number between 16 and 254 can be used to start track counting for the specified number of tracks.



Notes: 1. The fall of RWC when the desired number of tracks is input in binary format starts the track count.
2. During track counting, TOFF is high and the tracking servocontroller is turned off. For this reason, issuance of a feed motor signal is required.
3. The Track Count In and Track Count Out commands cause the WRQ signal to change from the Q subcode standby monitor when normal to the track count monitor. WRQ goes high at half the track count and low again at the end of the count. The microprocessor monitors WRQ to detect track count completion.
4. When a 2-byte Command Reset command is not issued, the track count starts again. For example, to advance 20,000 tracks, the microprocessor can set the track count number to 200 and wait 100 WRQ pulses.
5. The Brake command is used to bring the pickup to the track when counting is finished.

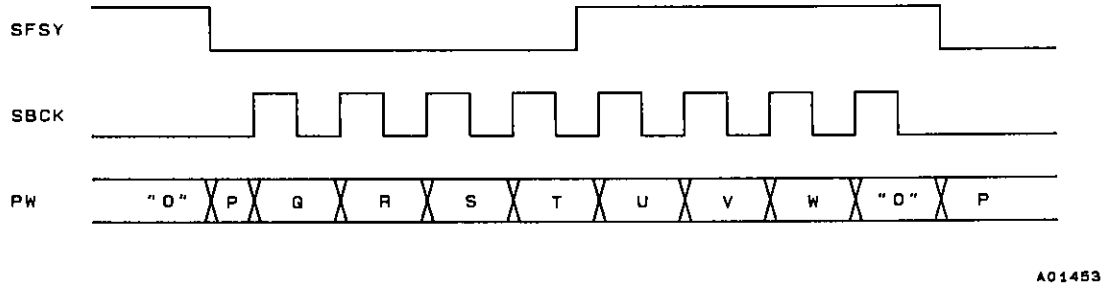
Error Flag Output (pin 45: EFLG and pin 49: FSX)



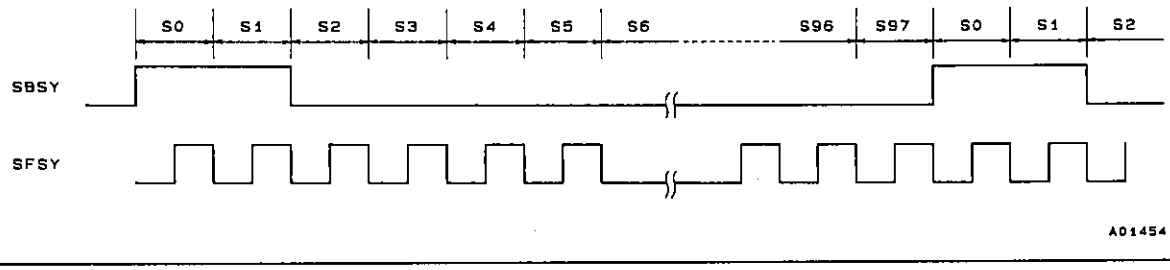
The 7.35 kHz FSX frame synchronization signal is divided down from the reference clock. The status of error correction in each frame is output on EFLG, as shown in the figure, where the number of high pulses in each FSX period indicates the quality of the replay signal.

P, Q, and R through W Subcode Output Circuit (pin 46: PW, pin 44: SBSY, pin 47: SFSY and pin 48: SBCK)

PW is the subcode signal output pin. The falling edge of SFSY starts the 136 µs period during which SBCK is clocked eight times, allowing all codes — P, Q, and R through W — to be read. The signals appearing at the PW pin change with the rising edge of SBCK. When SBCK is static, the P code is input to PW. SFSY is the signal output for each subcode frame, and the rising edge of this signal indicates standby status for output of the subcode symbols (P through W). Subcode data P if output simultaneously with the falling edge of this signal.



SBSY is output for each subcode block. It is high during the S0 and S1 synchronization cycles. Its falling edge indicates the end of synchronization and the start of EIAJ-format data within the subcode block.



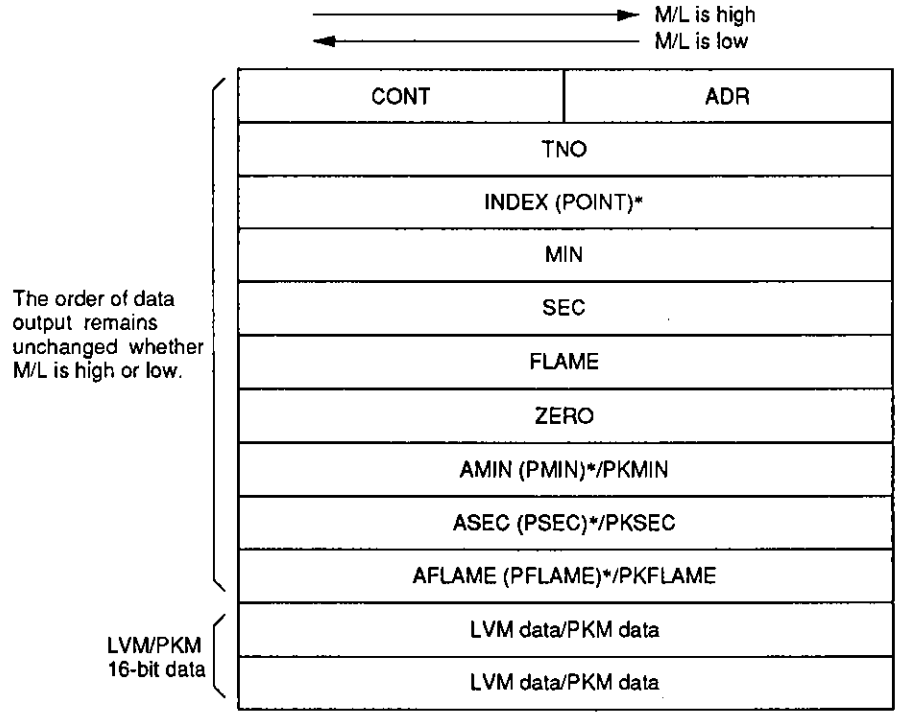
Q Subcode Output Circuit
(pin 50: WRQ, pin 51: RWC, pin 52: SQOUT, pin 54: $\overline{\text{CQCK}}$, pin 56: M/L and pin 62: $\overline{\text{CS}}$)

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 1	ADDRESS FREE	
1 0 0 0 1 0 0 1	ADDRESS 1	○

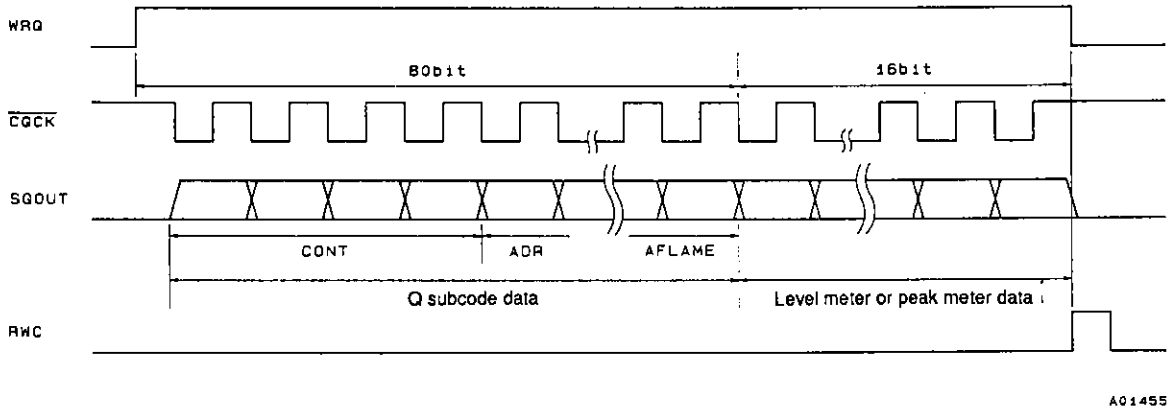
Q subcode data can be read from the SQOUT pin by clocking the $\overline{\text{CQCK}}$ pin.

Of the 8-bit subcode data, the Q signal is effective for operations such as song access and display. WRQ is high only when the block CRC is correct and the address in the Q subcode format is 1*.When the microprocessor senses that WRQ is high and issues $\overline{\text{CQCK}}$, data can be read from SQOUT in the sequence indicated below. When $\overline{\text{CQCK}}$ is activated, the DSP disables internal register updating. When the microprocessor finishes reading data, it briefly sets RWC high to reenable data updating and resets WRQ low. $\overline{\text{CQCK}}$ should start to oscillate in the 11.2 ms period during which WRQ is high. Data can be read in LSB-first format when M/L is low and in MSB-first format when it is high.

Note: * This condition is ignored when the Address Free command is issued. (The Address Free command is used in CD-V applications.)



Note: * Items in parentheses are for the disc lead-in area.



Notes: 1. The WRQ pin normally indicates Q subcode standby status, but provides different information during the Track Count mode or internal braking. (See the sections on track counting and internal braking.)

2. The LC78681E is active when $\overline{CS}$ is low, with output from SQOUT. SQOUT is in the high-impedance state when the $\overline{CS}$ pin is high.

Reading Level Meter (LVM) and Peak Meter (PKM) Data

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 1 0 1 1	PKM set (LVM reset)	
0 0 1 0 1 1 0 0	LVM set (PKM reset)	○
0 0 1 0 1 1 0 1	PKM mask set	
0 0 1 0 1 1 1 0	PKM mask reset	○

1. Level Meter (LVM)

- The Level Meter mode is enabled by inputting the Level Meter Set command (2CH).
- Level meter data is 16 bits, and is composed of 15 bits of absolute-value data and an MSB indicating left-right polarity. Data is for the left channel when the MSB is high and for the right channel when low.
- Level meter data is appended at the end of 80 bits of Q subcode data, and can be read from the SQOUT pin by clocking the $\overline{CQCK}$ pin 96 times. The left and right channels are swapped each time that level meter data is read. The left and right channels are independent, and the highest value read for each of the channels is held.

2. Peak Meter (PKM)

- The Peak Meter mode is enabled by inputting the Peak Meter Set command (2BH).
- Peak meter data is 16 bits, and is composed of 15 bits of absolute-value data and an MSB fixed at 0. The maximum value is detected with no regard for right or left channel.
- Peak meter data is read in a manner similar to that for level meter data. However, data is not updated by further reading.
- The absolute time for Q subcode data when in the Peak Meter mode is issued while holding the absolute time (ATIME) that is detected after generation of the maximum value. (Relative time is normal operation.)
- Issuing a Peak Meter Mask Set command causes values larger than the maximum value already in memory to be ignored, even when this command is issued in the Peak Meter mode. This is canceled by the Peak Meter Mask Reset command (used in peak searches for songs in memory).

Mute Control Circuit

MSB	LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 0 0 1		Mute 0 dB	
0 0 0 0 0 0 1 0		Mute −12 dB	
0 0 0 0 0 0 1 1		Mute ∞ dB	○

Volume can be reduced by 12 dB (MUTE −12 dB) or muted fully (MUTE ∞ dB) by issuing the commands shown above. Muting switches at zero crossings to prevent switching noise on the audio output. A zero crossing is judged to be any data where the upper seven bits are all 1 or all 0.

Bilingual Function

MSB	LSB	Command	$\overline{RES}$ = low
0 0 1 0 1 0 0 0		STO CONT	○
0 0 1 0 1 0 0 1		Lch CONT	
0 0 1 0 1 0 1 0		Rch CONT	

- The left and right channels are output to the left and right channels when reset or when the Stereo command (28H) is issued.
- Left channel data is output to both the left and right channels when the Left Channel Set command (29H) is issued.
- Right channel data is output to both the left and right channels when the Right Channel Set command (2AH) is issued.

Deemphasis Control (pin 29: EMPH)

The preemphasis on/off bit in the Q subcode data is output on EMPH. Deemphasis is required when EMPH is high.

MSB	LSB	Command	$\overline{RES}$ = low
0 1 1 0 1 0 0 1		DEP OFF	

The LC7868/69 includes a digital deemphasis circuit in the Difil block. On reset, the IC enters a mode in which the internal deemphasis is used. If an external deemphasis circuit is added, issue the DEP OFF command described above.

D/A converter interface; Pin 30: DFOFF, pin 31: WCLK (TEST7), pin 32: TEST (SYSCLK), pin 33: LRCLK, pin 34: DFOUT (DATAR), pin 35: DFOUT (DATAR), pin 36: DACLK

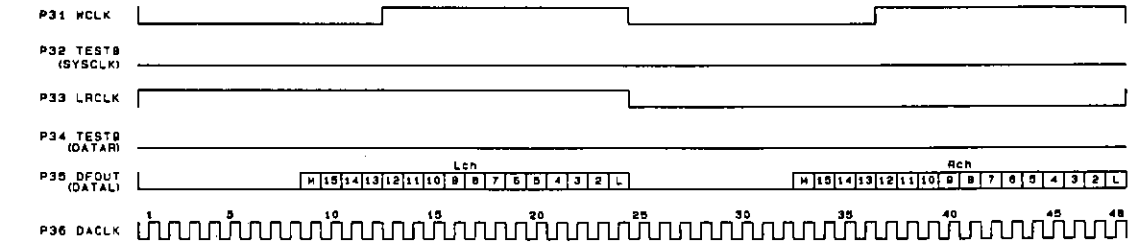
Data for the D/A converter is output from DFOUT MSB first, synchronized with the falling edge of DACLK.

MSB	LSB	Command	$\overline{RES}$ = low
0 1 1 0 0 0 1 0		DF FORM IIS	
0 1 1 0 0 0 1 1		DF FORM LC78815	○
0 1 1 0 1 0 0 0		DF FORM B.B	
1 0 0 0 1 0 0 0		CD-ROM XA	
1 0 0 0 1 0 1 1		CONT and CD-ROM XA reset	○

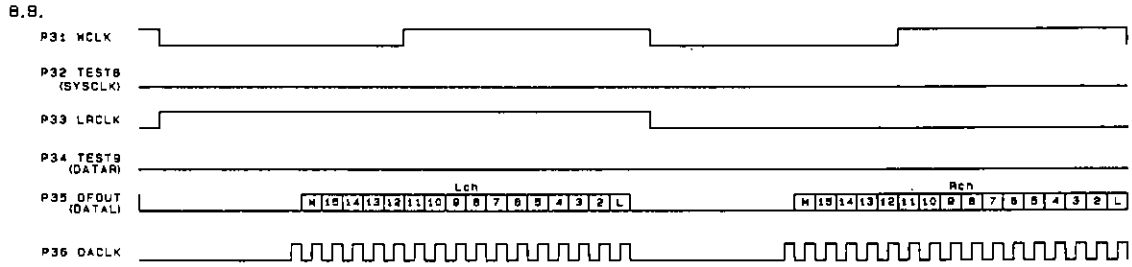
When the CD-ROM XA command listed above is issued, data for which neither interpolation nor muting is performed is output from DFOUT. This is for use with CD-ROM XA applications. Note that the CD-ROM XA reset is shared with the CONT reset (pin 60).

(1) LC7868E (4FS)

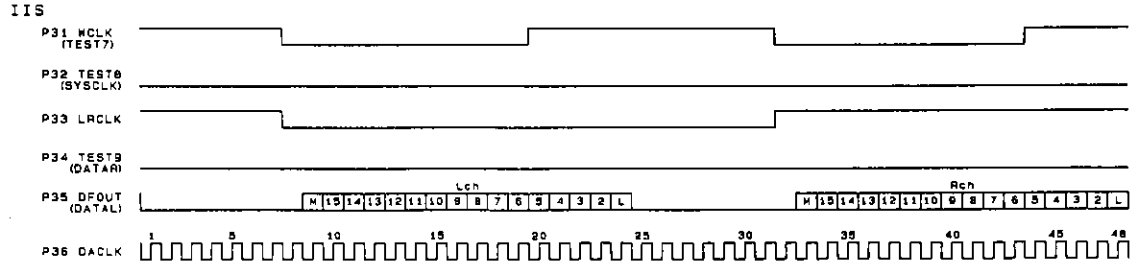
LC78815



B.B.



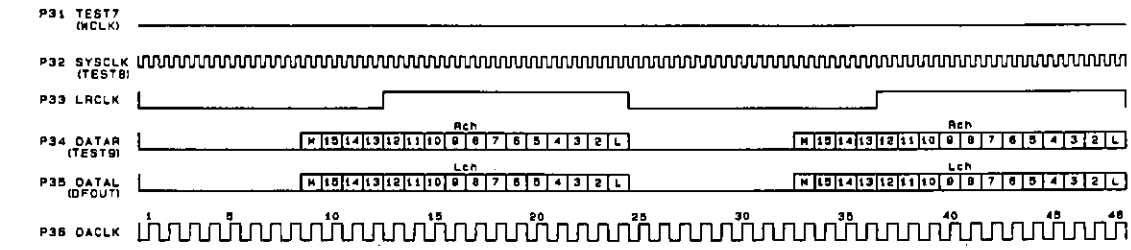
IIS



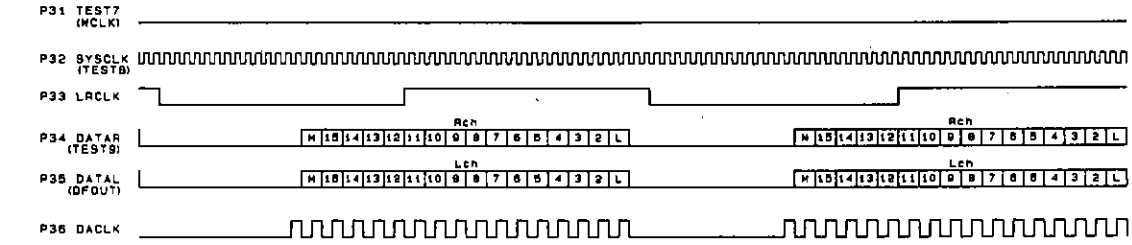
A01456

(2) LC7869E (8FS)

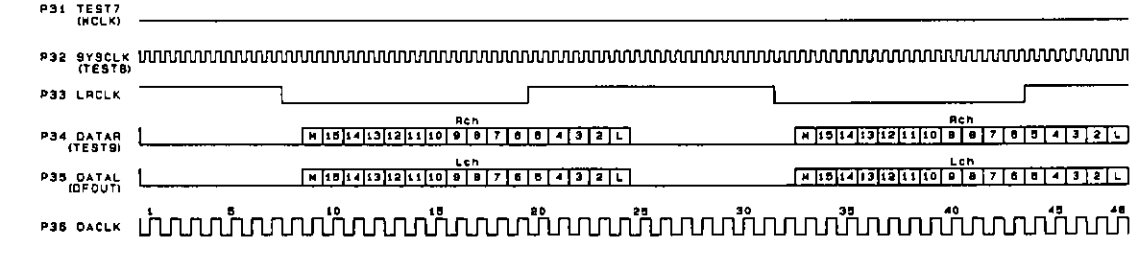
LC78815



B.B.



IIS

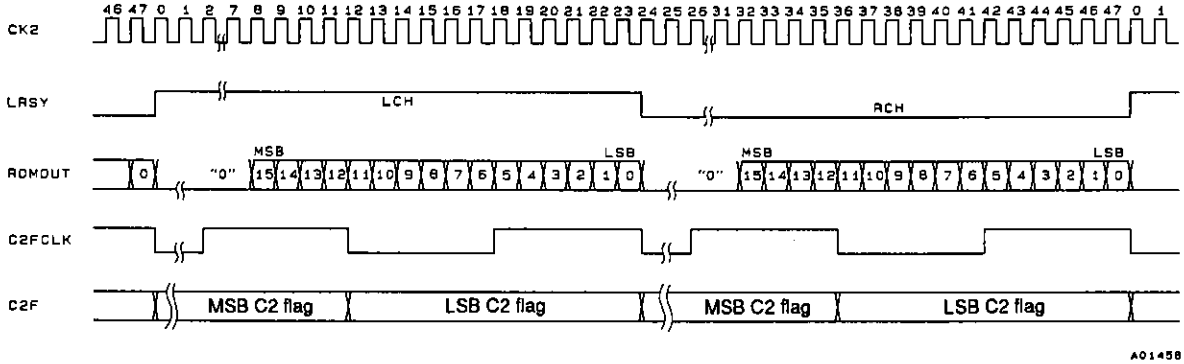


A01457

Output for CD-ROM (pin 39: CK2, pin 37: LRSY, pin 40: ROMOUT: pin 42: C2F and pin 41: C2FCLK)

Data from the ROMOUT pin which is synchronized with the LRSY signal is output in MSB-first format. Because this data has not been processed by either the interpolation, previous-value hold, or digital filtering circuits, it is suitable for CD-ROM IC input. CK2 is a 2.1168 MHz clock, and data is output on its rising edge. C2F flags 8-bit units of data, and is synchronized to C2FCLK.

LC89510-LC7868/69 Interface



Digital Audio Out Circuit (pin 43: DOUT)

This is the output pin for the digital audio interface, with output in EIAJ format. The signal is output after interpolation and muting. This output pin has a built-in driver, and can drive a transistor directly.

MSB LSB	Command	$\overline{RES}$ = low
0 1 0 0 0 0 1 0	DOUT ON	O
0 1 0 0 0 0 1 1	DOUT OFF	
0 1 0 0 0 0 0 0	UBIT ON	O
0 1 0 0 0 0 0 1	UBIT OFF	

- The digital out pin can be fixed low by issuing the DOUT OFF command.
- The UBIT data in the DOUT data can be fixed at 0 by issuing the UBIT OFF command.

Control Pin (pin 60: CONT)

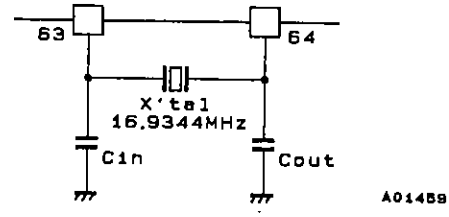
MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 1 1 1 0	CONT set	Low
1 0 0 0 1 0 1 1	CONT and CD-ROM XA Reset	O

The CONT pin can be set high by issuing the CONT Set command.

Crystal Oscillator (pin 63: X_{IN} and pin 64: X_{OUT})

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 1 1 0	OSC ON	O
1 0 0 0 1 1 0 1	OSC OFF	
0 1 1 0 0 0 0 0	VCO 8 M	O
0 1 1 0 0 0 0 1	VCO 16 M	

A 16.9344 MHz crystal oscillator is attached at these pins to form the time base clock.
The OSC OFF command turns off both the crystal oscillator and the VCO. The table below shows the relationship between the crystal oscillator and the VCO.



External components	X'tal	VCO	
	16.9344 MHz	8.6436 MHz	17.2872 MHz
Command	VCO 8M	VCO 8M	VCO 16M

Recommended crystal oscillator constants

Manufacturer	Oscillator	Cin/Cout
CITIZEN WATCH CO., LTD.	CSA-309 (16.9344 MHz)	6 pF to 10 pF (Cin = Cout)

4.2M and 16M Pins (pin 59: 4.2M and pin 58: 16M)

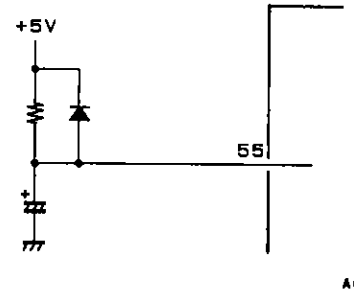
The 16.9344 MHz buffer output from the 16.9344 MHz crystal oscillator is output from the 16M pin. This signal is divided by four to generate a 4.2336 MHz signal, which is output from the 4.2M pin. When the oscillator is not operating, these pins are fixed to either high or low.

Reset Circuit (pin 55: $\overline{\text{RES}}$)

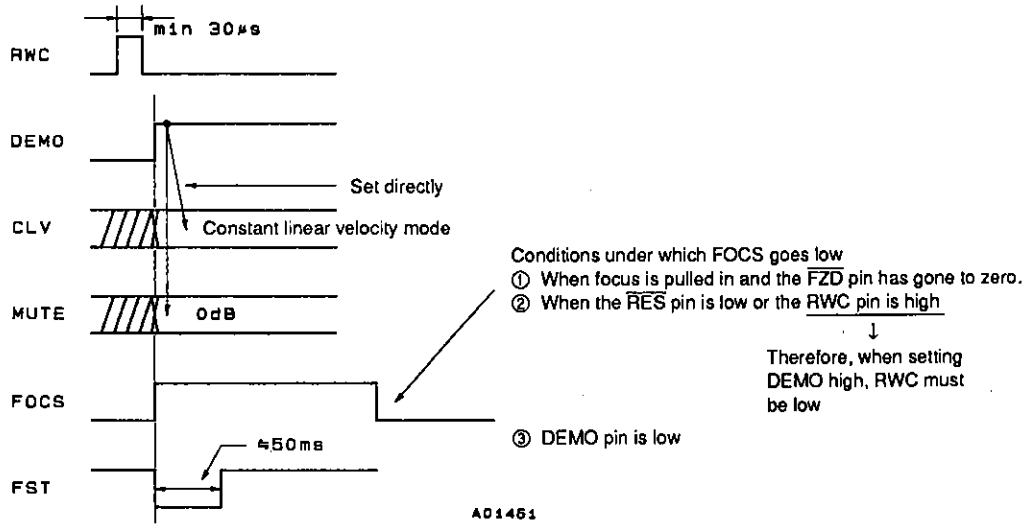
This pin should momentarily be held low after power-on before being driven high. This is set to –∞ dB for muting or to STOP for the disc motor.

Constant linear velocity servo	START	**STOP**	BRAKE	CLV
Muting control	0 dB	–12 db	**∞**	
Q subcode address conditions	**Address 1**	Address free		
Laser control	ON (low)	**OFF**	(high)	
CONT	High	**Low**		
OSC	**ON**	OFF		
Track jump mode	**Standard**	New		
Track count mode	Standard	**New**		

The states shown above in boxes are set directly when $\overline{\text{RES}}$ is low.



Audio Output for Calibration (pin 27: DEMO)



Setting this pin high sets muting to 0 dB and the disc motor to constant linear velocity, even when the microprocessor issues no command, and activates focusing. Because this also makes the $\overline{\text{LASER}}$ pin active, EFM signals and audio output can be obtained without the microprocessor as long as the mechanism and servo are hooked up correctly.

Other Pins (pin 1: TEST1, pin 9: TEST2, pin 23: TEST3, pin 28: TEST4, pin 61: TEST5 and pin 37: DFIN)

These are test pins for the internal circuitry of the LC7868E and the LC7869E. TEST1 through TEST5 have internal pull-down resistors. The test inputs can be left open during normal operation.

Description of Block Operation

1. RAM Address Control

The LC7868 includes an 8 bit by 2 kword RAM on chip. This is used as a ±4 frame buffer memory for the EFM demodulated data jitter compensation function, which is implemented using address control. The buffer controller constantly monitors buffer free space and adjusts the CLV servocontroller divider ratio to keep the data write address in the middle of the buffer (i.e., at zero). If the ±4-frame limit is exceeded, the write address is forced to ±0, and the output is muted for 128 frames because the resulting error cannot be handled by normal error processing algorithms.

Position	Division ratio or processing	
−4 or less	Force to ±0	
−3	589	Increase ratio
−2	589	
−1	589	
±0	588	Standard ratio
+1	587	Decrease ratio
+2	587	
+3	587	
+4 or more	Force to ±0	

C1 and C2 Error Correction

After EFM demodulation, data is written to the internal RAM, jitter is absorbed, and the processing described below is carried out under uniform timing according to the crystal clock. First, the C1 stage involves error detection and correction, determination of the C1 flags, and writing to the C1 flag register. Next, the C2 stage involves error detection and correction, determination of the C2 flags, and writing to the internal RAM.

C1 flag	Error correction and flag processing	
No errors	No correction required	Flag reset
1 error	Correction	Flag reset
2 errors	Correction	Flag set
3 errors or more	Correction not possible	Flag set

C2 flag	Error correction and flag processing	
No errors	No correction required	Flag reset
1 error	Correction	Flag reset
2 errors	Depends on C1 flags*1	
3 errors or more	Depends on C1 flags*2	

Notes: 1. If the error positions determined in the C2 stage match the C1 flags, correction is carried out and the flags are reset. However, if there are seven or more C1 flags, no correction is made (because of the danger of erroneous correction), and the C1 flags are taken as the C2 flags without change. If one error position matches but another does not, correction cannot be performed. Moreover, if there are five or fewer C1 flags, the results of the C1 stage may be incorrect, and the flag is set. If there are six or more, the situation is handled as uncorrectable, and the C1 flags are taken as the C2 flags without change. Correction is not possible if even only one error position is different, and the flags are set even if there are two or fewer C1 flags, because such data may be erroneous even if it passes the C1 stage. Otherwise the C1 flags are taken as the C2 flags without change.

2. If there are three or more errors and correction is determined to be impossible, no correction is made; if there are two or fewer C1 flags, data which passes the C1 stage may still be corrupt, and so the flags are set. Otherwise the C1 flags are taken as the C2 flags without change.

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