QUAD/DUAL N-CHANNEL ENHANCEMENT MODE EPAD® MATCHED PAIR MOSFET ARRAY

$V_{GS(th)}$= +0.8V

GENERAL DESCRIPTION

ALD110808A/ALD110808/ALD110908A/ALD110908 are monolithic quad/dual N-Channel MOSFETs matched at the factory using ALD's proven EPAD® CMOS technology. These devices are intended for low voltage, small signal applications.

These MOSFET devices are built on the same monolithic chip, so they exhibit excellent temperature tracking characteristics. They are versatile as circuit elements and are useful design component for a broad range of analog applications. They are basic building blocks for current sources, differential amplifier input stages, transmission gates, and multiplexer applications. For most applications, connect V- and N/C pins to the most negative voltage potential in the system and V+ pin to the most positive voltage potential (or left open unused). All other pins must have voltages within these voltage limits.

ALD110808/ALD110908 devices are built for minimum offset voltage and differential thermal response, and they are suited for switching and amplifying applications in +1.0V to +10V (+/- 5 V) systems where low input bias current, low input capacitance and fast switching speed are desired. As these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment.

These devices are suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result from extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 30pA at room temperature. For example, DC beta of the device at a drain current of 3mA and input leakage current of 30pA at 25°C is = 3mA/30pA = 100,000,000.

FEATURES

- Enhancement-mode (normally off)
- Standard Gate Threshold Voltages: +0.8V
- Matched MOSFET to MOSFET characteristics
- Tight lot to lot parametric control
- Low input capacitance
- $V_{GS(th)}$ match to 2mV and 10mV
- High input impedance — $10^{12}\Omega$ typical
- Positive,zero, and negative $V_{GS(th)}$ temperature coefficient
- DC current gain $>10^8$
- Low input and output leakage currents

ORDERING INFORMATION

Operating Temperature Range* 0°C to +70°C		0°C to +70°C	
16-Pin Plastic Dip Package	16-Pin SOIC Package	8-Pin Plastic Dip Package	8Pin SOIC Package
ALD110808APC ALD110808 PC	ALD110808ASC ALD110808SC	ALD110908APA ALD110908PA	ALD110908ASA ALD110908SA

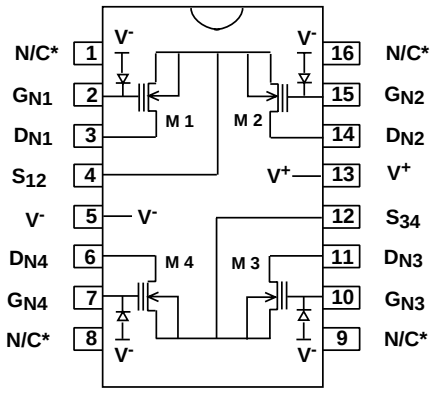
* Contact factory for industrial or military temp. ranges or user-specified threshold voltage values.

APPLICATIONS

- Precision current mirrors
- Precision current sources
- Voltage choppers
- Differential amplifier input stage
- Voltage comparator
- Voltage bias circuits
- Sample and Hold
- Analog inverter
- Level shifters
- Source followers and buffers
- Current multipliers
- Analog switches / multiplexers

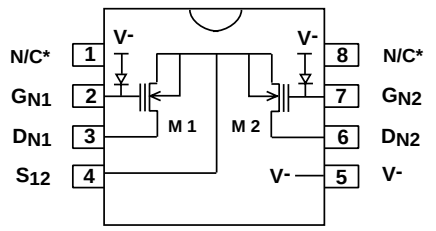
PIN CONFIGURATION

ALD110808



PC, SC PACKAGES

ALD110908



PA, SA PACKAGES

*N/C pins are internally connected.
Connect to V- to reduce noise

ABSOLUTE MAXIMUM RATINGS

Drain-Source voltage, V_{DS} 10.6V
Gate-Source voltage, V_{GS} 10.6V
Power dissipation 500 mW
Operating temperature range PA, SA, PC, SC package 0°C to +70°C
Storage temperature range -65°C to +150°C
Lead temperature, 10 seconds +260°C

OPERATING ELECTRICAL CHARACTERISTICS

V+ = +5V (or open) V- = GND T_A = 25°C unless otherwise specified

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

Parameter	Symbol	ALD110808A / ALD110908A			ALD110808/ ALD110908			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Gate Threshold Voltage	$V_{GS(th)}$	0.78	0.80	0.82	0.78	0.80	0.82	V	I_{DS} =1μA V_{DS} = 0.1V
Offset Voltage V_{GS1}-V_{GS2}	V_{OS}		1	2		3	10	mV	I_{DS}=1μA
V_{GS1}-V_{GS2} Tempco	ΔV_{OS}		5			5		μV/ °C	V_{DS1}= V_{DS2}
GateThreshold Tempco	$\Delta V_{GS(th)}$			-1.7 0.0 +1.6			-1.7 0.0 +1.6	mV/ °C	I_D= 1μA I_D= 20μA V_{DS} = 0.1V I_D= 40μA
On Drain Current	$I_{DS (ON)}$		12.0 3.0			12.0 3.0		mA	V_{GS}= +10.3V V_{GS}= +4.8V V_{DS}= +5V
Forward Transconductance	G_{FS}		1.4			1.4		mmho	V_{GS} = +4.8V V_{DS} = +9.8V
Transconductance Mismatch	ΔG_{FS}		1.8			1.8		%	
Output Conductance	G_{OS}		68			68		μmho	V_{GS} =+4.8V V_{DS} = +9.8V
Drain Source On Resistance	$R_{DS (ON)}$		500			500		Ω	V_{DS} = 0.1V V_{GS} = +4.8V
Drain Source On Resistance Mismatch	$\Delta R_{DS (ON)}$		0.5			0.5		%	
Drain Source Breakdown Voltage	BV_{DSX}	10			10			V	I_{DS} = 1.0μA V_{GS} = -0.2V
Drain Source Leakage Current[1]	$I_{DS (OFF)}$		10	100 4		10	100 4	pA nA	V_{GS} = -0.2V V_{DS} =10V, T_A = 125°C
Gate Leakage Current1	I_{GSS}		3	30 1		3	30 1	pA nA	V_{DS} = 0V V_{GS} = 10V T_A =125°C
Input Capacitance	C_{ISS}		2.5			2.5		pF	
Transfer Reverse Capacitance	C_{RSS}		0.1			0.1		pF	
Turn-on Delay Time	t_{on}		10			10		ns	V^+ = 5V R_L= 5KΩ
Turn-off Delay Time	t_{off}		10			10		ns	V^+ = 5V R_L= 5KΩ
Crosstalk			60			60		dB	f = 100KHz

Notes: [1] Consists of junction leakage currents