AKD4584
AK4584 Evaluation Board Rev.A

GENERAL DESCRIPTION

AKD4584 is an evaluation board for the 24bit 96kHz CODEC, AK4584. The AKD4584 can evaluate A/D converter D/A converter separately in addition to loop back mode (A/D → D/A). The AKD4584 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4584 --- Evaluation board for AK4584
(Cable for connecting with printer port of IBM-AT,
compatible PC and control software are packed with this.)

FUNCTION

- **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

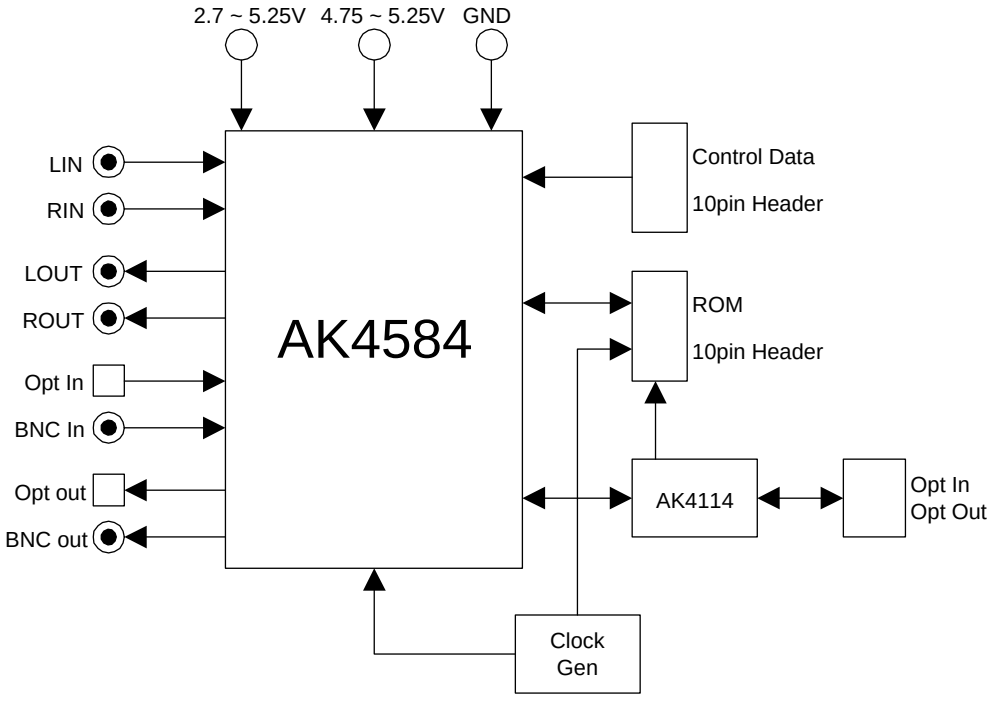


Figure 1. AKD4584 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

Evaluation Board Manual

■ Analog Input / Output circuits

(1) Input circuits

The analog input of AK4584 inputs from J1 (RIN), J3 (LIN).

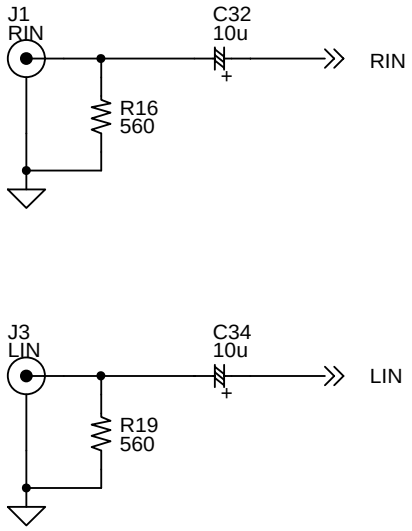


Figure 2. LIN/RIN Input circuits

(2) Output circuits

The analog output of AK4584's DAC outputs from J2 (ROUT), J4 (LOUT).

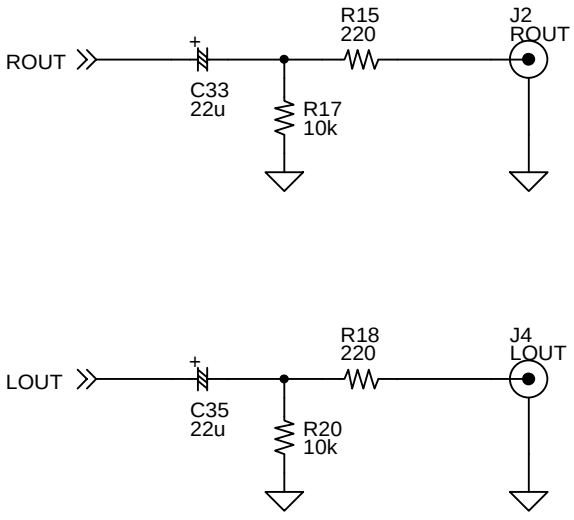


Figure 3. LOUT/ROUT Output circuits

* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Digital Input / Output circuits & Set-up jumper pin

(1) Digital input circuits

The digital input of AK4584 inputs from J7 (RX) or PORT5 (DIR).

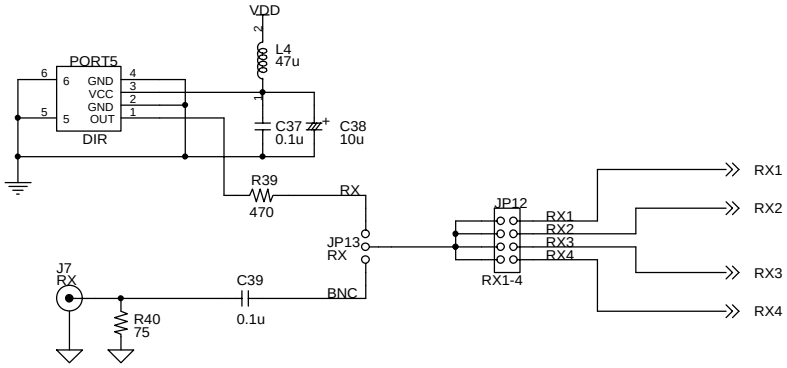
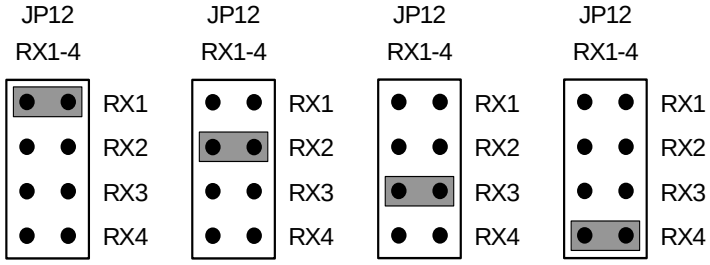
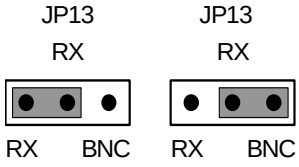


Figure 4. Digital input circuit

1. Digital signal is input to RX1-4 pins respectively.



2. Digital signal is input to RX1-4 pins via J7 (RX) and PORT5 (DIR).



* AKM assumes no responsibility for the trouble when using the above circuit examples.

(2) Digital output circuits

The digital output of AK4584 inputs from J6 (TX) or PORT4 (DIT).

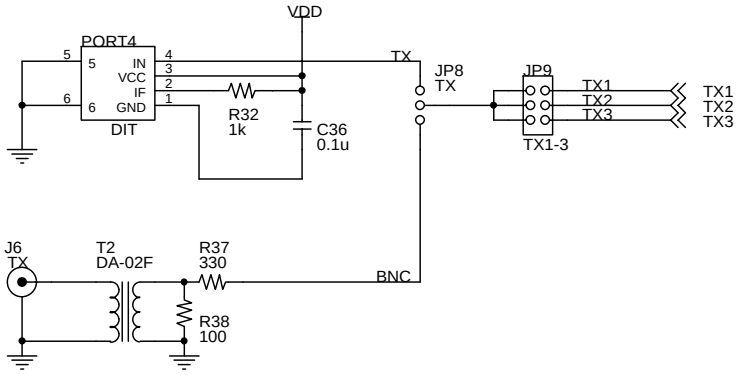
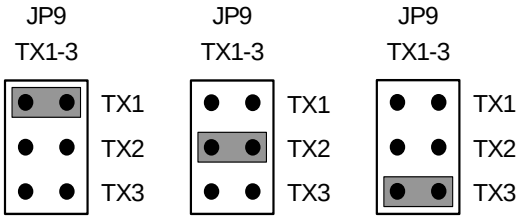
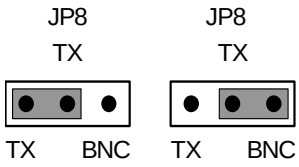


Figure 5. Digital output circuit

1. Digital signal is output to TX1-3 pins respectively.



2. Digital signal is output to TX1-3 pins via J6 (TX) and PORT4 (DIT).



* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Operation sequence

1) Set up the power supply lines.

[AVDD]	(Red)	= 4.75 ~ 5.25V	: for AVDD, DVDD, PVDD of AK4584 (typ. 5.0V)
[TVDD]	(Orange)	= 2.7 ~ 5.25V	: for TVDD of AK4584 (typ. 3.0V)
[VCC]	(Red)	= 5.0V	: for logic (typ. 5.0V)
[VDD]	(Red)	= 5.0V	: for logic (typ. 5.0V)
[AGND]	(Black)	= 0V	: for analog ground
[DGND]	(Black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4584 should be reset once bringing SW1 "L" upon power-up.

■ Evaluation mode

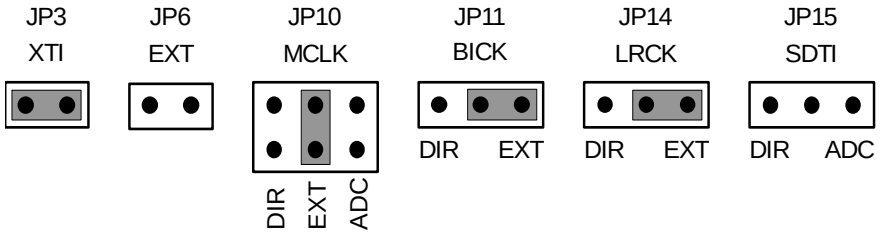
(1) Slave mode

In case of AK4584 evaluation using AK4114, it is necessary to correspond to AK4584's and AK4114's audio interface format. About AK4584's audio interface format, refer to AK4584's datasheet. About AK4114's audio interface format, see Table2.

(1-1) A/D evaluation using DIT function of AK4584
(1-2) A/D evaluation using DIT function of AK4114
(1-3) D/A evaluation using DIR function of AK4114
(1-4) All interfacing signal (MCLK, BICK, LRCK) are fed from the external circuit

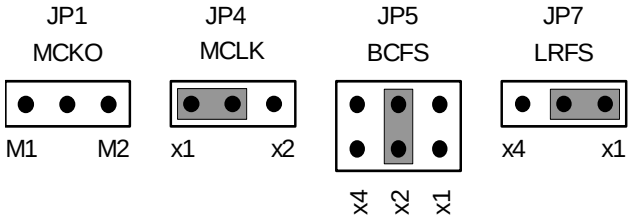
(1-1) A/D evaluation using DIT function of AK4584

Using J5 (EXT), PORT4 (DIT) and J6 (TX). Nothing should be connected to J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). The bi-phase data is output from TX3. JP6 (EXT) should be open.

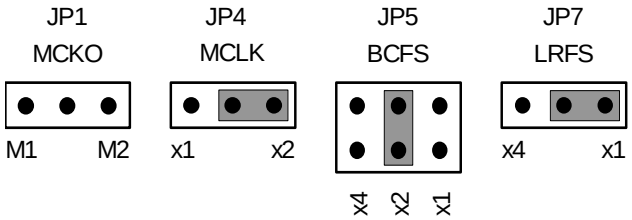


• Clock setting

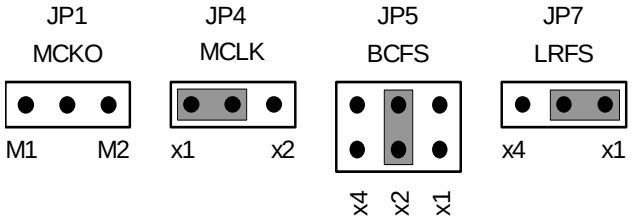
(1-1-1) Normal Speed (MCLK=256fs=11.2896MHz@fs=44.1kHz)



(1-1-2) Normal Speed (MCLK=512fs=22.5792MHz@fs=44.1kHz)

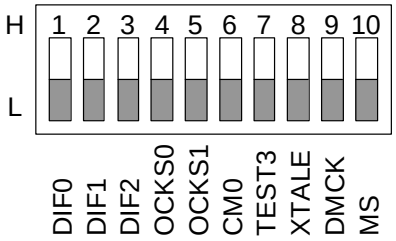


(1-1-3) Double Speed (MCLK=256fs=22.5792MHz@fs=88.2kHz)



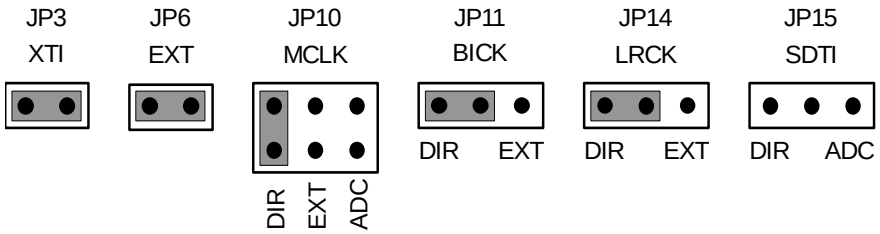
• SW2 (MODE) setting (See Table 1)

Normal speed and double speed are same setting.
(1) When XTALE is “H”, MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(2) When DMCK is “H”, MCKO1 output is disabled.



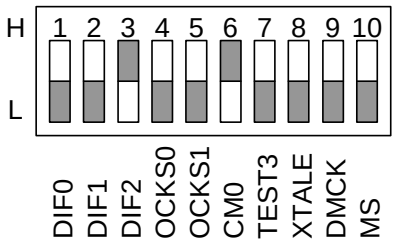
(1-2) A/D evaluation using DIT function of AK4114

Using X'tal (X2) and PORT2 (DIT). Nothing should be connected to J5 (EXT), J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed and double speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



• SW2 (MODE) setting (See Table 1)

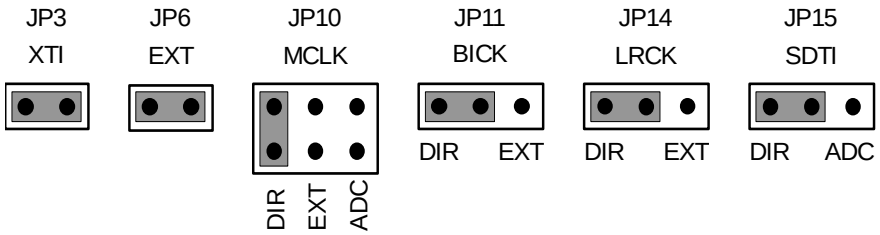
Normal speed and double speed are same setting.
(1) Set the audio interface format of AK4114 using DIF2-0.
(2) Set the master clock output of AK4114using OCKS1-0.
(3) Set the PLL mode or X'tal mode of AK4114 using CM0.
(4) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(5) When DMCK is "H", MCKO1 output is disabled.



Above figure is 24bit MSB justified, MCKO output of AK4114 is 256fs, AK4114 is X'tal mode.
Using DIT of AK4114, AK4114 is set X'tal mode.

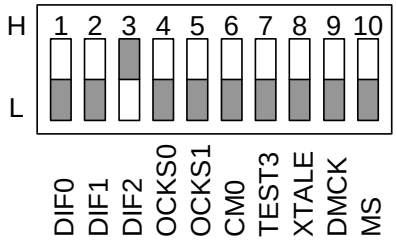
(1-3) D/A evaluation using DIR function of AK4114

Using PORT1 (DIR). Nothing should be connected to J7 (RX), PORT5 (DIR) and PORT6 (ROM). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



- SW2 (MODE) setting (See Table 1)

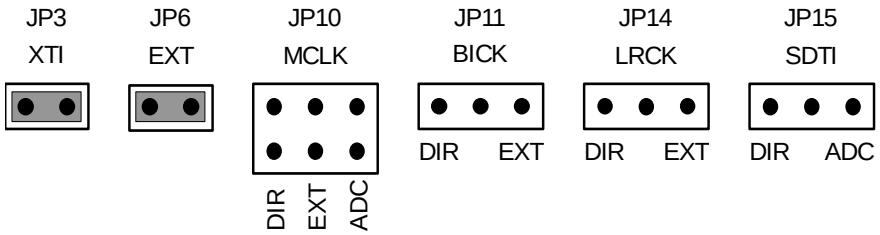
(1) Set the audio interface format of AK4114 using DIF2-0.
(2) Set the master clock output of AK4114using OCKS1-0.
(3) Set the PLL mode or X'tal mode of AK4114 using CM0.
(4) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(5) When DMCK is "H", MCKO1 output is disabled.



Above figure is 24bit MSB justified, MCKO output of AK4114 is 256fs, AK4114 is PLL mode.
In quad speed mode of AK4114, set OCKS1="H" and OCKS0="H". The MCKO output of AK4114 is output 128fs.

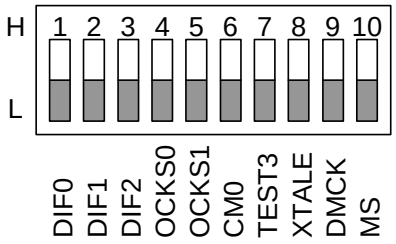
(1-4) All interfacing signal (MCLK, BICK, LRCK) are fed from the external circuit

Using PORT6 (ROM). Nothing should be connected to J7 (RX), PORT1 (DIR) and PORT5 (DIR). Remove the X'tal (X1). JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.



- SW2 (MODE) setting (See Table 1)

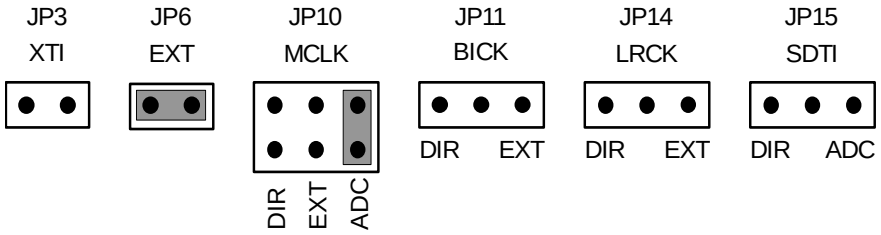
(1) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(2) When DMCK is "H", MCKO1 output is disabled.



(2) Master Mode

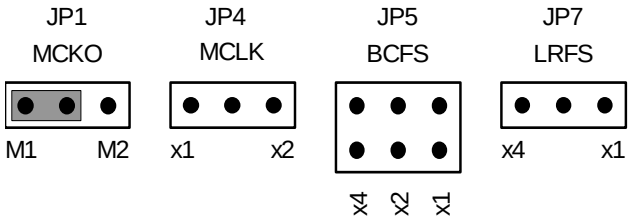
(2-1) A/D evaluation using DIT function of AK4584

Using X'tal (X1), PORT4 (DIT) and J6 (TX). Nothing should be connected to J7 (RX), PORT1 (DIR), PORT5 (DIR) and PORT6 (ROM). The bi-phase data is output from TX3. JP6 (EXT) should be short. In normal speed, double speed mode and quad speed mode, JP3 (XTI), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.

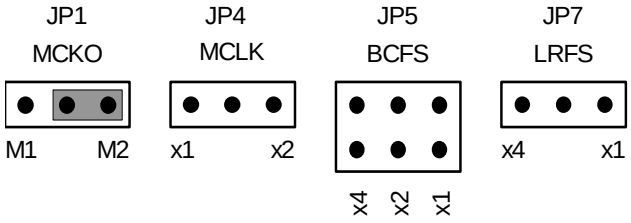


• Clock Setting

(2-1-1) Select MCKO1

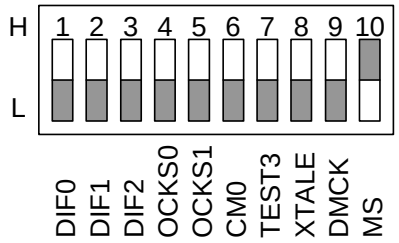


(2-1-2) Select MCKO2



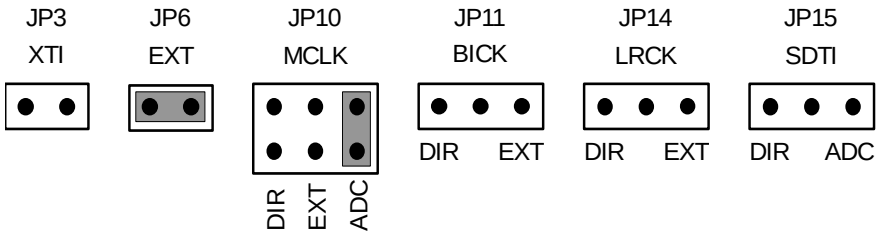
• SW2 (MODE) setting (See Table 1)

Normal speed and double speed are same setting.
(1) When XTALE is "H", MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(2) When DMCK is "H", MCKO1 output is disabled.



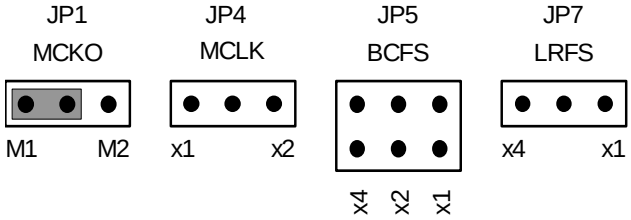
(2-2) D/A evaluation using DIR function of AK4584

Using PORT5 (DIR) or J7 (RX). Nothing should be connected to PORT1 (DIR) and PORT6 (ROM). JP6 (EXT) should be short. In normal speed and double speed mode, JP1 (MCKO), JP4 (MCLK), JP5 (BCFS) and JP7 (LRFS) should be open.

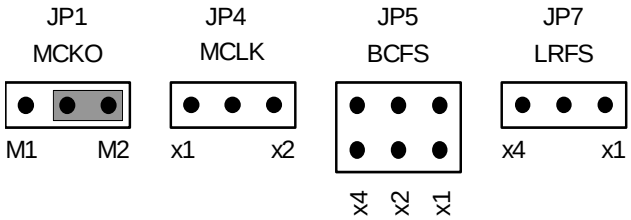


• Clock setting

(2-2-1) Select MCKO1

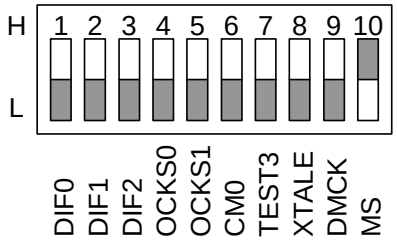


(2-2-2) Select MCKO2



• SW2 (MODE) setting (See Table 1)

Normal speed, double speed and quad speed mode are same setting.
(1) When XTALE is “H”, MCLK can output from MCKO1/2 pins though AK4584 is powered down.
(2) When DMCK is “H”, MCKO1 output is disabled.



■ DIP Switch set up

[SW2] (MODE): Setting evaluation mode for AK4584 and AK4114
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")
1	DIF0	AK4114 Audio Format Setting See Table 2	
2	DIF1		
3	DIF2		
4	OCKS0	AK4114 Master Clock Output Setting See Table 3	
5	OCKS1		
6	CM0	AK4114 X'tal Mode	AK4114 PLL Mode
7	TEST3	Normally OFF	
8	XTALE	MCKO1/2 Enable	MCKO1/2 Disable
9	DMCK	MCKO1 Disable	MCKO1 Enable
10	M/S	Master Mode	Slave Mode

Table 1. Setting mode for AK4584 and AK4114

Mode	DIF2	DIF1	DIF0	AK4114 DAUX	AK4114 SDTO
0	0	0	0	24bit, MSB justified	16bit, LSB justified
1	0	0	1	24bit, MSB justified	18bit, LSB justified
2	0	1	0	24bit, MSB justified	20bit, LSB justified
3	0	1	1	24bit, MSB justified	24bit, LSB justified
4	1	0	0	24bit, MSB justified	24bit, MSB justified
5	1	0	1	24bit, I^2S	24bit, I^2S

Table 2. Setting AK4114 audio interface format

Mode	OCKS1	OCKS0	MCKO1	X'tal	fs
0	0	0	256fs	256fs	~ 96kHz
1	0	1	256fs	256fs	~ 96kHz
2	1	0	512fs	512fs	~ 48kHz
3	1	1	128fs	128fs	~ 192kHz

Table 3. Setting AK4114 master clock output

■ Other jumper pins set up

1. JP1 (GND): Analog ground and Digital ground
OPEN: Separated. <Default>
SHORT: Common. (The connector "DGND" can be open.)

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Power down of AK4584. Keep "H" during normal operation.

[SW3] (DIR): Power down of AK4114. Keep "H" during normal operation.

■ Indication for LED

[LED1] (INT0): Output INT0 pin of AK4584.

[LED2] (INT1): Output INT1 pin of AK4584.

[LED3] (ERF): Output INT0 pin of AK4114.

[LED4] (DZF): Output DZF pin of AK4584.

■ Serial Control

The AK4584 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CTRL) with PC by 10 wire flat cable packed with the AKD4584.

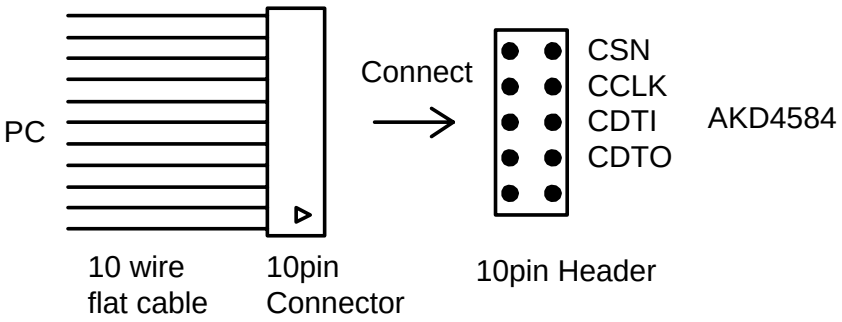


Figure 6. Connect of 10 wire flat cable

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4584 according to previous term.

2. Connect IBM-AT compatible PC with AKD4584 by 10-line type flat cable (packed with AKD4584). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled “AKD4584 Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “akd4584.exe” to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click “Port Reset” button.

■ Explanation of each buttons

1. [Port Reset]: Set up the USB interface board (AKDUSBIF-A).
2. [Write default]: Initialize the register of AK4584.
3. [All Write]: Write all registers that is currently displayed.
4. [Function1]: Dialog to write data by keyboard operation.
5. [Function2]: Dialog to write data by keyboard operation.
6. [Function3]: The sequence of register setting can be set and executed.
7. [Function4]: The sequence that is created on [Function3] can be assigned to buttons and executed.
8. [Function5]: The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
9. [SAVE]: Save the current register setting.
10. [OPEN]: Write the saved values to all register.
11. [Write]: Dialog to write data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”.
Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog]: Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog.
If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

When writing the input data to AK4584, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog]: Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

When writing the input data to AK4584, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog]: Dialog to evaluate GAIN/ATT
This dialog corresponds to address 04H, 05H, 06H, and 07H.

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4584 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

With checking this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

Without checking this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

When writing the input data to AK4584, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4584. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set “-1” to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is “aks”.

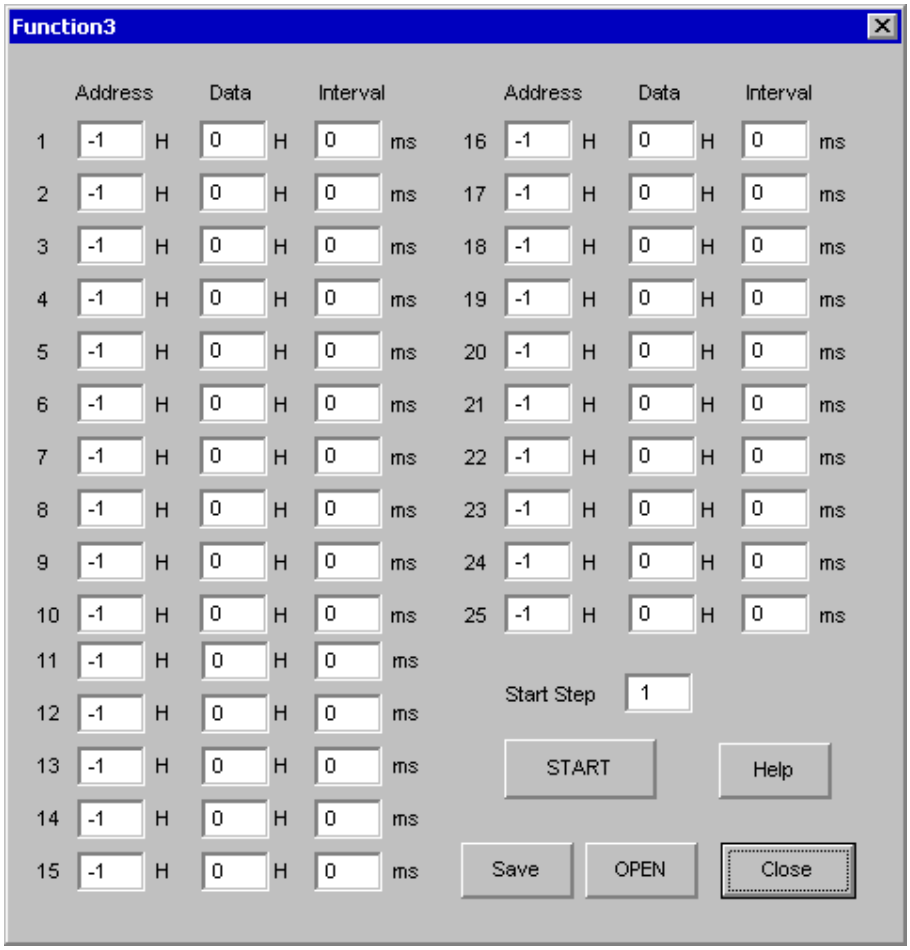


Figure 1. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 2 opens.

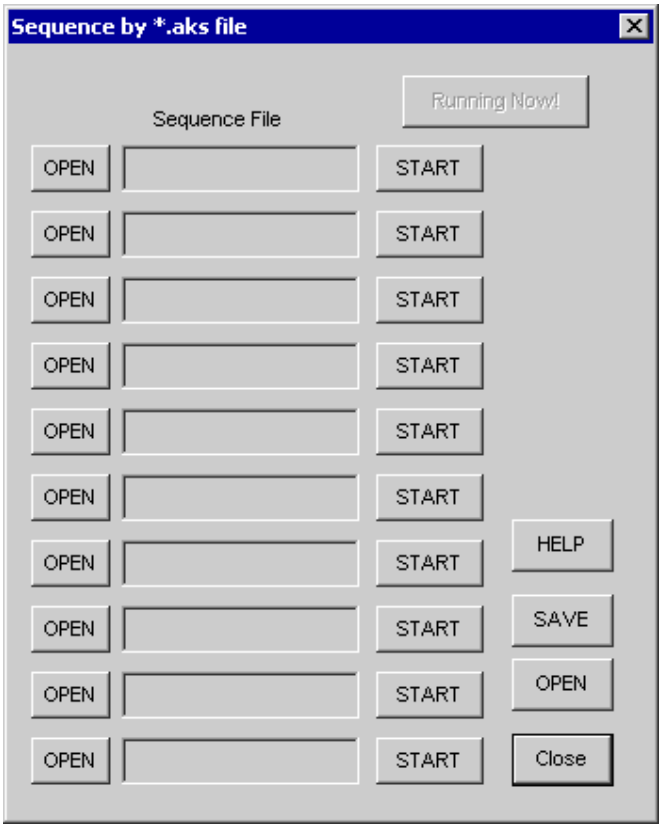


Figure 2. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 3.

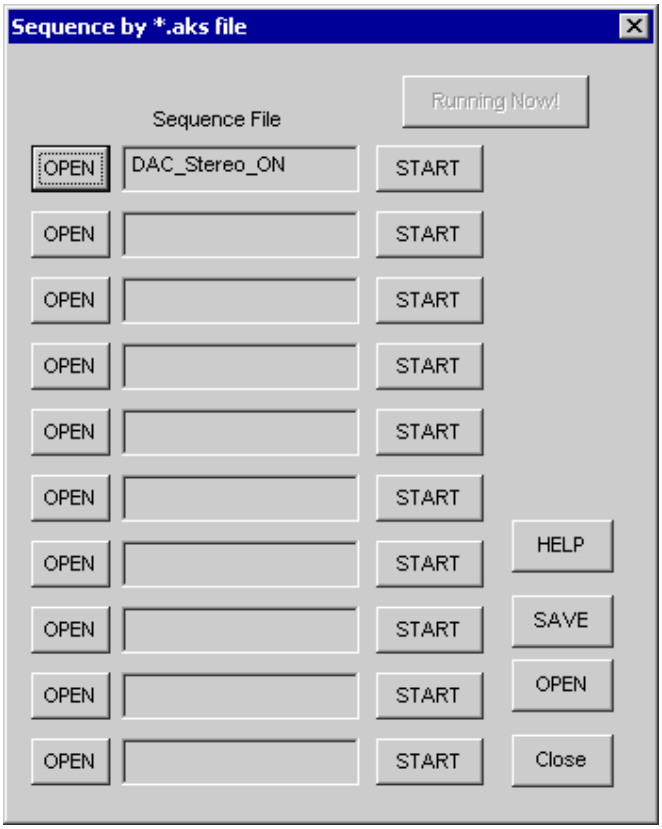


Figure 3. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The sequence file names can assign be saved. The file name is *.ak4.

[OPEN]: The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 4opens.

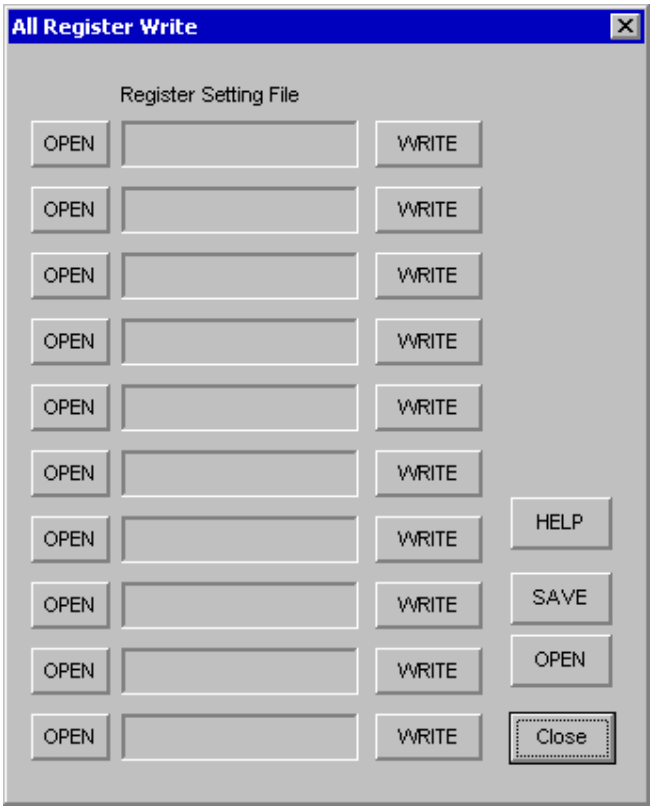


Figure 4. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

(2) Click [WRITE] button, then the register setting is executed.

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE]: The register setting file names assign can be saved. The file name is *.ak5.

[OPEN]: The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System Two Cascade
- MCLK : 256fs
- BCLK : 64fs
- fs : 44.1kHz, 96kHz
- Bit : 24bit
- Power Supply : AVDD=DVDD=TVDD=PVDD=5.0V
- Interface : DIR/DIT
- Temperature : Room

[Measurement Results]

Parameter	Result	Unit
ADC Analog Input Characteristics		
S/(N+D)		
(fs=44.1kHz, -0.5dB Input)	92.0	dB
(fs=96kHz, -0.5dB Input)	88.3	dB
D-Range		
(fs=44.1kHz, -60dB Input, A-weighted)	100.6	dB
(fs=96kHz, -60dB Input)	96.1	dB
S/N		
(fs=44.1kHz, A-weighted)	101.0	dB
(fs=96kHz)	96.1	dB
Interchannel Isolation	110.5	dB
DAC Analog Output Characteristics		
S/(N+D)		
(fs=44.1kHz, 0dB Output)	95.3	dB
(fs=96kHz, -0.5dB Output)	95.1	dB
D-Range		
(fs=44.1kHz, -60dB Output, A-weighted)	105.5	dB
(fs=96kHz, -60dB Output)	100.4	dB
S/N		
(fs=44.1kHz, A-weighted)	105.9	dB
(fs=96kHz)	100.5	dB
Interchannel Isolation	115.5	dB

[ADC Plot : fs=44.1kHz]

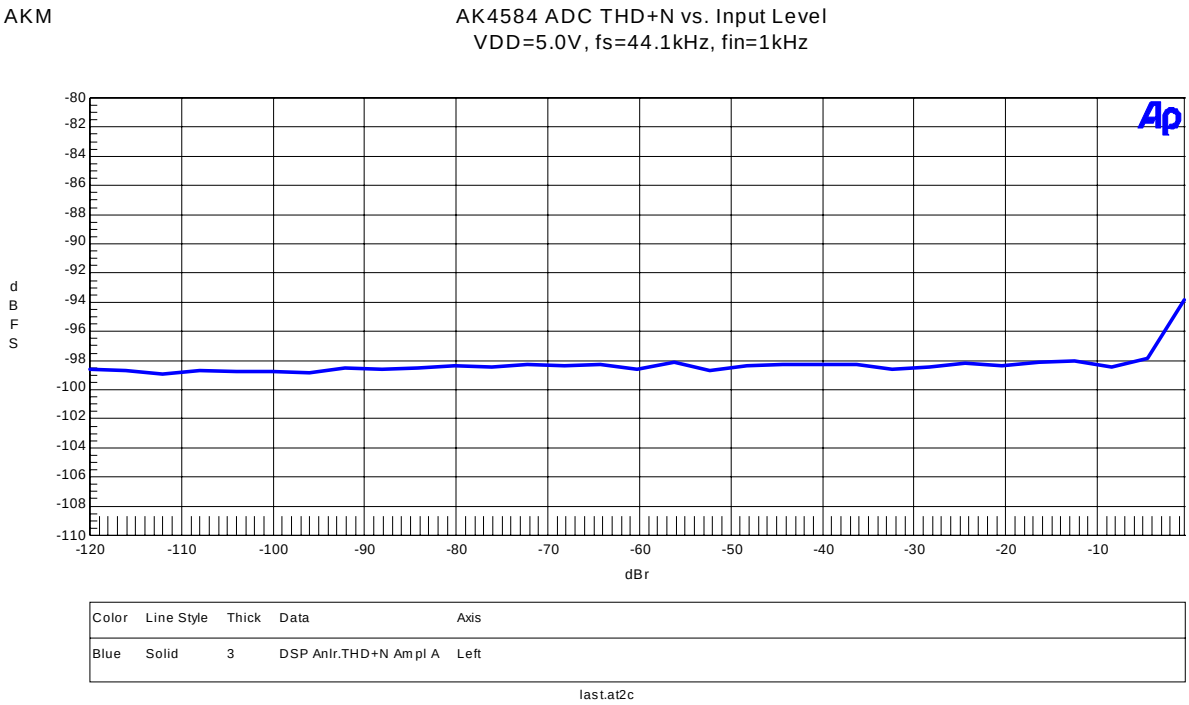


Figure 1. THD+N vs. Input Level

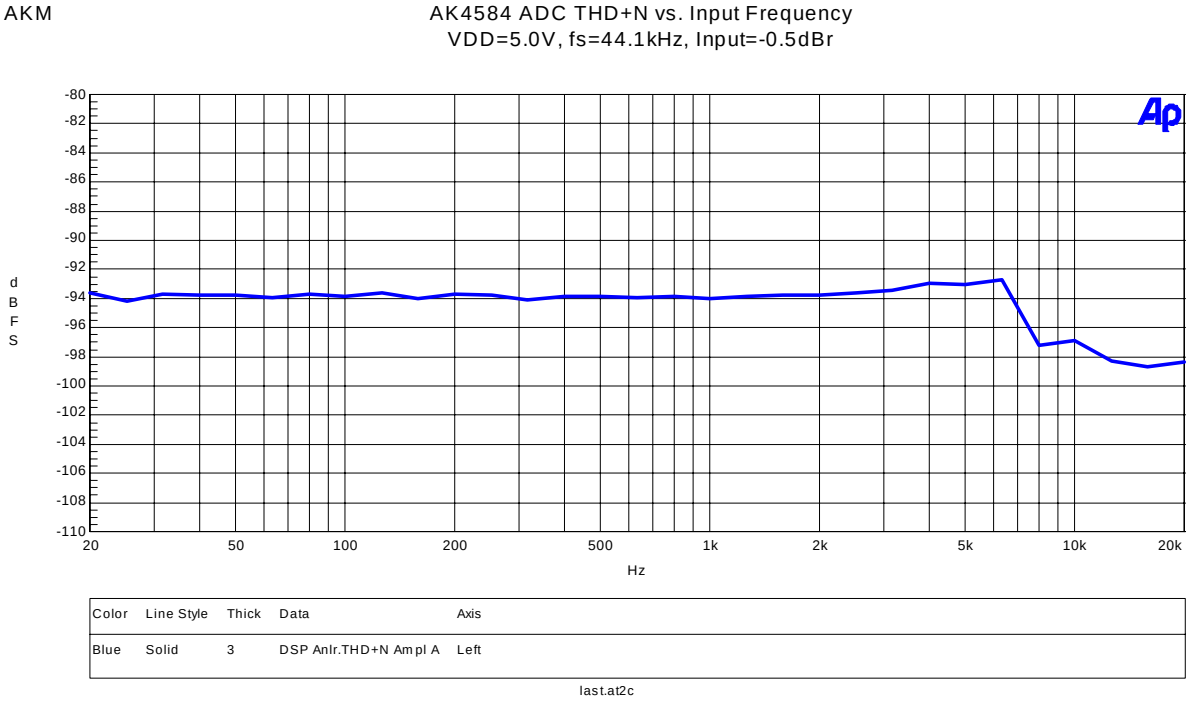


Figure 2. THD+N vs. Input Frequency

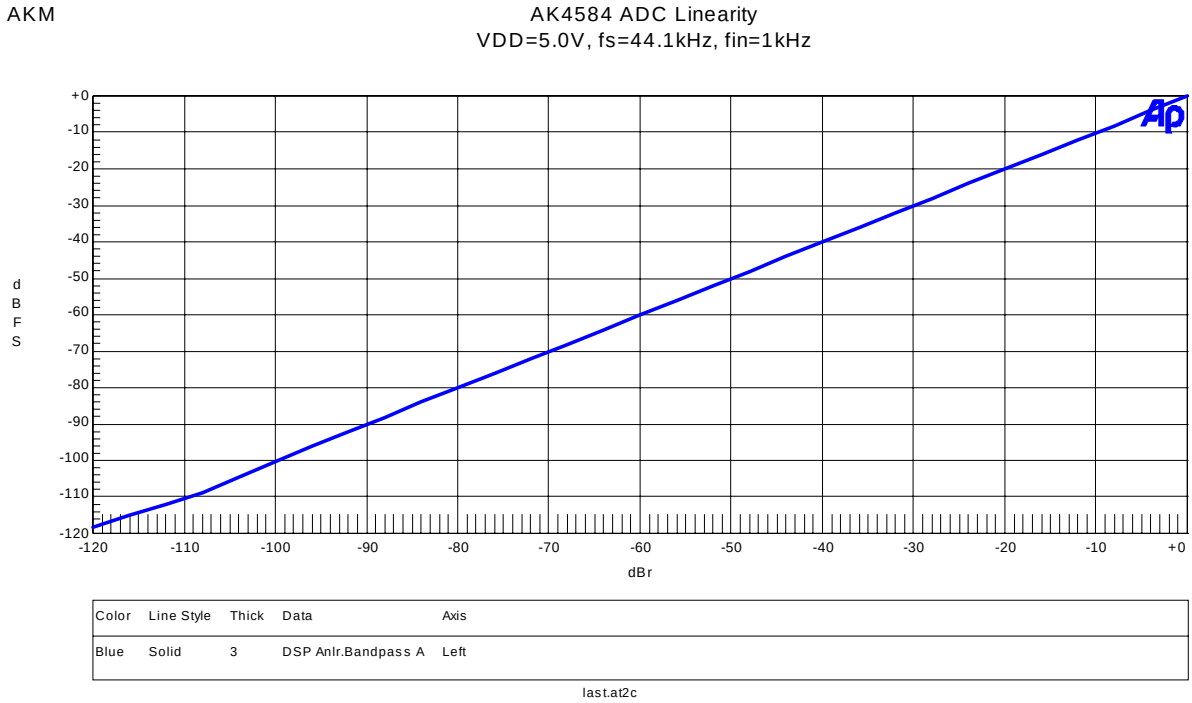


Figure 3. Linearity

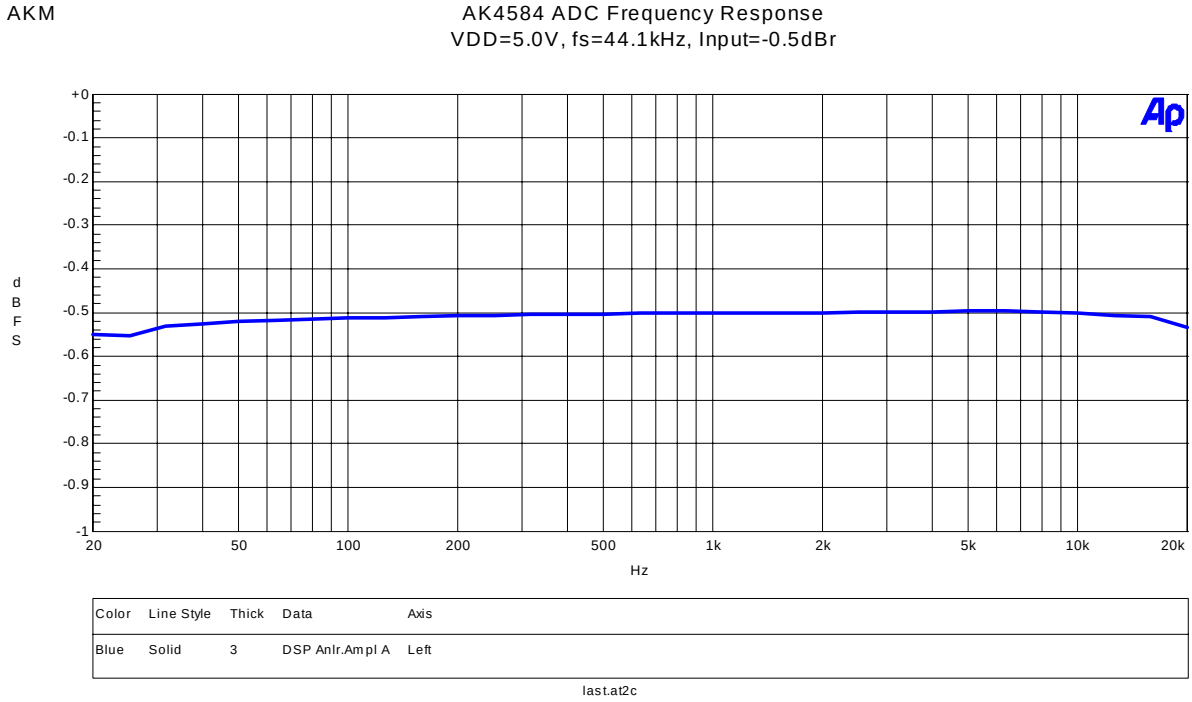


Figure 4. Frequency Response

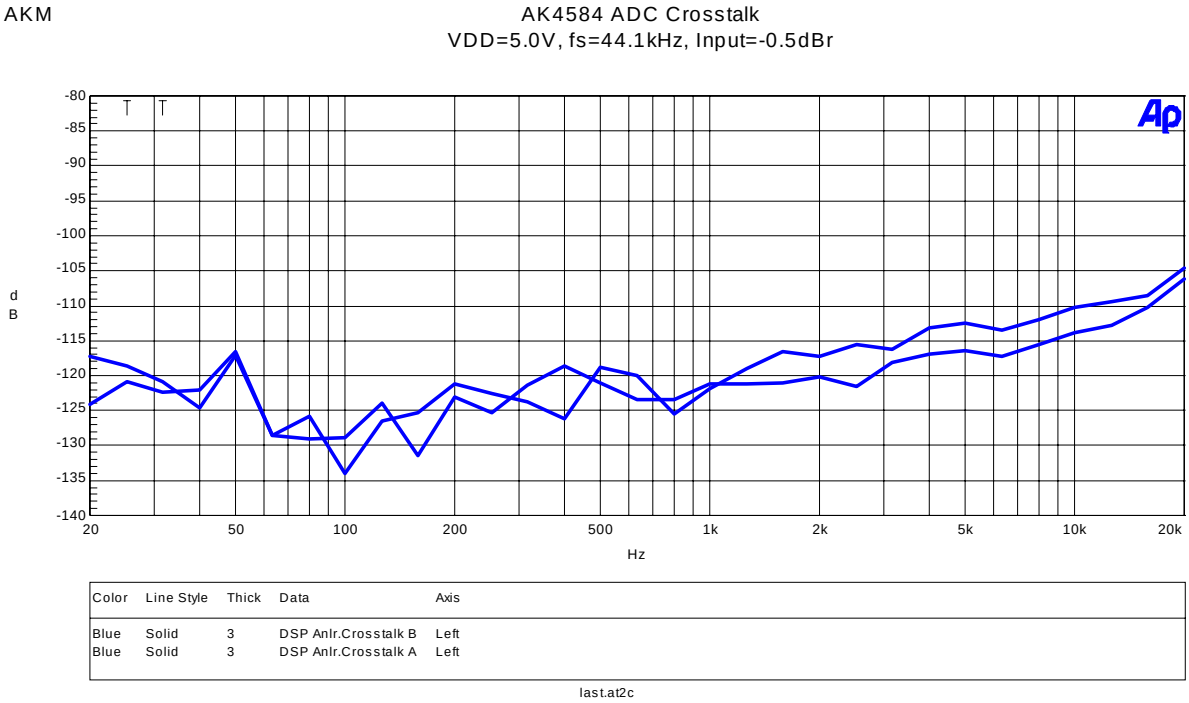


Figure 5. Crosstalk

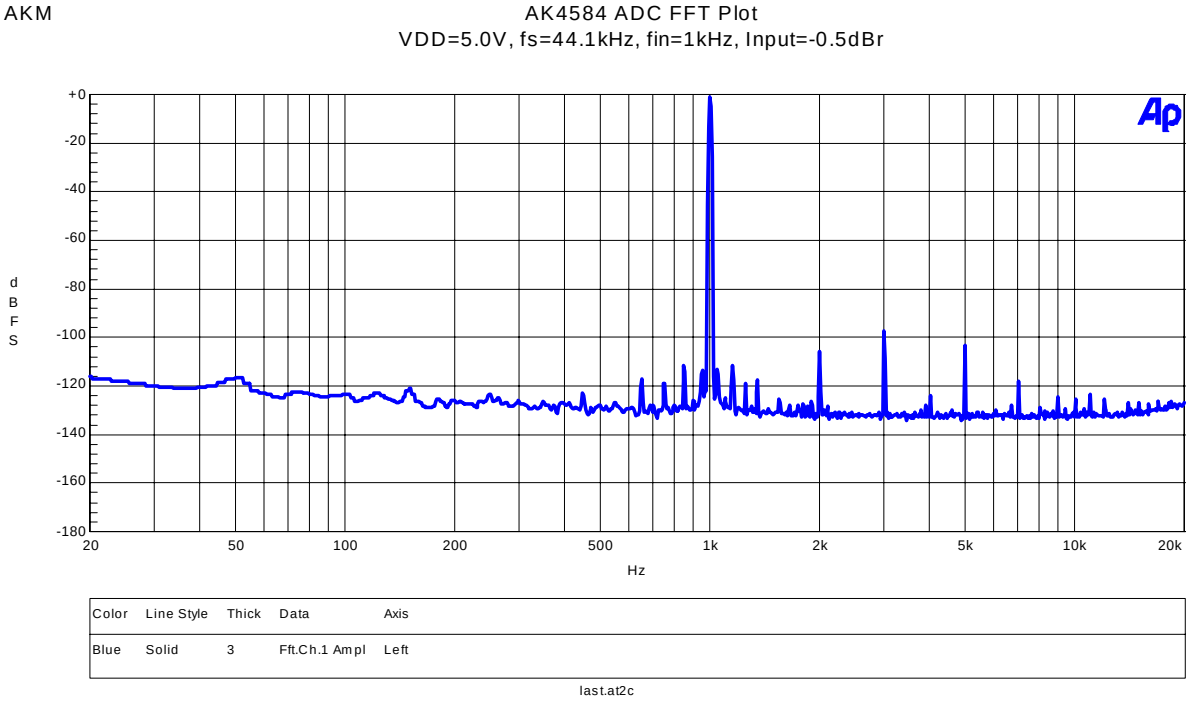


Figure 6. FFT Plot

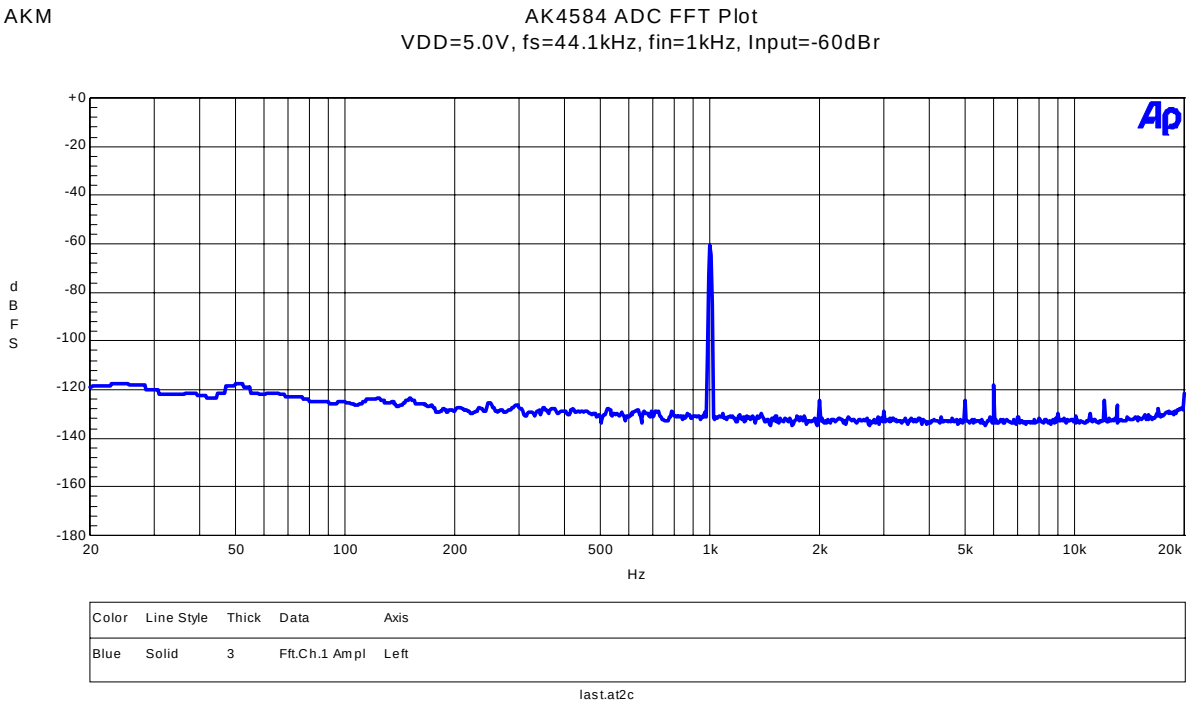


Figure 7. FFT Plot

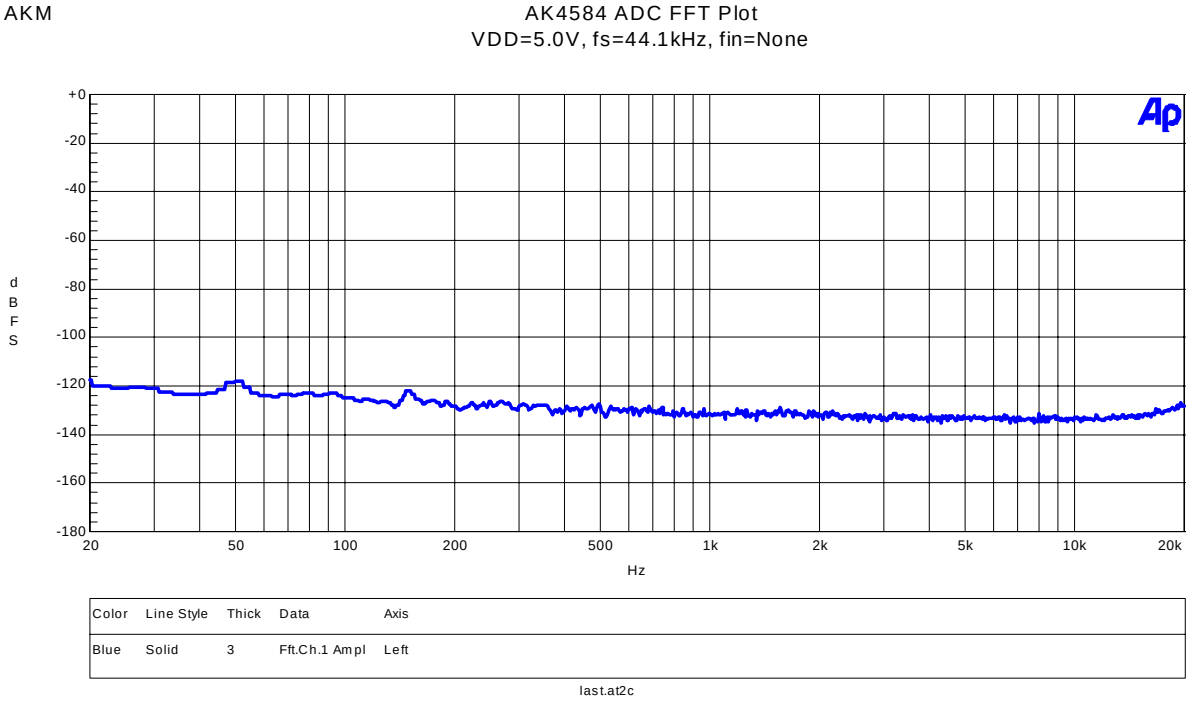


Figure 8. FFT Plot

[ADC Plot : fs=96kHz]

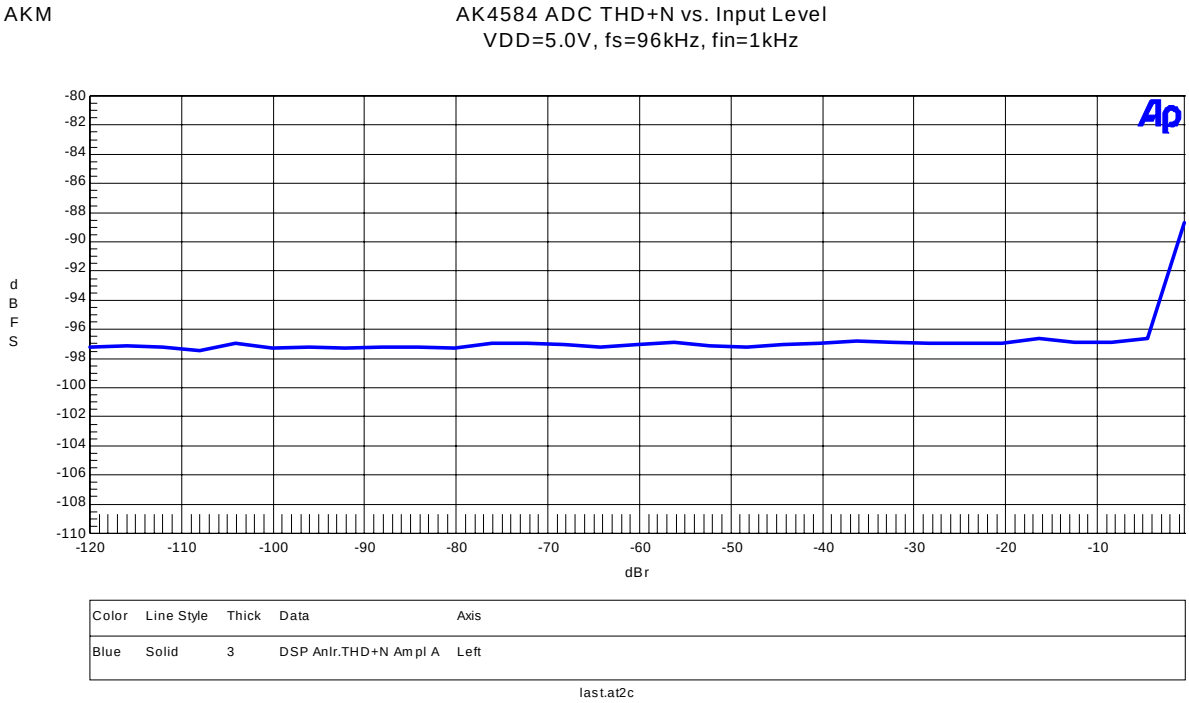


Figure 9. THD+N vs. Input Level

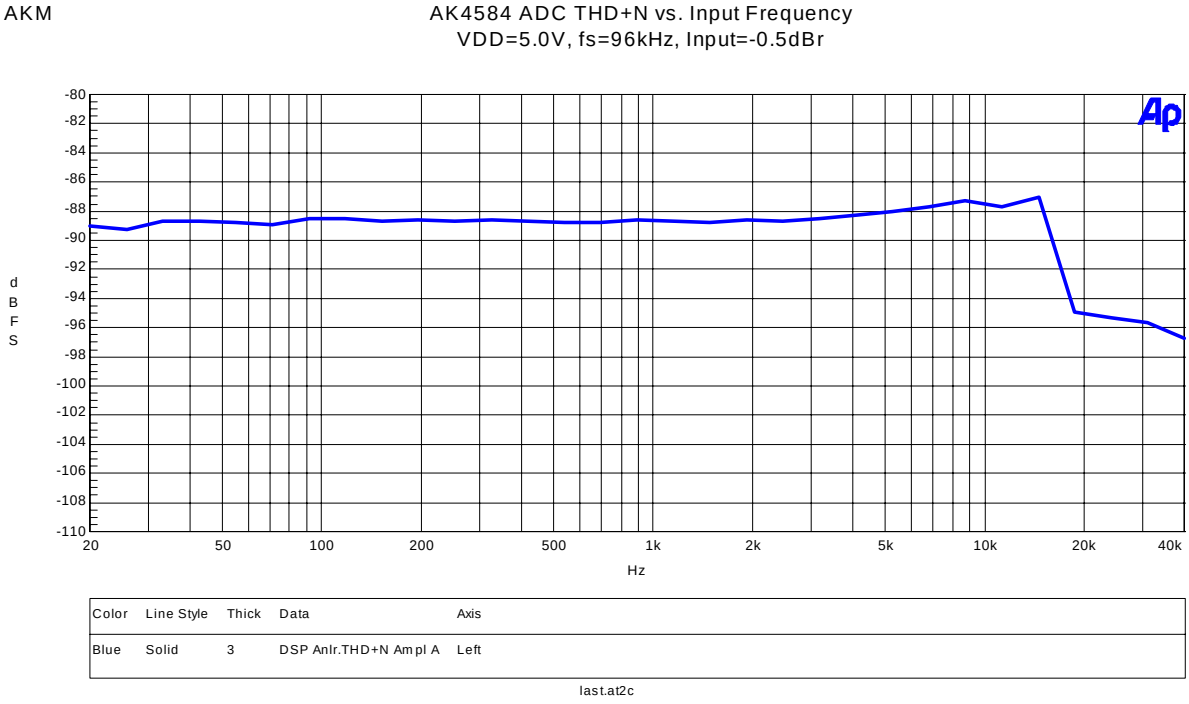


Figure 10. THD+N vs. Input Frequency

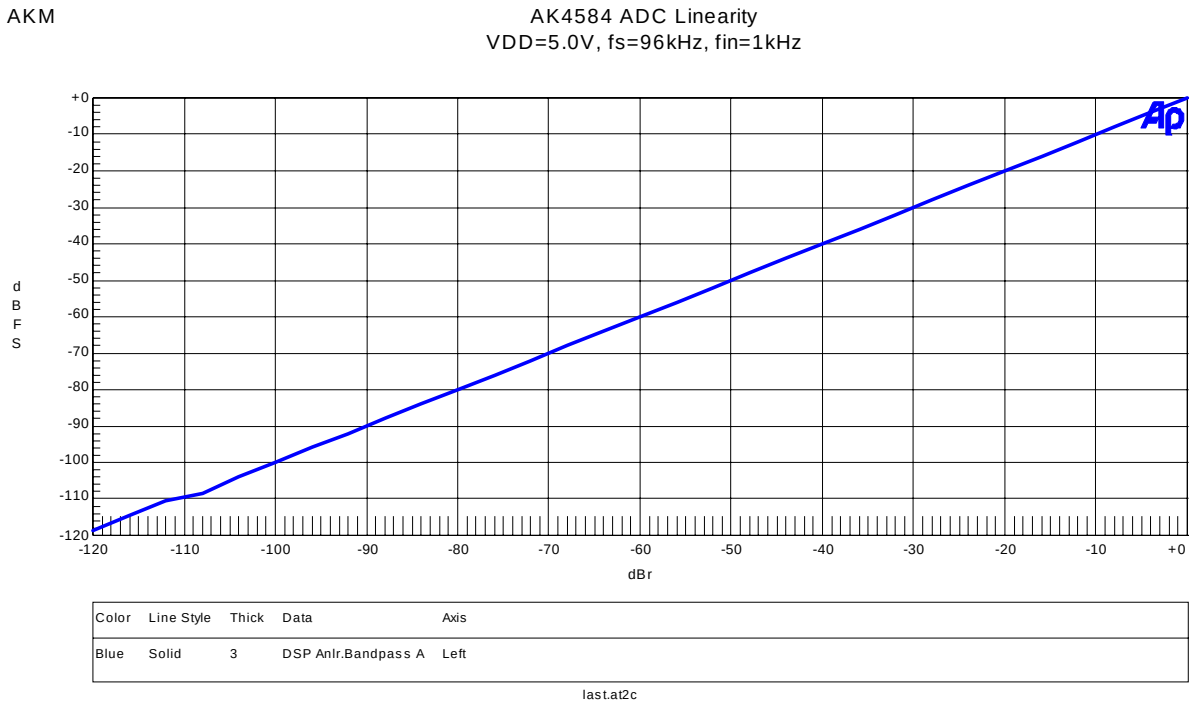


Figure 11. Linearity

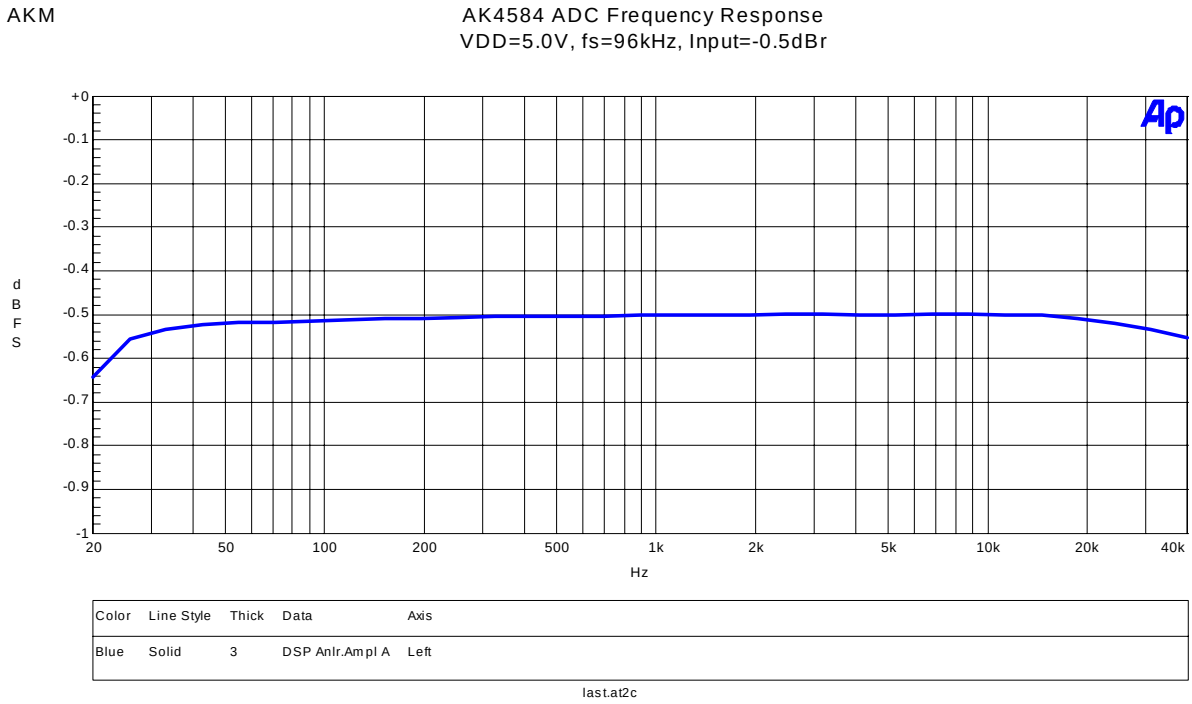


Figure 12. Frequency Response

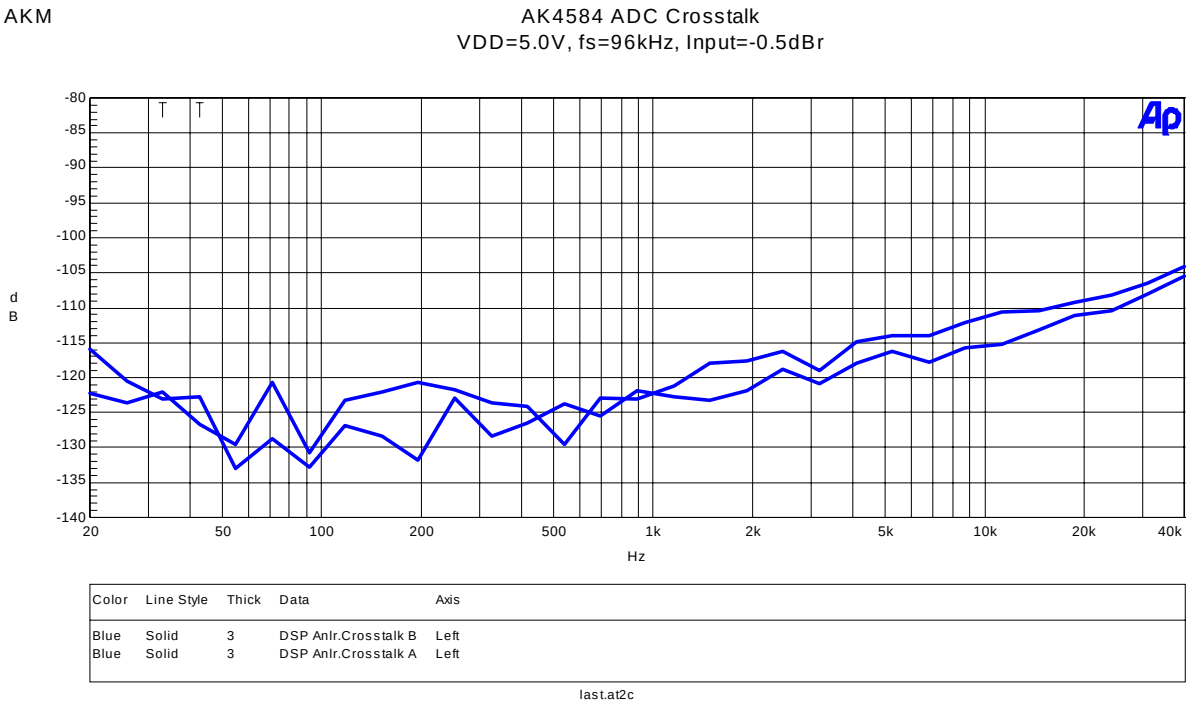


Figure 13. Crosstalk

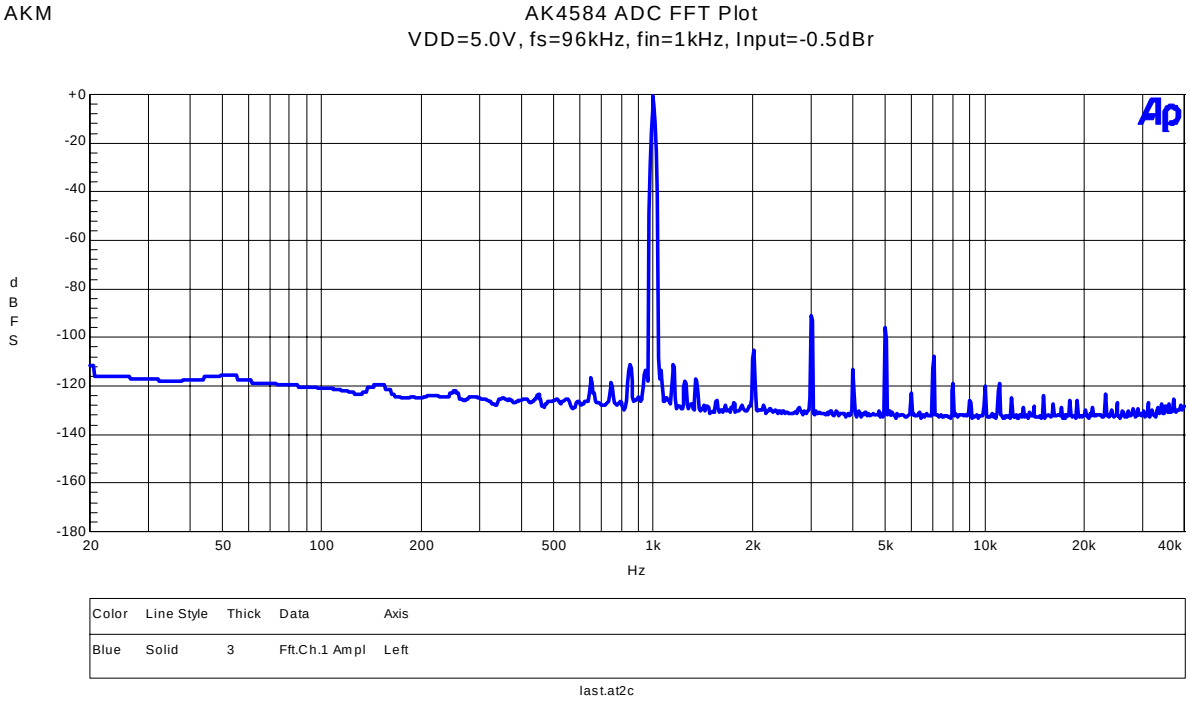


Figure 14. FFT Plot

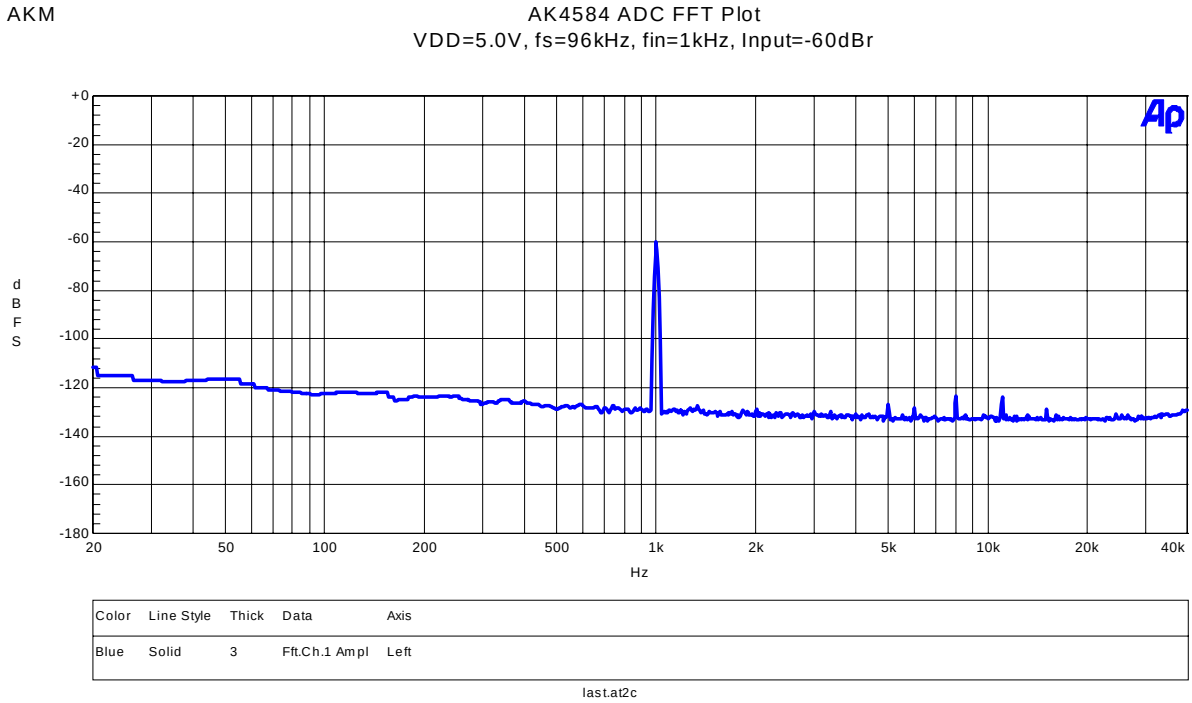


Figure 15. FFT Plot

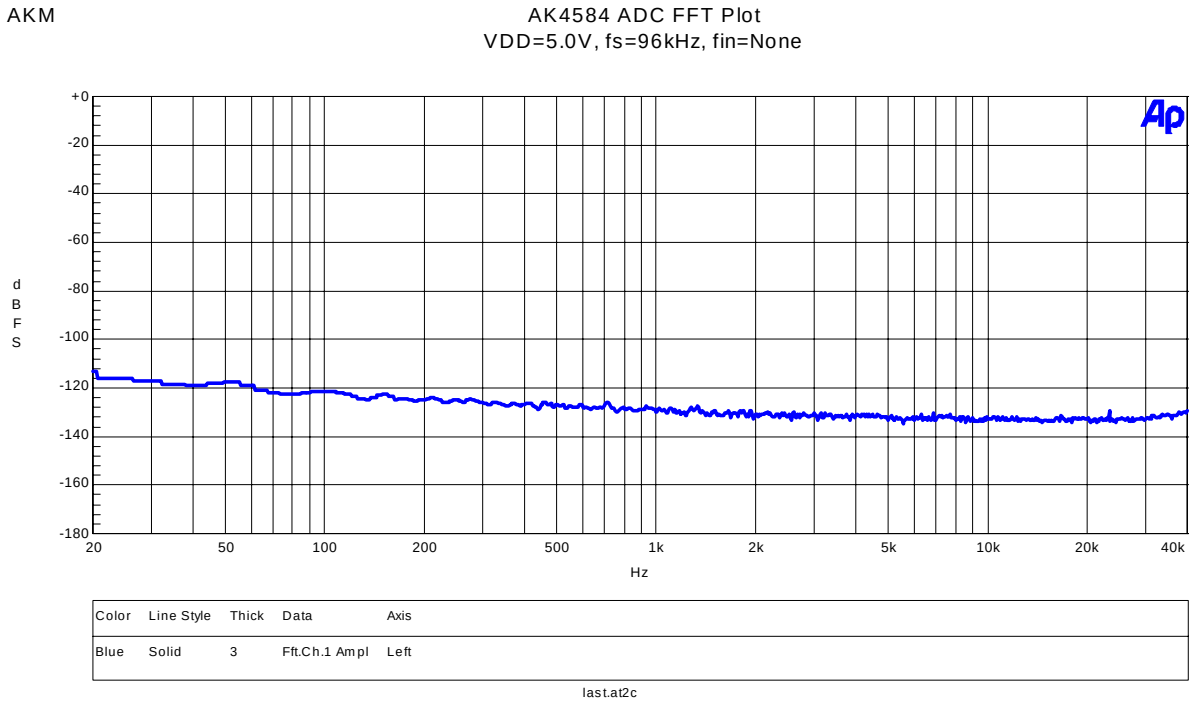


Figure 16. FFT Plot

[DAC Plot : fs=44.1kHz]

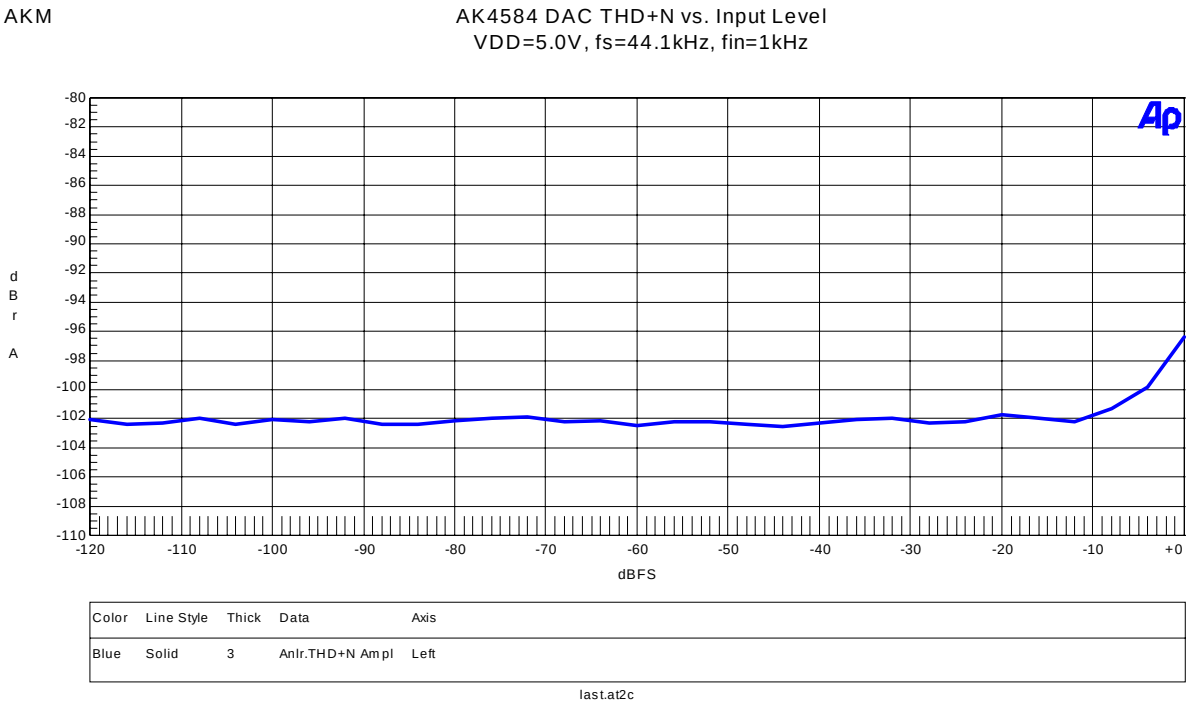


Figure 1. THD+N vs. Input Level

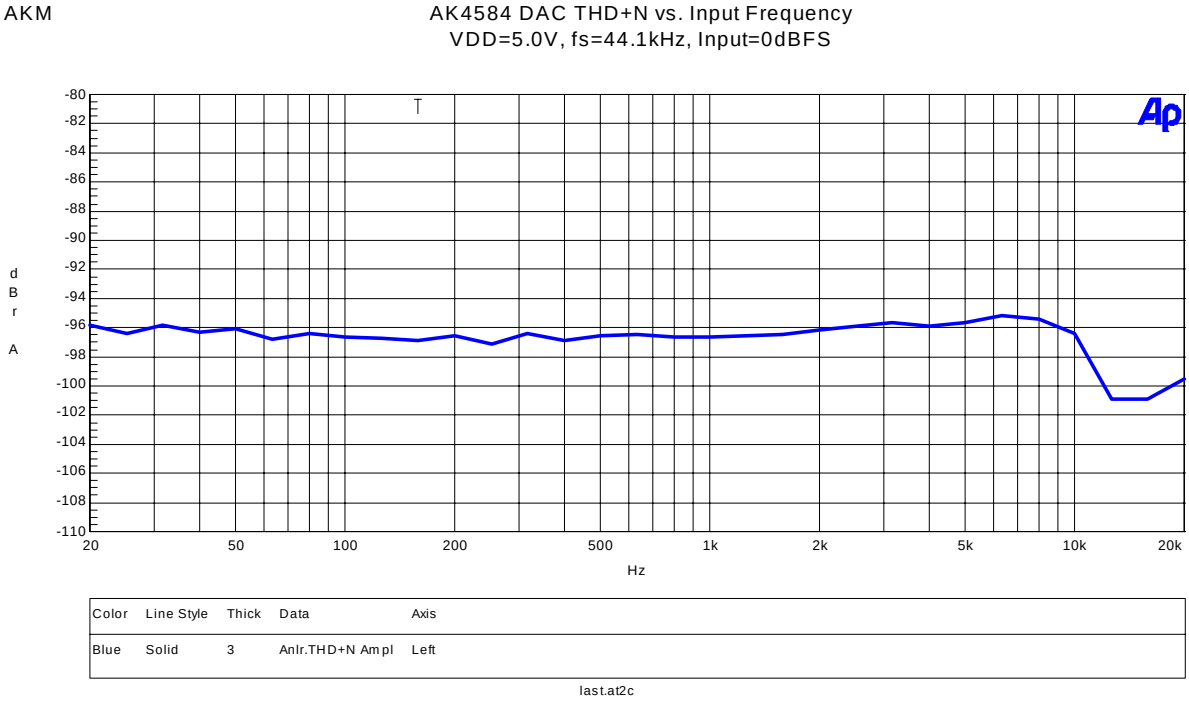


Figure 2. THD+N vs. Input Frequency

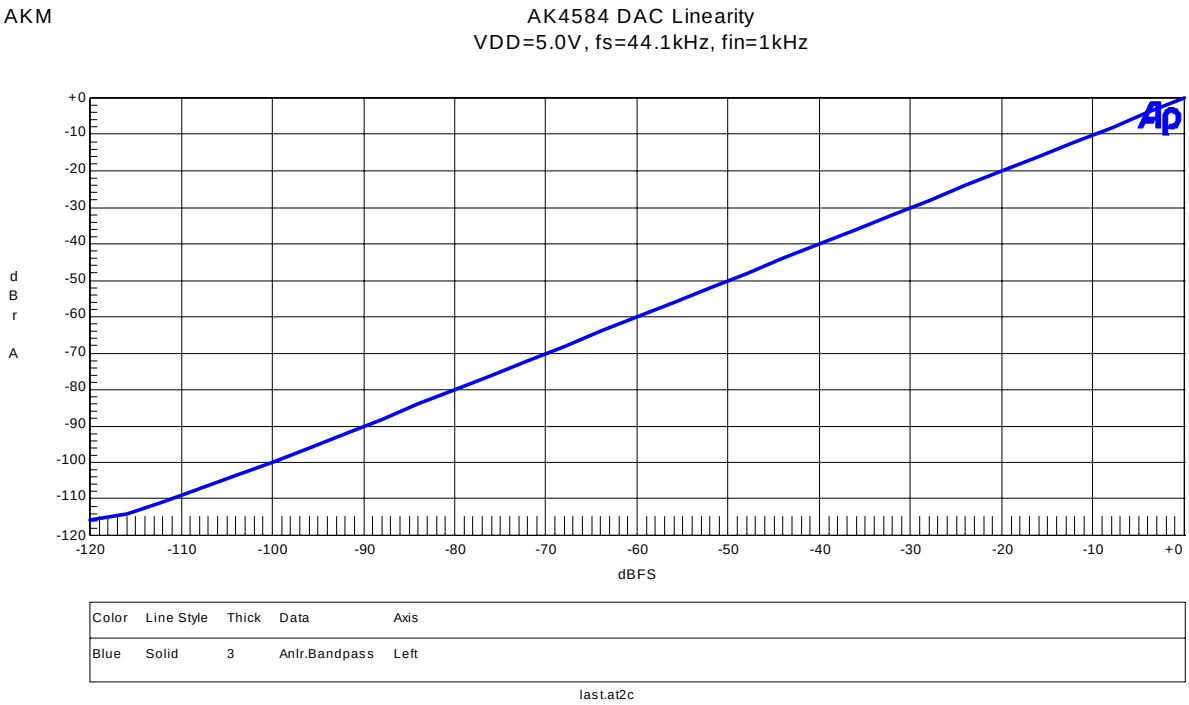


Figure 3. Linearity

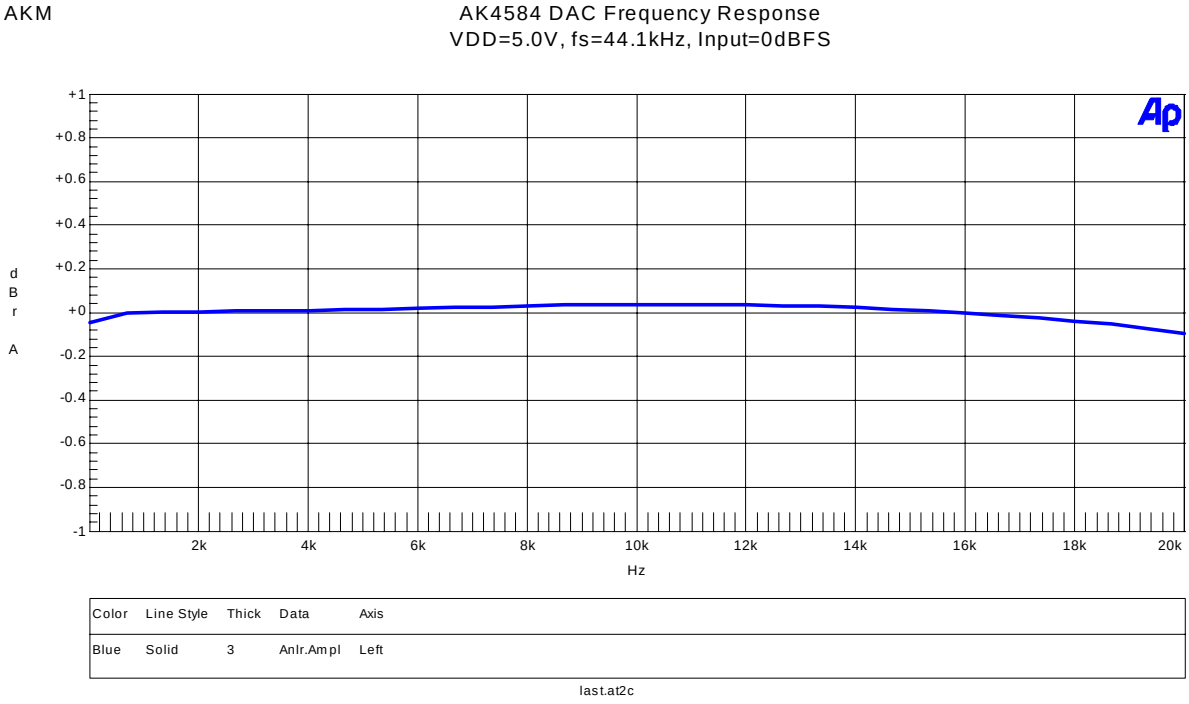


Figure 4. Frequency Response

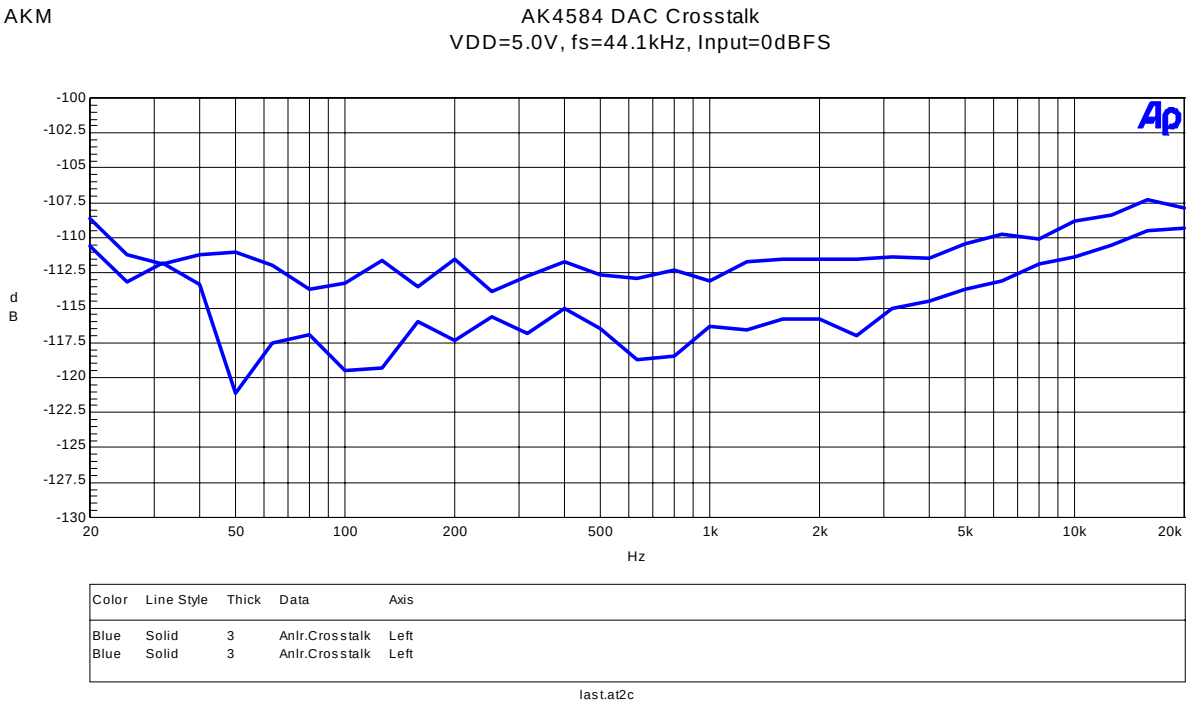


Figure 5. Crosstalk

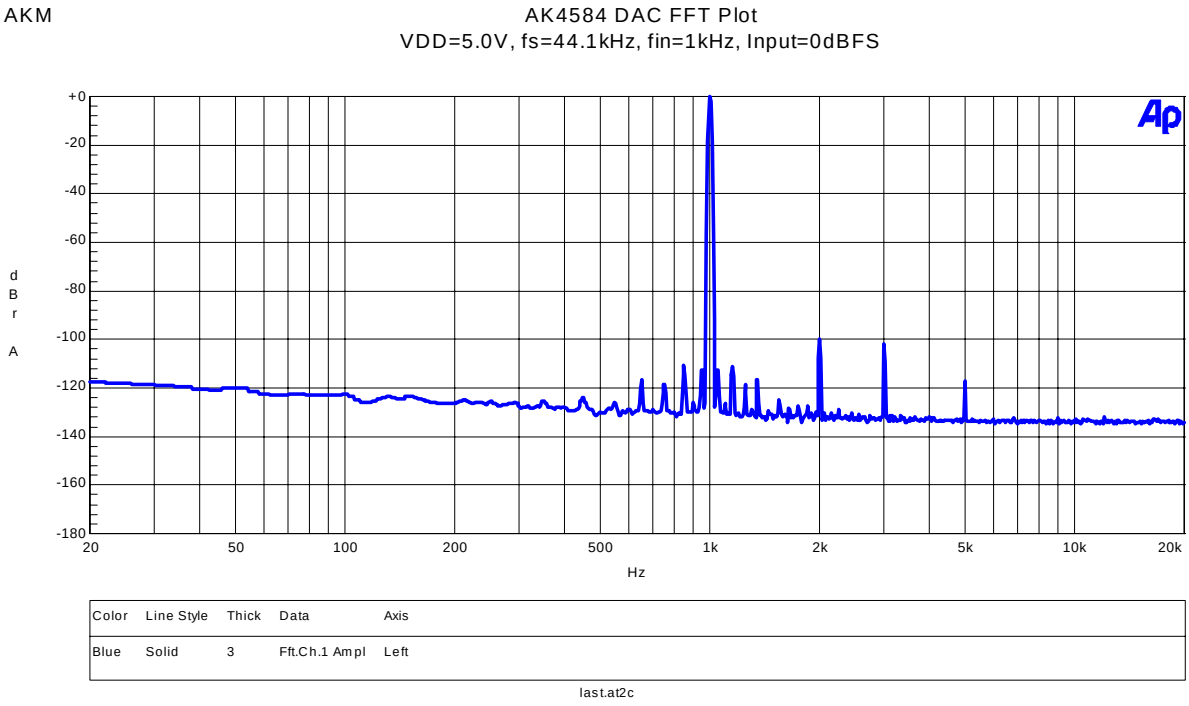


Figure 6. FFT Plot

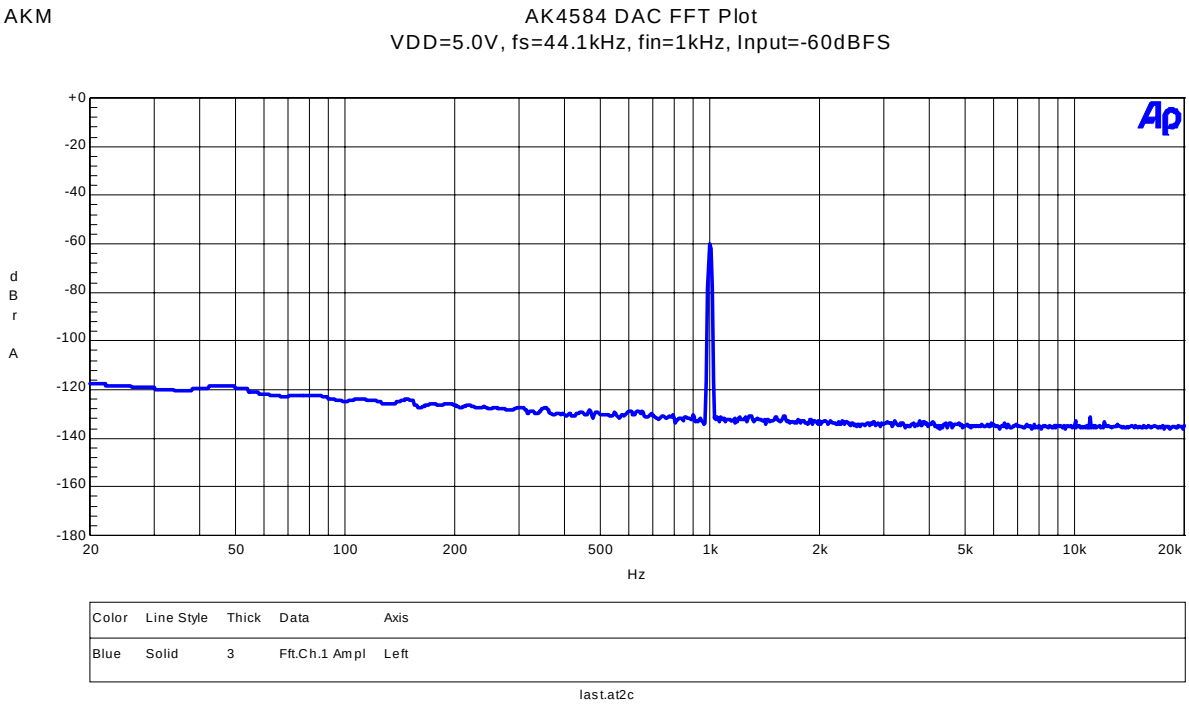


Figure 7. FFT Plot

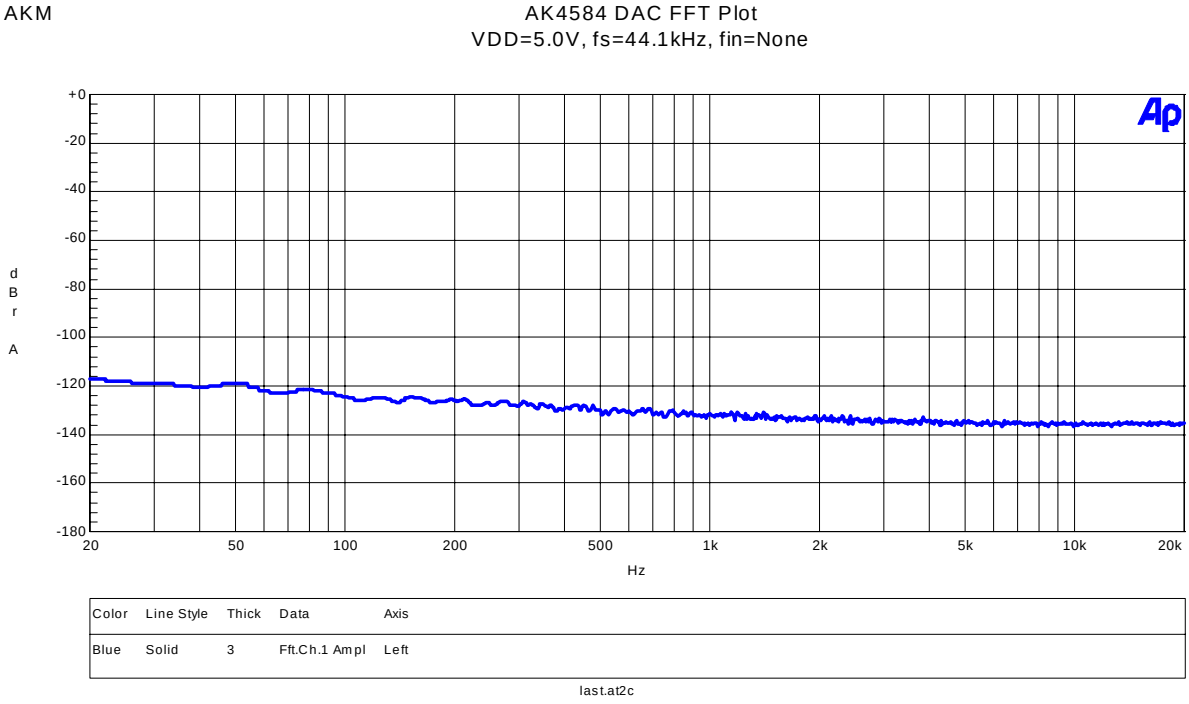


Figure 8. FFT Plot

[DAC Plot : fs=96kHz]

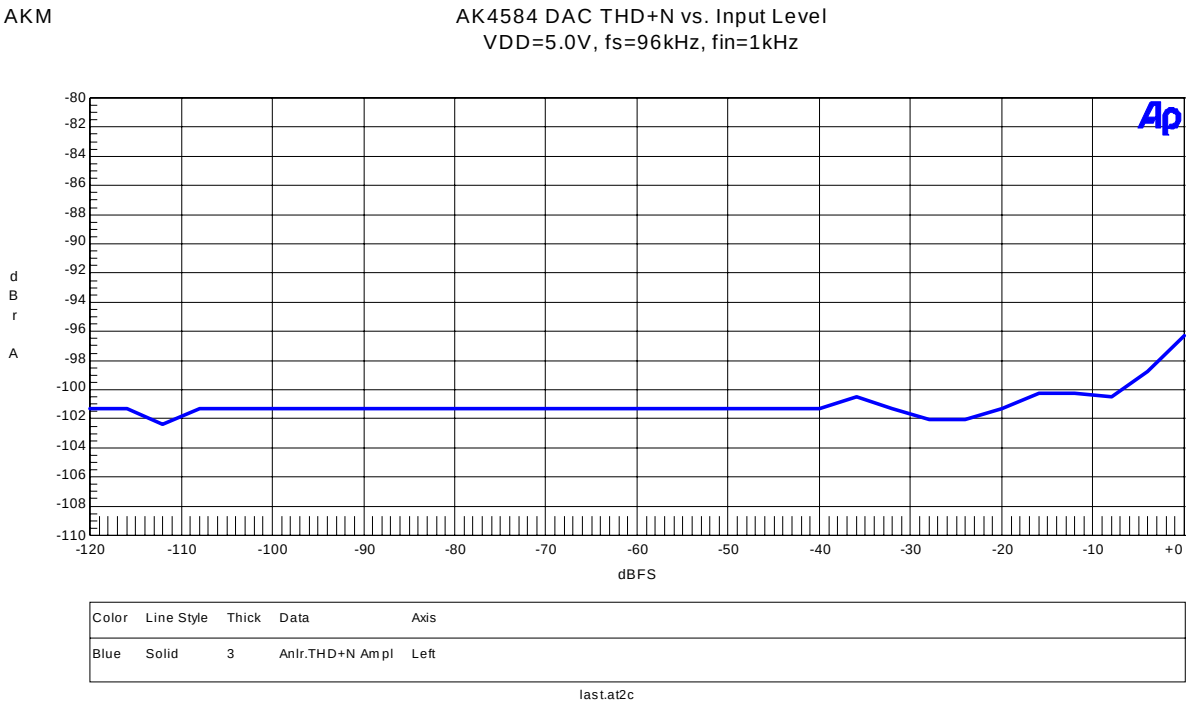


Figure 9. THD+N vs. Input Level

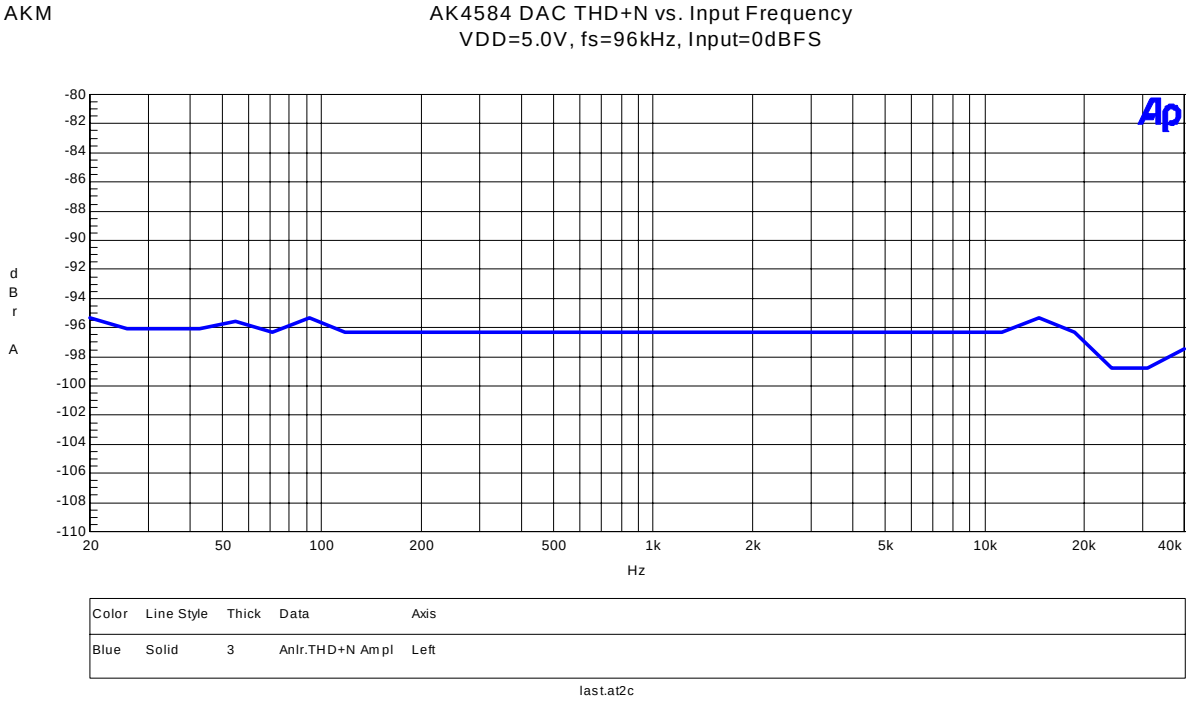


Figure 10. THD+N vs. Input Frequency

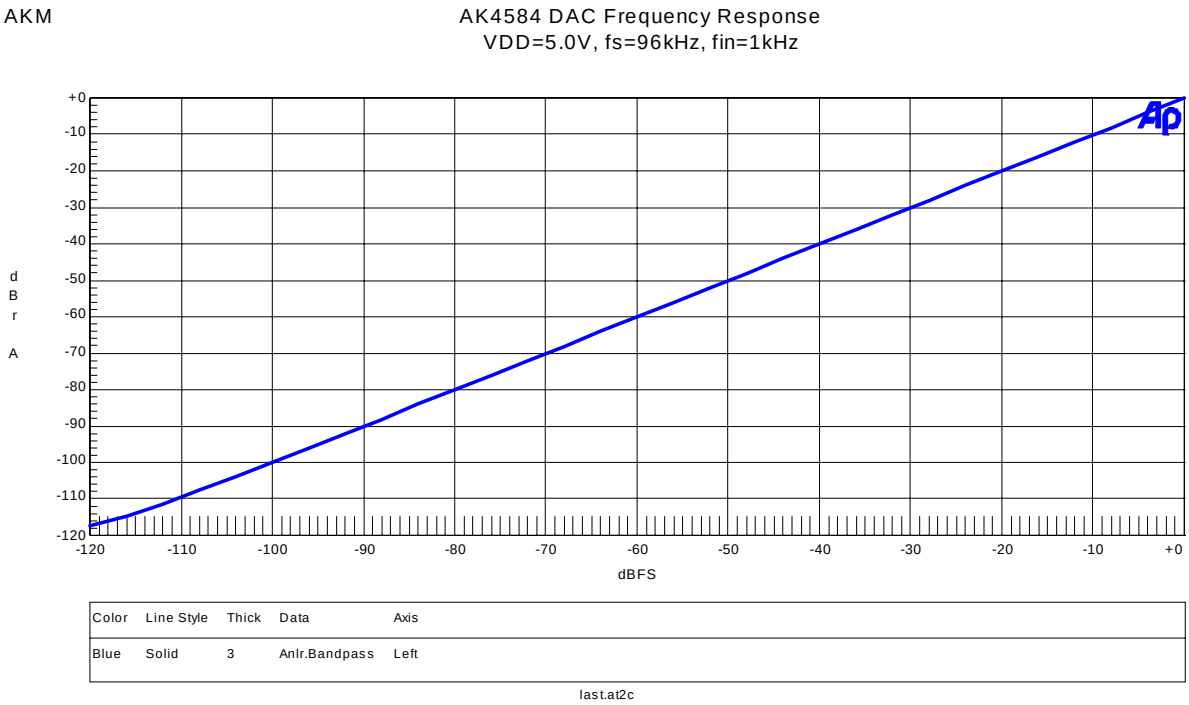


Figure 11. Linearity

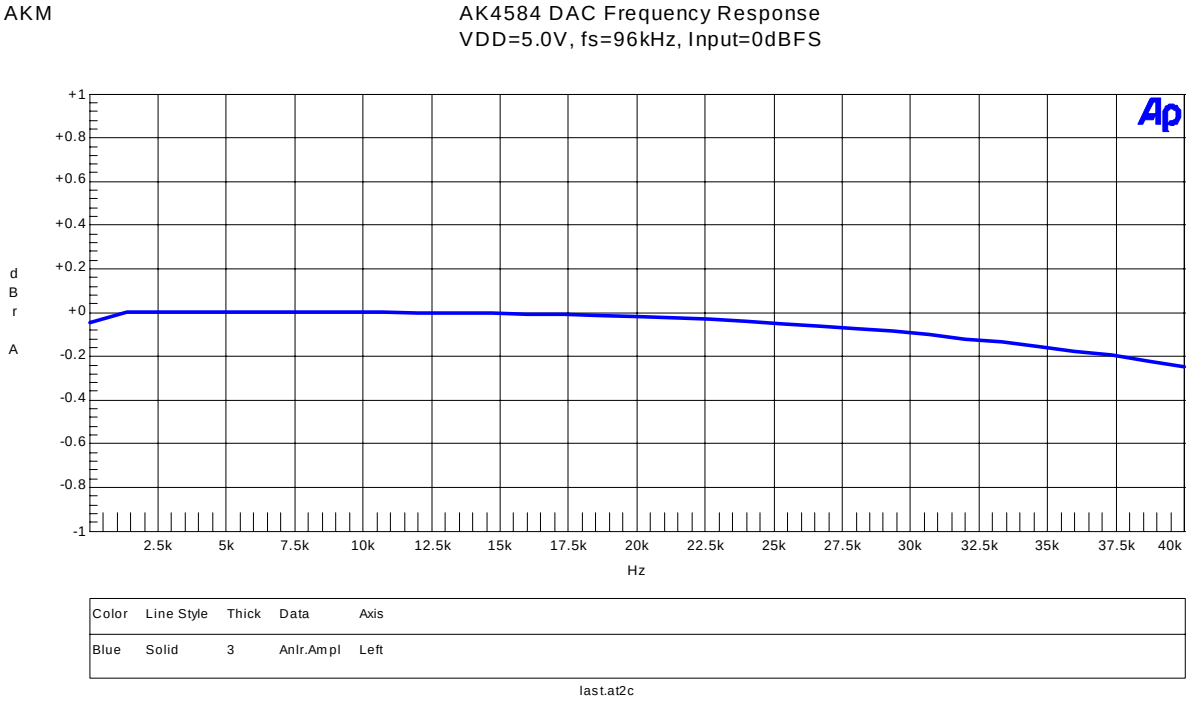


Figure 12. Frequency Response

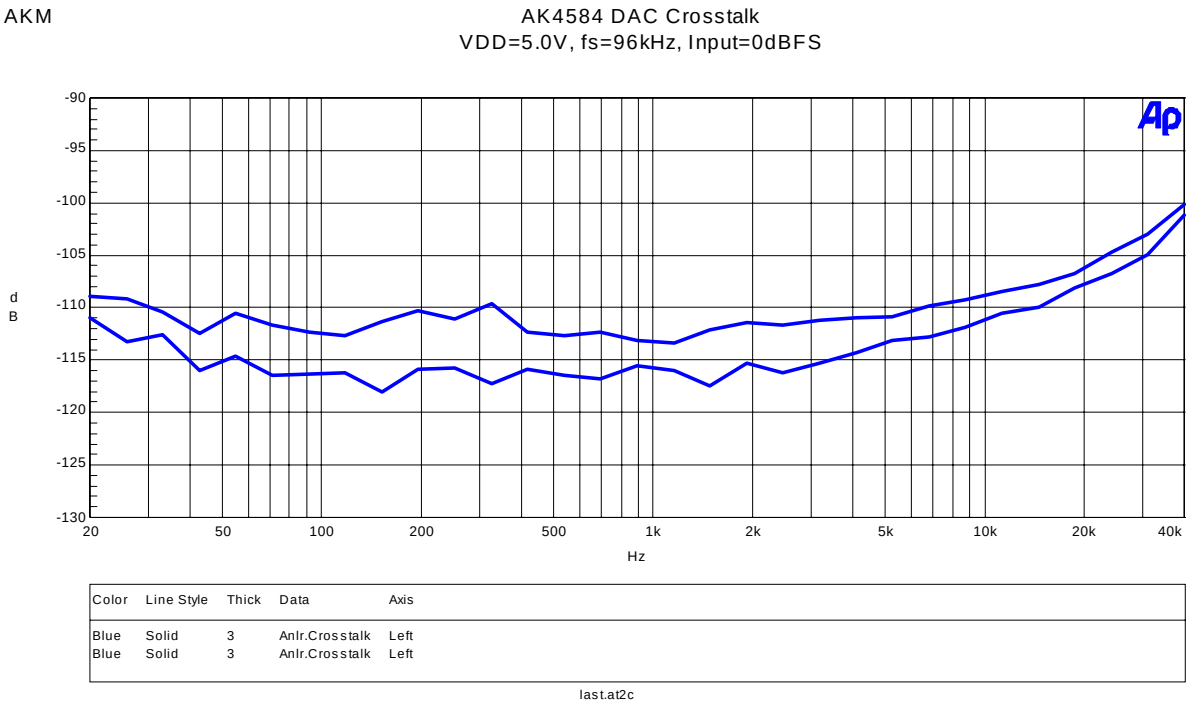


Figure 13. Crosstalk

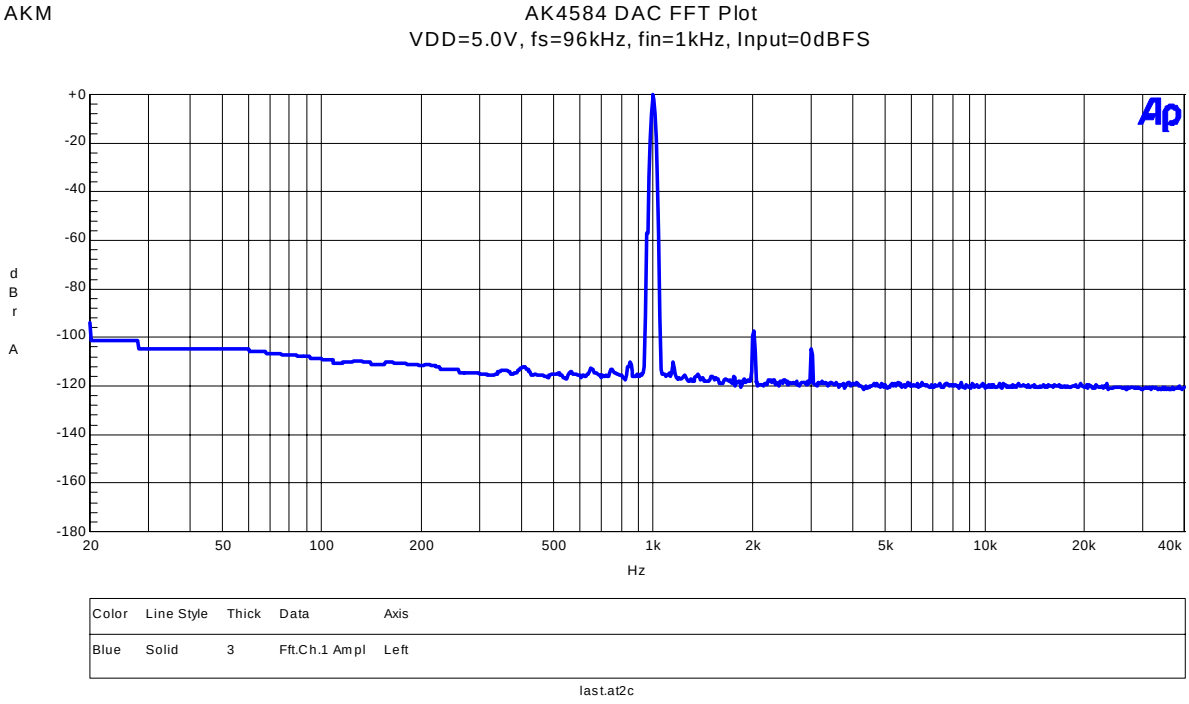


Figure 14. FFT Plot

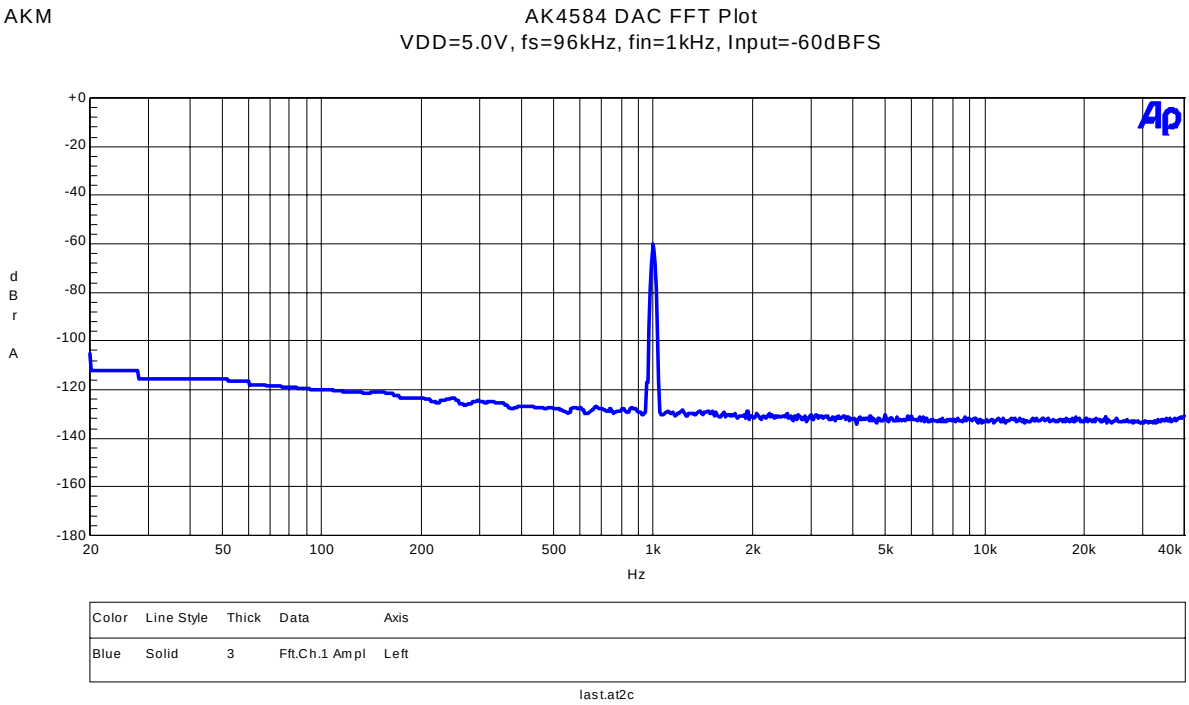


Figure 15. FFT Plot

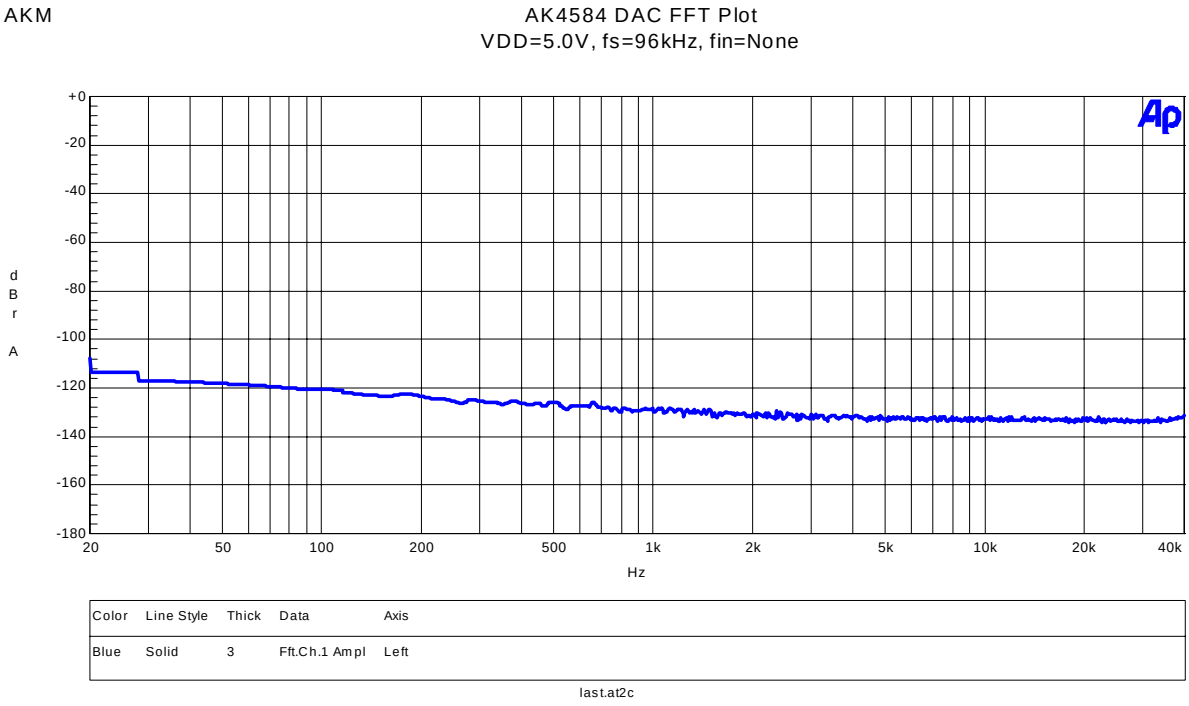


Figure 16. FFT Plot

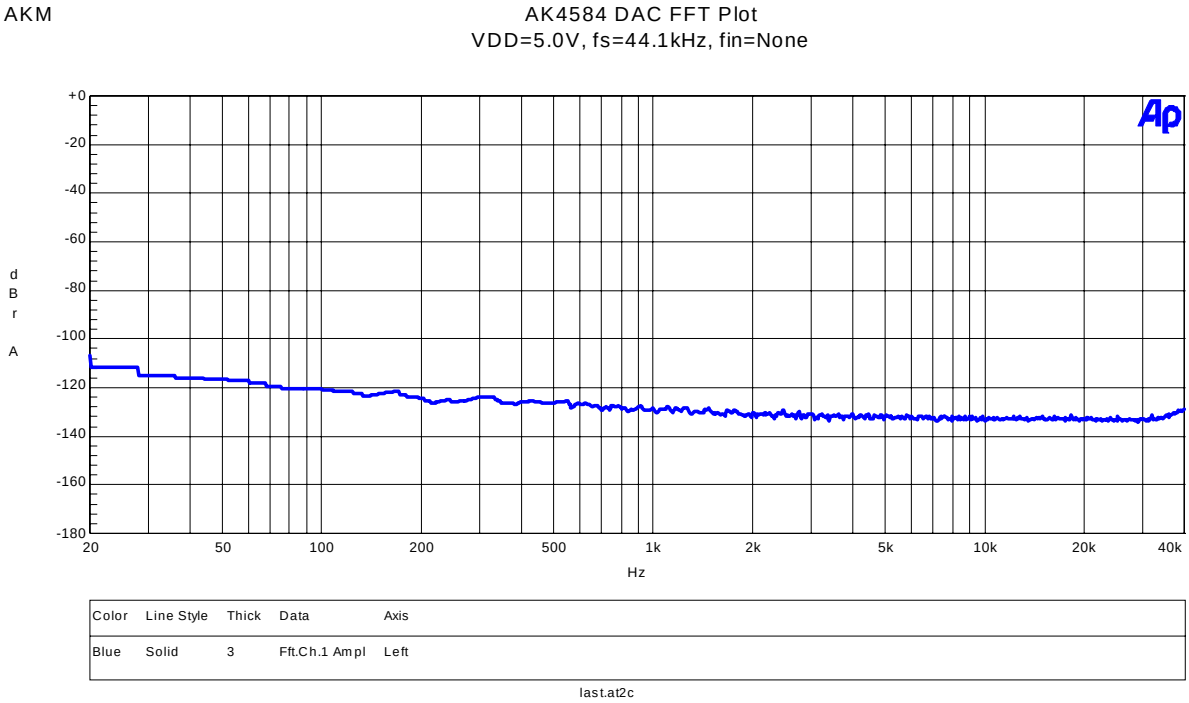


Figure 17. Outband Noise (fs=44.1kHz)

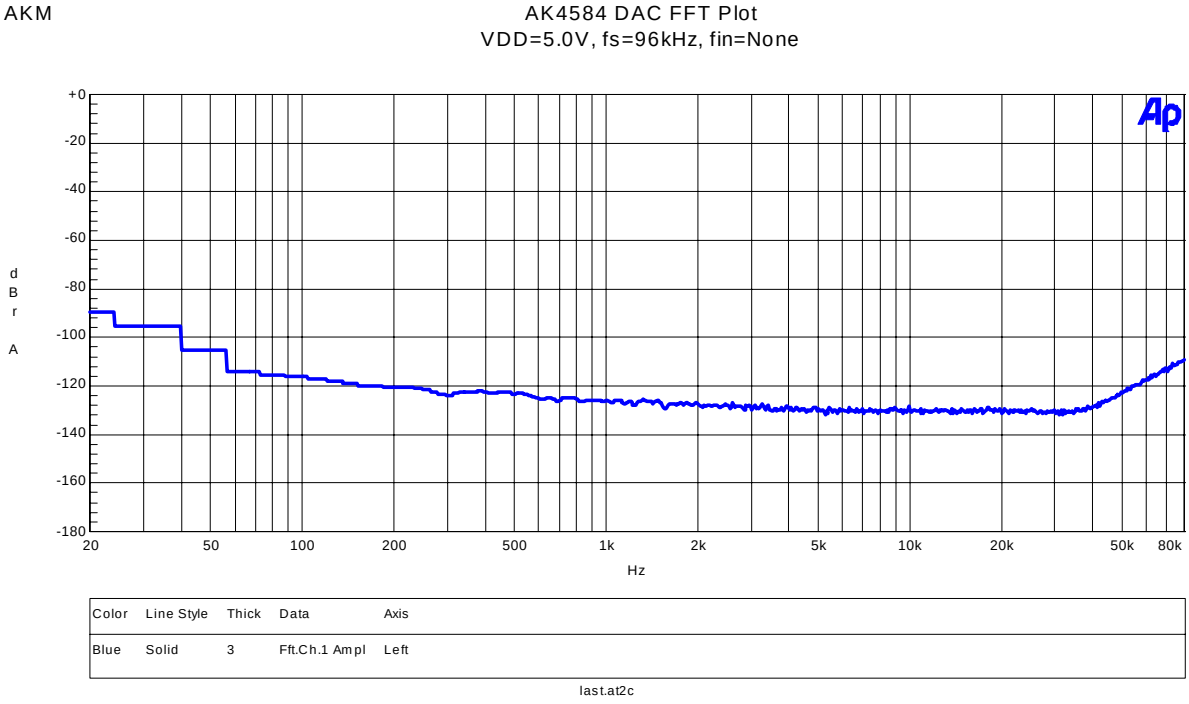


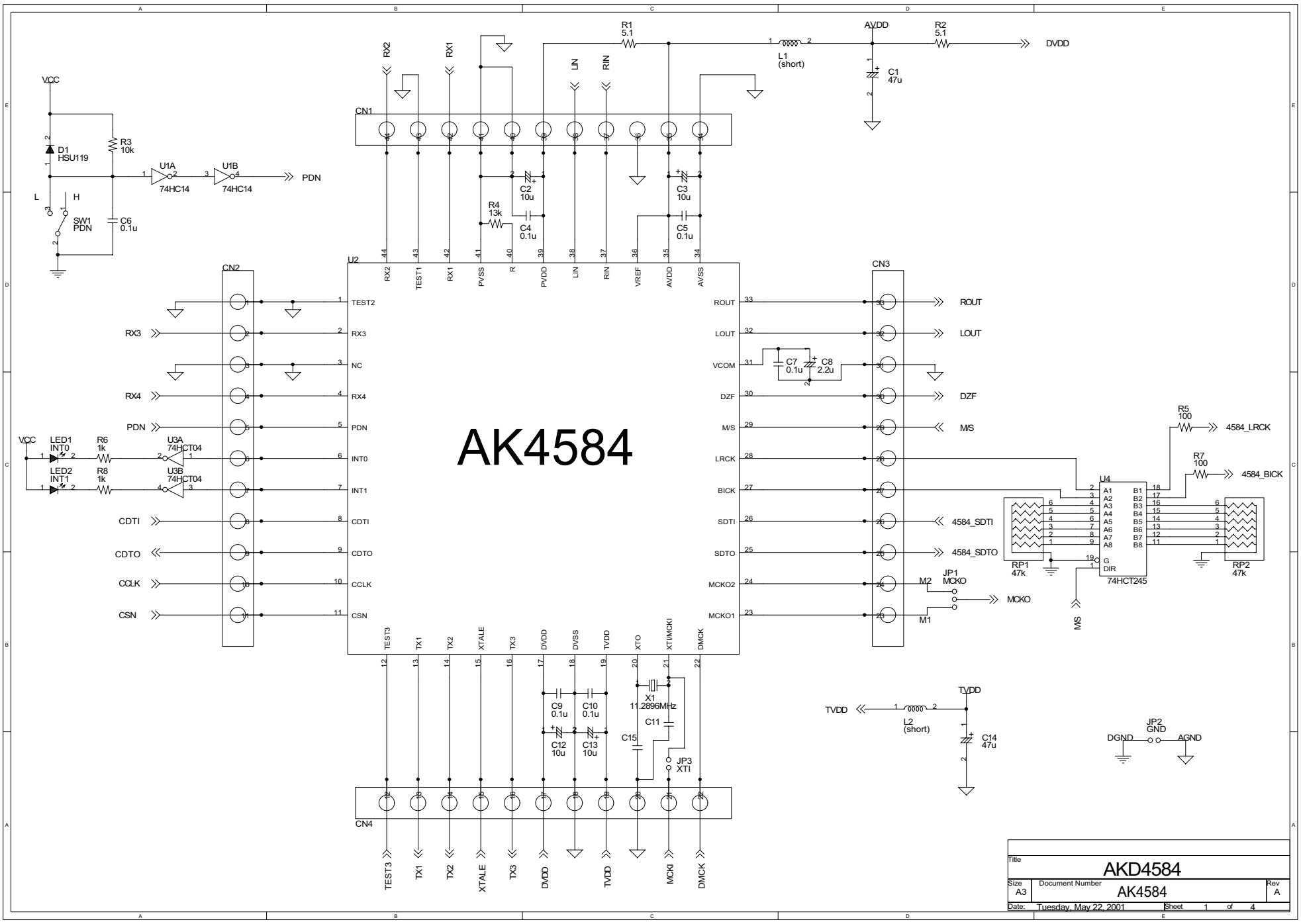
Figure 18. Outband Noise (fs=96kHz)

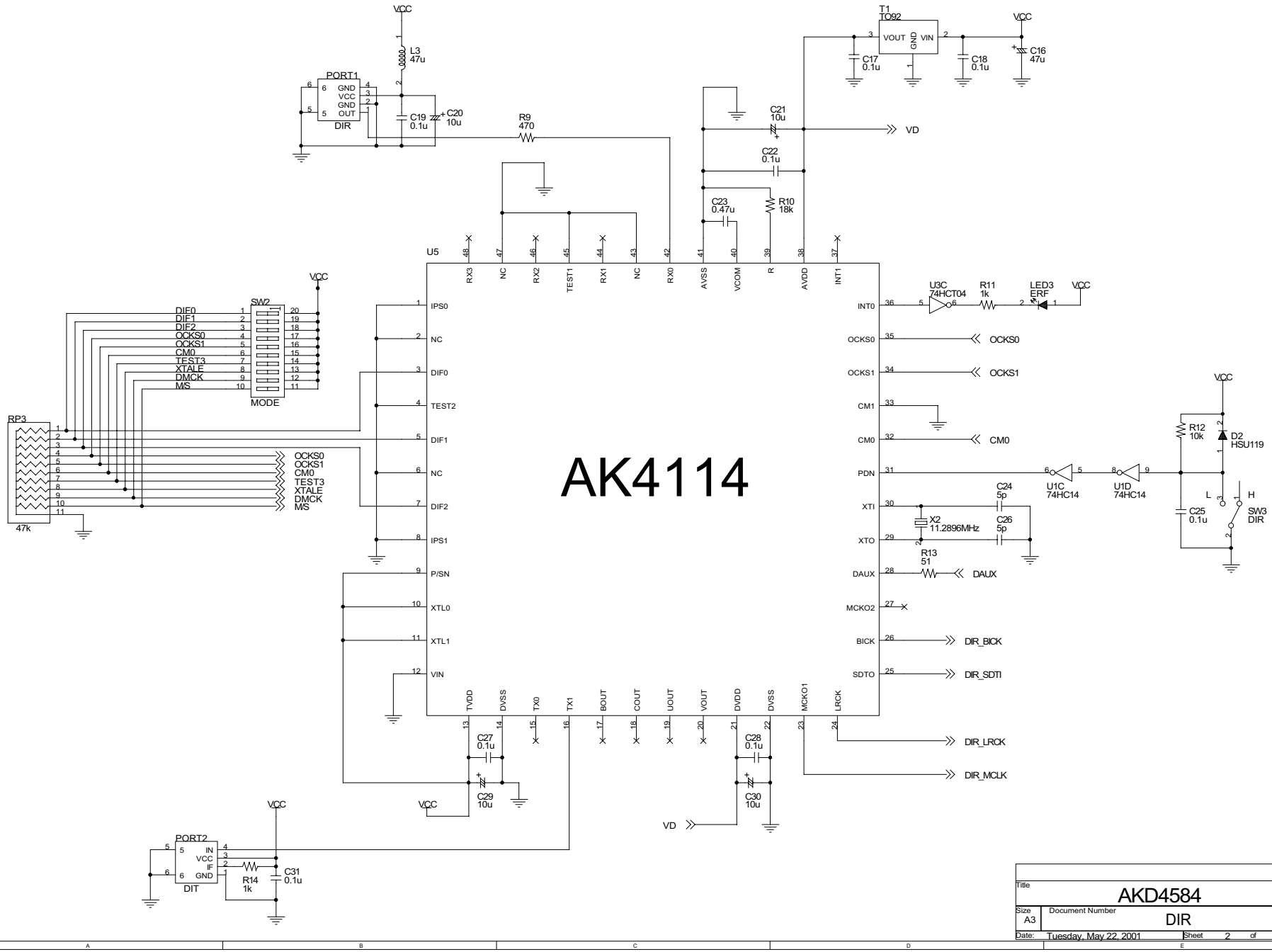
Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
01/11/01	KM065800	0	First Edition	
06/06/26	KM065801	0	Change	Revised Control Software Manual

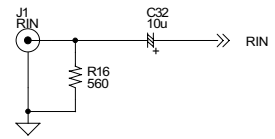
IMPORTANT NOTICE

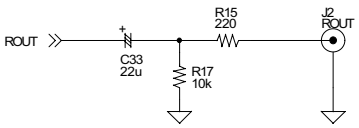
- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.

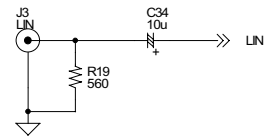

AK4584
VCC
D1
HSU119
R3
10k
U1A
74HC14
U1B
74HC14
PDN
L
H
SW1
PDN
C6
0.1u
R1
5.1
L1
(short)
AVDD
R2
5.1
DVDD
C1
47u
RX2
RX1
LIN
RIN
CN1
C2
10u
C3
10u
R4
13k
C4
0.1u
C5
0.1u
U2
CN2
CN3
RX3
RX4
PDN
CDTI
CDTO
CCLK
CSN
TEST2
NC
INT0
INT1
ROUT
LOUT
VCOM
DZF
M/S
LRCK
BICK
SDTI
SDTO
MCKO2
MCKO1
C7
0.1u
C8
2.2u
LED1
INT0
LED2
INT1
R6
1k
R8
1k
U3A
74HCT04
U3B
74HCT04
4584_SDTI
4584_SDTO
JP1
MCKO
M2
M1
MCKO
R5
100
R7
100
4584_LRCK
4584_BICK
U4
74HCT245
RP1
47k
RP2
47k
TVDD
L2
(short)
C14
47u
JP2
GND
DGND
AGND
TEST3
TX1
TX2
XTALE
TX3
DVDD
DVSS
TVDD
XTO
XTI/MCKI
DMCK
C9
0.1u
C10
0.1u
C12
10u
C13
10u
X1
11.2896MHz
C11
C15
JP3
XTI
CN4
MCKI
Title
AKD4584
Size
A3
Document Number
AK4584
Rev
A
Date:
Tuesday, May 22, 2001
Sheet
1
of
4

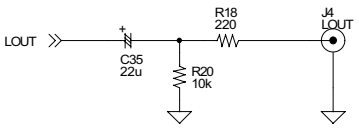


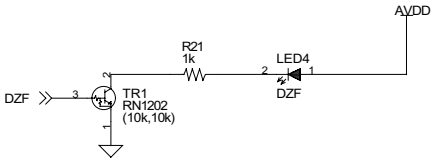
Title	AKD4584	
Size A3	Document Number DIR	Rev A
Date: Tuesday, May 22, 2001	Sheet 2 of 4	

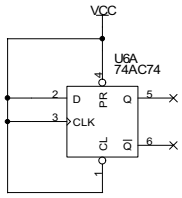


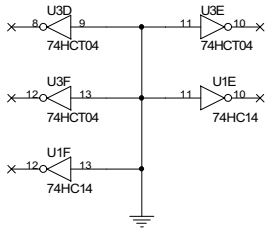




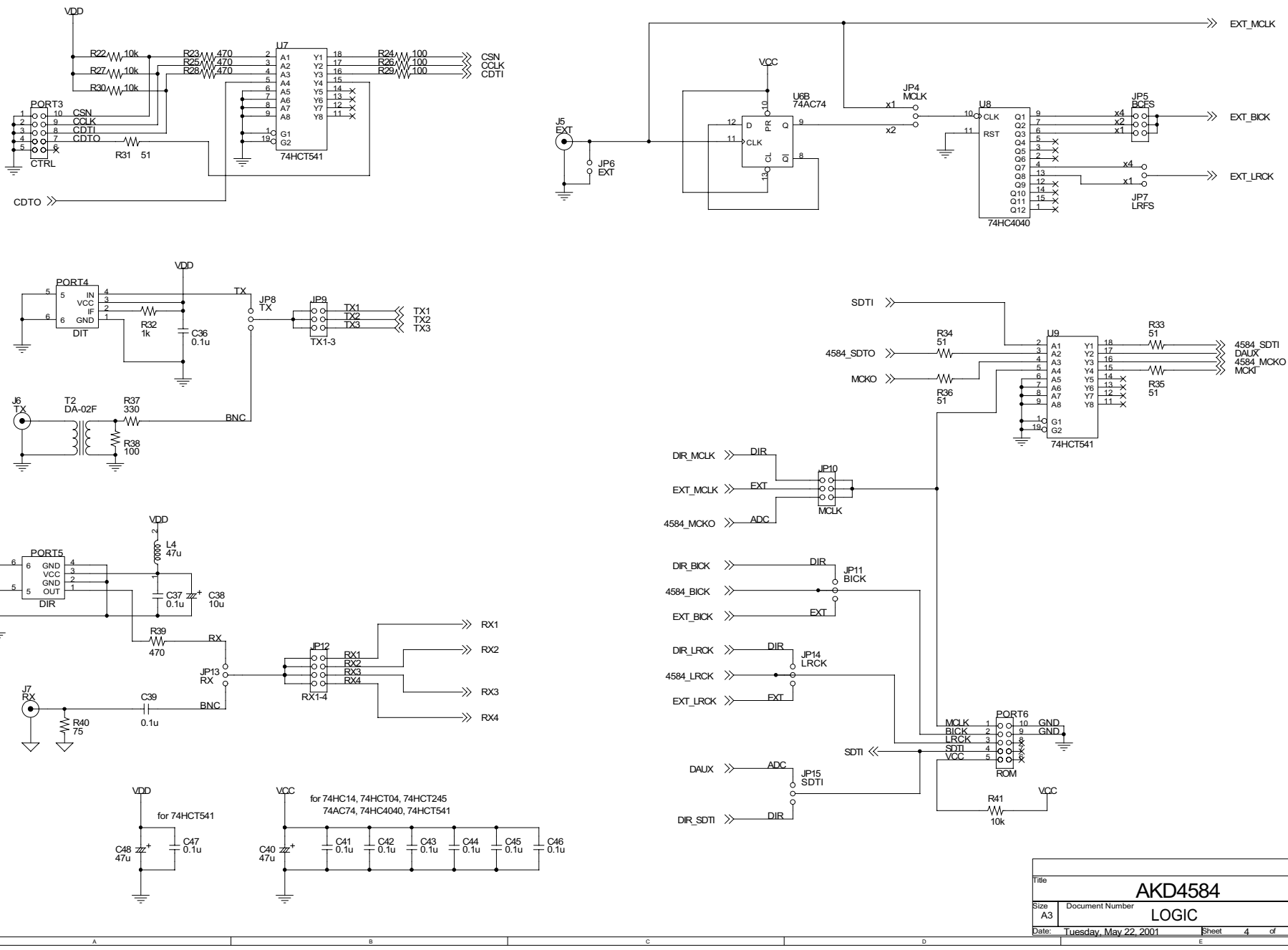




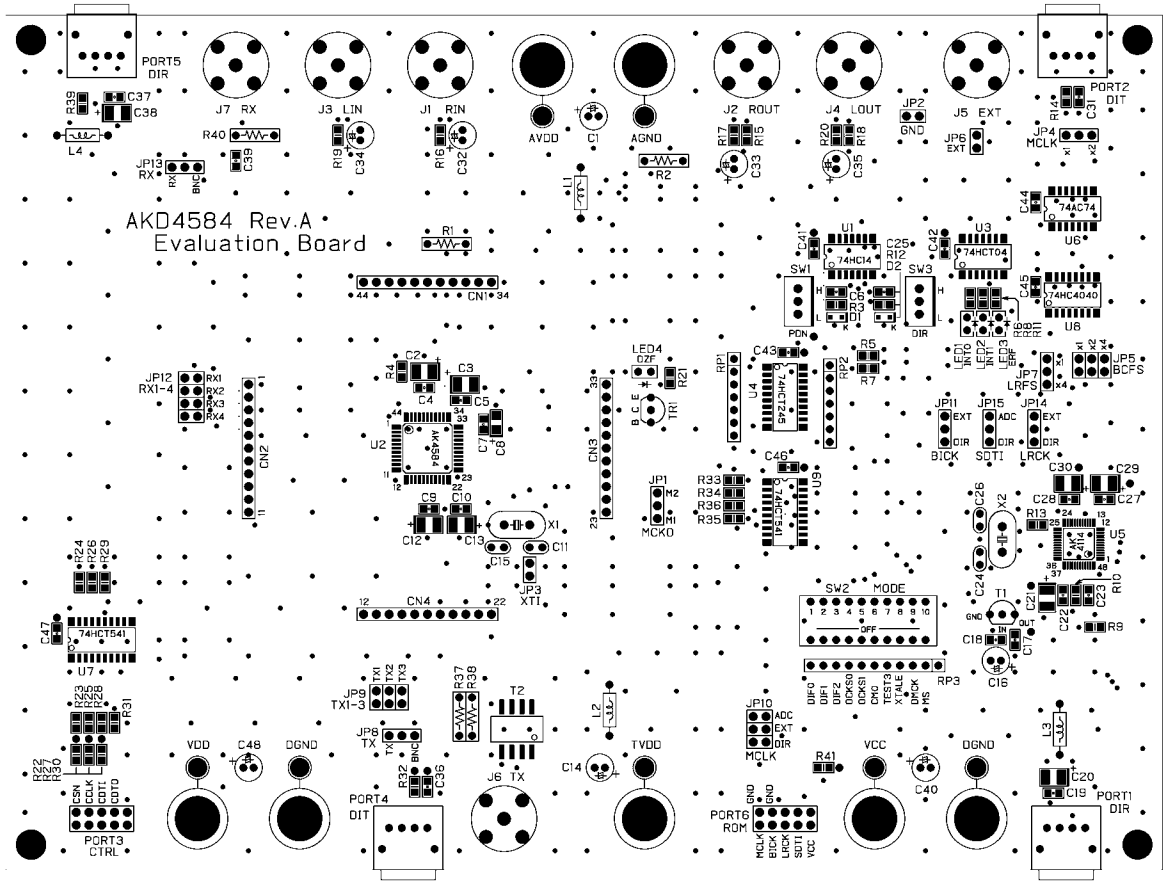




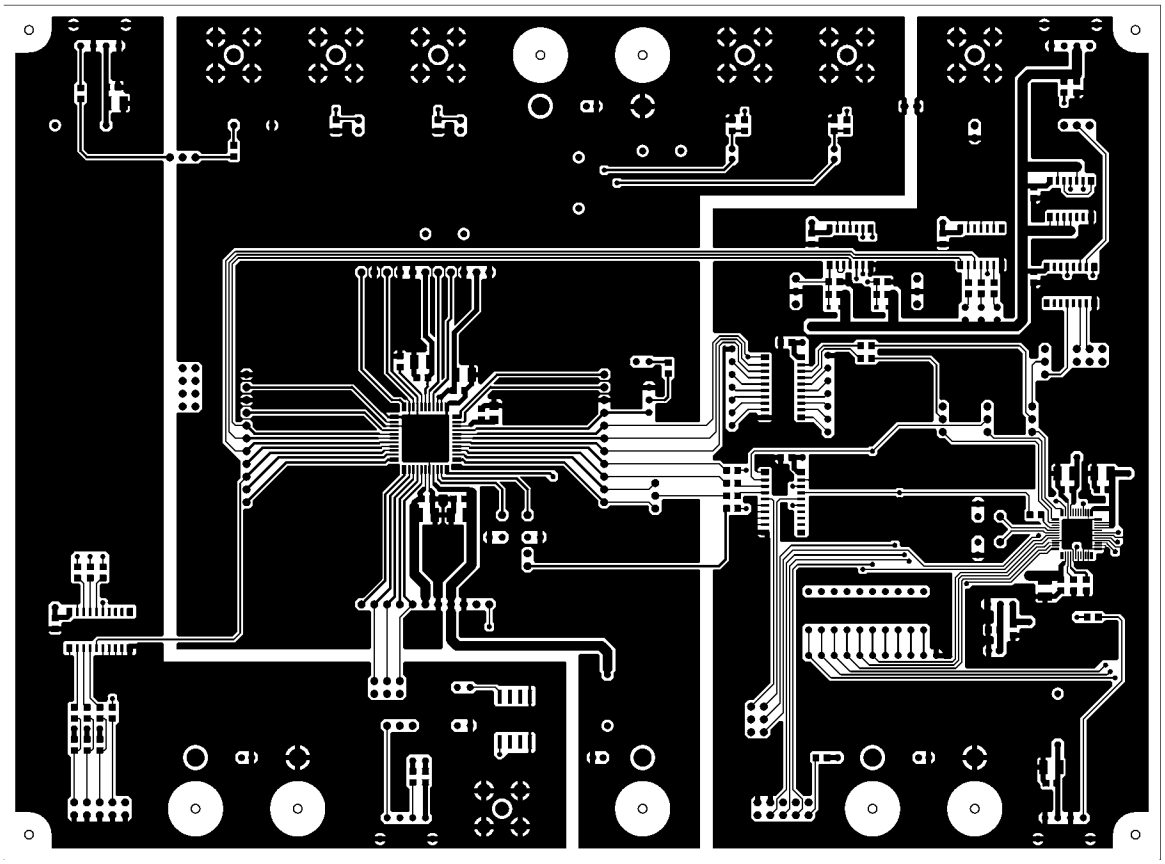
Title	AKD4584	
Size: A3	Document Number: Input/Output	Rev: A
Date: Tuesday, May 22, 2001	Sheet 3 of 4	



Title	AKD4584	
Size A3	Document Number LOGIC	Rev A
Date: Tuesday, May 22, 2001	Sheet 4 of 4	



AKD4584 Rev.A L1 SR SILK



AKD4584 Rev.A L1

AKD4589 Rev.A L2